

## CY62157E MoBL<sup>®</sup>

# 8-Mbit (512K x 16) Static RAM

#### Features

- Very high speed: 45 ns □ Industrial: -40°C to +85°C □ Automotive-E: -40°C to +125°C
- Wide voltage range: 4.5V–5.5V
- Ultra low standby power Typical standby current: 2 μA Maximum standby current: 8 μA (Industrial)
- Ultra low active power Typical active current: 1.8 mA at f = 1 MHz
- Ultra low standby power
- **Easy** memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 44-pin TSOP II and 48-ball VFBGA package

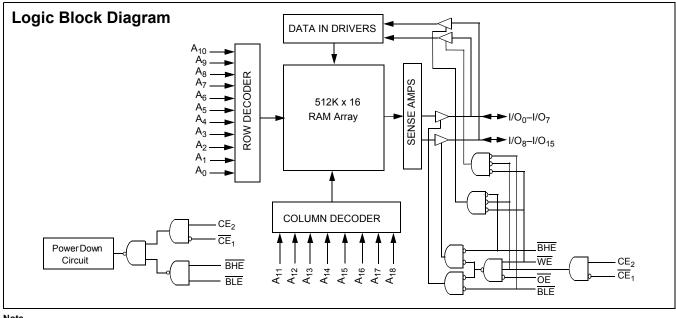
#### Functional Description<sup>[1]</sup>

The CY62157E is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life<sup>™</sup> (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected (CE1 HIGH or CE2 LOW or both BHE and BLE are HIGH). The input or output pins (I/O0 through I/O<sub>15</sub>) are placed in a high impedance state when:

- Deselected (CE<sub>1</sub>HIGH or CE<sub>2</sub> LOW)
- Outputs are disabled (OE HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH)
- Write operation is active (CE<sub>1</sub> LOW, CE<sub>2</sub> HIGH and WE LOW)

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$ HIGH) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A0 through  $A_{18}$ ). If Byte High Enable (BHE) is LOW, then data from I/O pins  $(I/O_8 \text{ through } I/O_{15})$  is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$ HIGH) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O8 to I/O15. See the "Truth Table" on page 10 for a complete description of read and write modes.



Note

1. For best practice recommendations, please refer to the Cypress application note AN1064, SRAM System Guidelines.

**Cypress Semiconductor Corporation** Document #: 38-05695 Rev. \*G

198 Champion Court

San Jose, CA 95134-1709 408-943-2600 Revised December 20, 2010



## CY62157E MoBL<sup>®</sup>

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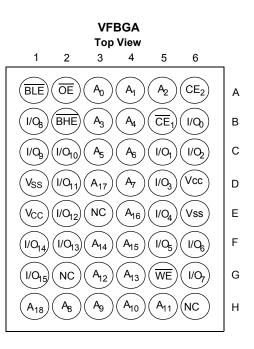
#### **Product Portfolio**

								Power D	issipatio	n				
Product	Banga	V <sub>CC</sub> Range (V)			Speed (ns)	Operating I <sub>CC</sub> , (mA)			<b>v</b> )	Standby, I <sub>SB2</sub>				
FIGURE	Range				. ,	f = 1 MHz		f = 1 MHz		f = 1 MHz f = f <sub>max</sub>				Ă)
		Min	<b>Typ</b> <sup>[2]</sup>	Max		<b>Typ</b> <sup>[2]</sup>	Max	<b>Typ</b> <sup>[2]</sup>	Мах	<b>Typ</b> <sup>[2]</sup>	Max			
CY62157ELL	Industrial	4.5	5.0	5.5	45	1.8	3	18	25	2	8			
CY62157ELL	Automotive	4.5	5.0	5.5	55	1.8	4	18	35	2	30			

### **Pin Configuration**

The following pictures show the TSOP II and VFBGA pinouts.<sup>[3, 4]</sup>

	TSOP II Top View						
A <sub>4</sub> A <sub>3</sub> A <sub>2</sub> L L L L L L L L L L L L L L L L L L L	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24	$\begin{array}{c c} A_5 & A_7 \\ \hline A_7 \\ \hline B \\ \hline B \\ \hline B \\ \hline B \\ \hline C \\ C \\$				
A <sub>15</sub> A <sub>14</sub>	21 22		A <sub>12</sub>				



#### Notes

Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
 NC pins are not connected on the die.
 The 44-pin TSOP II package has only one chip enable (CE) pin.



## CY62157E MoBL<sup>®</sup>

## Maximum Ratings

Electrical Characteristics

Over the Operating Range

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature	–65°C to + 150°C
Ambient Temperature with Power Applied	–55°C to + 125°C
Supply Voltage to Ground Potential	–0.5V to 6.0V
DC Voltage Applied to Outputs in High-Z State <sup>[5, 6]</sup>	–0.5V to 6.0V

#### DC Input Voltage<sup>[5, 6]</sup>.....-0.5V to 6.0V Static Discharge Voltage .....> 2001V (MIL-STD-883, Method 3015) Latch up Current ......> 200 mA

### **Operating Range**

Device	Range	Ambient Temperature	<b>V</b> cc <sup>[7]</sup>	
CY62157ELL	Industrial	–40°C to +85°C	4.5V to 5.5V	
	Automotive	–40°C to +125°C		

#### 45 ns (Industrial) 55 ns (Automotive) Parameter Description **Test Conditions** Unit **Typ**<sup>[8]</sup> **Typ**<sup>[8]</sup> Min Max Min Max V<sub>ОН</sub> Output HIGH V I<sub>OH</sub> = –1 mA 2.4 2.4 Voltage Output LOW 0.4 0.4 V Vol $I_{OI} = 2.1 \text{ mA}$ Voltage VIH Input HIGH V<sub>CC</sub> = 4.5V to 5.5V 2.2 V<sub>CC</sub> + 0.5 V<sub>CC</sub> + 0.5 V 2.2 Voltage Input LOW $V_{CC} = 4.5V$ to 5.5V -0.5 -0.5 0.8 V VII 0.8 Voltage Input Leakage $GND \leq V_1 \leq V_{CC}$ -1 -4 +1 +4 $I_{IX}$ μΑ Current Output Leakage $GND \leq V_O \leq V_{CC}$ , Output Disabled -1 +1 \_4 +4 μA I<sub>OZ</sub> Current V<sub>CC</sub> Operating 18 25 18 35 mΑ I<sub>CC</sub> Supply 1.8 3 1.8 4 Current $\label{eq:cell} \begin{array}{l} \overline{CE}_1 \geq V_{CC} - 0.2V \text{ or } CE_2 \leq 0.2V, \\ V_{IN} \geq V_{CC} - 0.2V, \ V_{IN} \leq 0.2V, \\ f = f_{max} (Address and Data Only), \\ f = 0 (OE, BHE, BLE and WE), \end{array}$ Automatic CE 2 8 2 30 μA I<sub>SB1</sub> Power Down Current — CMOS Inputs $V_{CC} = V_{CC(max)}$ I<sub>SB2</sub> <sup>[9]</sup> Automatic CE 2 8 2 30 μA Power Down Current — CMOS Inputs

#### Capacitance<sup>[10]</sup>

Parameter	Description Test Conditions		Max	Unit
C <sub>IN</sub>	Input Capacitance	$T_A = 25^{\circ}C, f = 1 MHz, V_{CC} = V_{CC(typ)}$	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

#### Notes

Notes
5. V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns for I < 30 mA.</li>
6. V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
7. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub>(min) and 200 μs wait time after V<sub>CC</sub> stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
9. Chip enables (CE<sub>1</sub> and CE<sub>2</sub>) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.
10. Tosted unitality and after any definer optimation and are proceed that may affect these normations.

10. Tested initially and after any design or process changes that may affect these parameters.

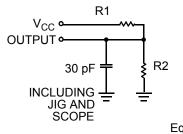


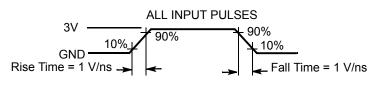
#### Thermal Resistance [11]

Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
$\Theta_{JA}$		Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	77	72	°C/W
Θ <sup>JC</sup>	Thermal Resistance (Junction to Case)		13	8.86	°C/W

#### AC Test Loads and Waveforms







Equivalent to: THEVENIN EQUIVALENT

> R<sub>TH</sub> OUTPUT -<u>~</u> \/

Parameters	Values	Unit						
R1	1800	Ω						
R2	990	Ω						
R <sub>TH</sub>	639	Ω						
V <sub>TH</sub>	1.77	V						

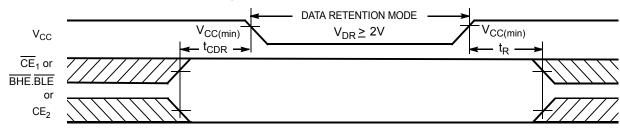
#### **Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions		Min	<b>Typ</b> <sup>[12]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention			2			V
I <sub>CCDR</sub>	Data Retention Current	$V_{CC}=2V, \overline{CE}_{1} \ge V_{CC} - 0.2V \text{ or } CE_{2} \le 0.2V,$ $V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$	Industrial			8	μA
		$V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$	Automotive			30	
t <sub>CDR</sub> <sup>[11]</sup>	Chip Deselect to Data Retention Time			0			ns
t <sub>R</sub> <sup>[13]</sup>	Operation Recovery Time			t <sub>RC</sub>			ns

### Data Retention Waveform<sup>[14]</sup>





#### Notes

**Notes** 11. Tested initially and after any design or process changes that may affect these parameters. 12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C. 13. <u>Full device</u> operation requires line ar  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \ge 100 \ \mu s$  or stable at  $V_{CC(min)} \ge 100 \ \mu s$ . 14. <u>BHE</u>.BLE is the AND of both <u>BHE</u> and <u>BLE</u>. Deselect the chip by either disabling chip enable signals or by disabling both <u>BHE</u> and <u>BLE</u>.



### **Switching Characteristics**

Over the Operating Range<sup>[15, 16]</sup>

Description	45 ns (In	dustrial)	55 ns (Automotive)		Unit
Description	Min	Max	Min	Мах	Unit
Read Cycle Time	45		55		ns
Address to Data Valid		45		55	ns
Data Hold from Address Change	10		10		ns
$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid		45		55	ns
OE LOW to Data Valid		22		25	ns
OE LOW to LOW-Z <sup>[17]</sup>	5		5		ns
OE HIGH to High-Z <sup>[17, 18]</sup>		18		20	ns
$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low-Z <sup>[17]</sup>	10		10		ns
$\overline{CE}_1$ HIGH and $CE_2$ LOW to High-Z <sup>[17, 18]</sup>		18		20	ns
$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up	0		0		ns
$\overline{CE}_1$ HIGH and $CE_2$ LOW to Power Down		45		55	ns
BLE/BHE LOW to Data Valid		45		55	ns
BLE/BHE LOW to Low-Z <sup>[17]</sup>	10		10		ns
BLE/BHE HIGH to HIGH-Z <sup>[17, 18]</sup>		18		20	ns
Write Cycle Time	45		55		ns
$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	35		40		ns
Address Setup to Write End	35		40		ns
Address Hold from Write End	0		0		ns
Address Setup to Write Start	0		0		ns
WE Pulse Width	35		40		ns
BLE/BHE LOW to Write End	35		40		ns
Data Setup to Write End	25		25		ns
Data Hold from Write End	0		0		ns
WE LOW to High-Z <sup>[17, 18]</sup>		18		20	ns
WE HIGH to Low-Z <sup>[17]</sup>	10		10		ns
	Address to Data ValidData Hold from Address Change $\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid $\overline{OE}$ LOW to Data Valid $\overline{OE}$ LOW to LOW- $Z^{[17]}$ $\overline{OE}$ HIGH to High- $Z^{[17, 18]}$ $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low- $Z^{[17]}$ $\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up $\overline{CE}_1$ LOW and $CE_2$ LOW to High- $Z^{[17, 18]}$ $\overline{CE}_1$ LOW and $CE_2$ LOW to Power Down $\overline{BLE}/\overline{BHE}$ LOW to Data Valid $\overline{BLE}/\overline{BHE}$ LOW to Low- $Z^{[17]}$ $\overline{BLE}/\overline{BHE}$ HIGH to HIGH- $Z^{[17, 18]}$ Write Cycle Time $\overline{CE}_1$ LOW and $CE_2$ HIGH to Write EndAddress Setup to Write EndAddress Setup to Write EndAddress Setup to Write Start $\overline{WE}$ Pulse Width $\overline{BLE}/\overline{BHE}$ LOW to Write EndData Hold from Write EndData Hold from Write End $\overline{WE}$ LOW to High- $Z^{[17, 18]}$	DescriptionMinRead Cycle Time45Address to Data Valid10Data Hold from Address Change10 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Data Valid10 $\overline{OE}$ LOW to Data Valid10 $\overline{OE}$ LOW to LOW- $Z^{[17]}$ 5 $\overline{OE}$ HIGH to High- $Z^{[17, 18]}$ 10 $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low- $Z^{[17]}$ 10 $\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up0 $\overline{CE}_1$ HIGH and $CE_2$ LOW to High- $Z^{[17, 18]}$ $\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Down $\overline{BLE/BHE}$ LOW to Data Valid $\overline{BLE/BHE}$ LOW to Low- $Z^{[17]}$ 10 $\overline{BLE/BHE}$ HIGH to HIGH- $Z^{[17, 18]}$ Write Cycle Time $45$ $\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End $35$ Address Setup to Write End $35$ Address Setup to Write End $0$ $\overline{WE}$ Pulse Width $35$ $\overline{BLE/BHE}$ LOW to Write End $35$ Data Setup to Write End $25$ Data Hold from Write End $0$ $\overline{WE}$ LOW to High- $Z^{[17, 18]}$	Read Cycle Time45Address to Data Valid45Data Hold from Address Change10 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Data Valid45 $\overline{OE}$ LOW to Data Valid22 $\overline{OE}$ LOW to LOW-Z <sup>[17]</sup> 5 $\overline{OE}$ HIGH to High-Z <sup>[17, 18]</sup> 18 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Low-Z <sup>[17]</sup> 10 $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low-Z <sup>[17]</sup> 10 $\overline{CE}_1$ LOW and $CE_2$ LOW to High-Z <sup>[17, 18]</sup> 18 $\overline{CE}_1$ LOW and $CE_2$ LOW to Power Up0 $\overline{CE}_1$ HIGH and $CE_2$ LOW to Power Down45 $\overline{BLE}/\overline{BHE}$ LOW to Data Valid45 $\overline{BLE}/\overline{BHE}$ LOW to Low-Z <sup>[17]</sup> 10 $\overline{BLE}/\overline{BHE}$ LOW to Low-Z <sup>[17]</sup> 10 $\overline{BLE}/\overline{BHE}$ HIGH to HIGH-Z <sup>[17, 18]</sup> 18Write Cycle Time45 $\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End35Address Setup to Write End35Address Setup to Write End35 $\overline{Address}$ Setup to Write End35 $\overline{BLE}/\overline{BHE}$ LOW to Write End35 $\overline{Data}$ Hold from Write End0 $\overline{WE}$ LOW to High-Z <sup>[17, 18]</sup> 18	DescriptionMinMaxMinRead Cycle Time4555Address to Data Valid4510Data Hold from Address Change1010 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Data Valid4522 $\overline{OE}$ LOW to Data Valid22 $\overline{OE}$ LOW to LOW-Z <sup>[17]</sup> $\overline{OE}$ LOW to LOW-Z <sup>[17]</sup> 55 $\overline{OE}$ HIGH to High-Z <sup>[17, 18]</sup> 18 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Low-Z <sup>[17]</sup> 10 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Power Up0 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Power Up0 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Power Up0 $\overline{CE}_1 LOW$ and $CE_2 LOW to Power Down45\overline{BLE/BHE} LOW to Data Valid45\overline{BLE/BHE} LOW to Low-Z[17]10\overline{BLE/BHE} HIGH to HIGH-Z[17, 18]18Write Cycle Time45\overline{CE}_1 LOW and CE_2 HIGH to Write End3540Address Setup to Write End3540Address Setup to Write End3540\overline{MEP} Pulse Width353540\overline{BLE/BHE} LOW to Write End3540\overline{ME} Pulse Width3540\overline{ME} Pulse Width252525Data Hold from Write End000\overline{W} LOW to High-Z[17, 18]18$	DescriptionMinMaxMinMaxRead Cycle Time4555Address to Data Valid4555Data Hold from Address Change1010 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Data Valid4555 $\overline{OE}$ LOW to Data Valid4555 $\overline{OE}$ LOW to Data Valid2225 $\overline{OE}$ LOW to LOW-Z <sup>[17]</sup> 55 $\overline{OE}$ HIGH to High-Z <sup>[17, 18]</sup> 1820 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Low-Z <sup>[17]</sup> 1010 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Power Up00 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Power Up00 $\overline{CE}_1 HIGH$ and $CE_2 LOW$ to Power Down4555 $\overline{BLE/BHE}$ LOW to Data Valid4555 $\overline{BLE/BHE}$ LOW to Low-Z <sup>[17]</sup> 1010 $\overline{DE}_1 HIGH$ to HIGH-Z <sup>[17, 18]</sup> 1820 $\overline{CE}_1 HIGH$ and $CE_2 LOW$ to Power Down4555 $\overline{BLE/BHE}$ LOW to Low-Z <sup>[17]</sup> 1010 $\overline{DE}_1 HIGH$ to HIGH-Z <sup>[17, 18]</sup> 1820 $\overline{CE}_1 LOW$ and $CE_2$ HIGH to Write End3540Address Setup to Write End3540Address Setup to Write End3540Address Setup to Write End3540Address Setup to Write End3540 $\overline{DE}_1 HIGH ELOW to Write End3540\overline{DE}_1 LOW to Write End3540\overline{DE}_1 LOW to Write End3540\overline{DE}_1 LOW to Write End3540\overline{DE}_2 HIGH to Write End35<$

Notes

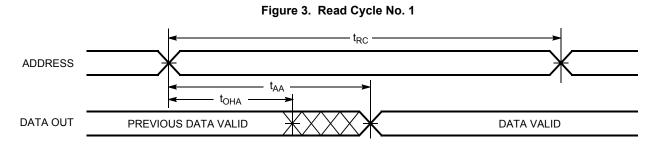
- Notes
  15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0 to V<sub>CC(typ)</sub>, and output loading of the specified <u>In //<sub>OH</sub> as</u> shown in the "AC Test Loads and Waveforms" on page 5.
  16. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application not AN13842 for further clarification.
  17. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZDE</sub>, t<sub>HZDE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
  18. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
  19. The internal write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE, BLE, or both = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

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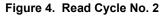


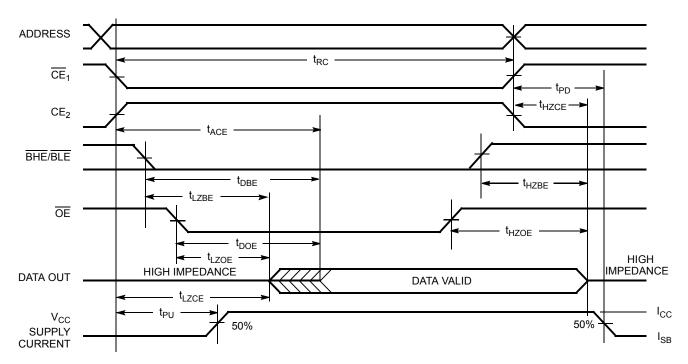
#### **Switching Waveforms**

Read Cycle No. 1 (Address Transition Controlled)<sup>[20, 21]</sup>



### Read Cycle No. 2 (OE Controlled)<sup>[21, 22]</sup>





#### Notes

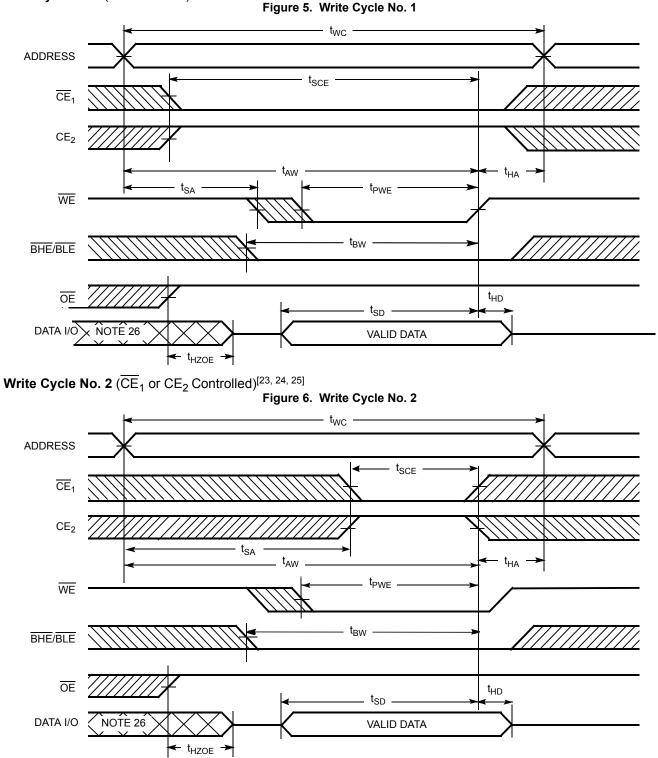
20. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . 21. WE is HIGH for read cycle.

22. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.



## Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled)<sup>[23, 24, 25]</sup>



Notes

- 23. The internal write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE, BLE, or both = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 24. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 25. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{H}$ , the output remains in a high impedance state.
- 26. During this period, the I/Os are in output state. Do not apply input signals.

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### Switching Waveforms (continued)

Write Cycle No. 3 (WE Controlled, OE LOW)<sup>[27]</sup>

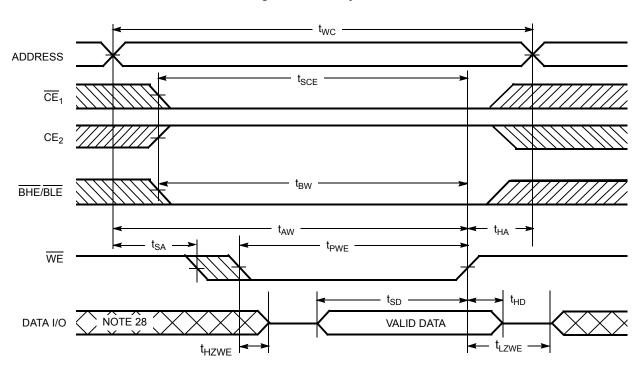
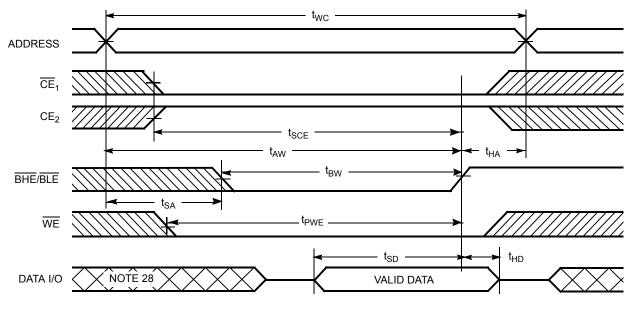


Figure 7. Write Cycle No. 3

Figure 8. Write Cycle No. 4



#### Notes

27. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{|H|}$ , the output remains in a high impedance state. 28. During this period, the I/Os are in output state. Do not apply input signals.

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Write Cycle No. 4  $(\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[27]</sup>





### **Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	X <sup>[29]</sup>	Х	Х	Х	Х	High-Z	Deselect/Power Down	Standby (I <sub>SB</sub> )
X <sup>[29]</sup>	L	Х	Х	Х	Х	High-Z	Deselect/Power Down	Standby (I <sub>SB</sub> )
X <sup>[29]</sup>	X <sup>[29]</sup>	Х	Х	Н	Н	High-Z	Deselect/Power Down	Standby (I <sub>SB</sub> )
L	Н	Н	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	L	Н	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); High-Z (I/O <sub>8</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	L	L	Н	High-Z (I/O <sub>0</sub> –I/O <sub>7</sub> ); Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	Н	L	Н	High-Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	Н	Н	Н	L	High-Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	Н	Н	L	L	High-Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	L	Х	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	L	Х	Н	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); High-Z (I/O <sub>8</sub> –I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	L	Х	L	Н	High-Z (I/O <sub>0</sub> –I/O <sub>7</sub> ); Data In (I/O <sub>8</sub> –I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )

Note 29. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

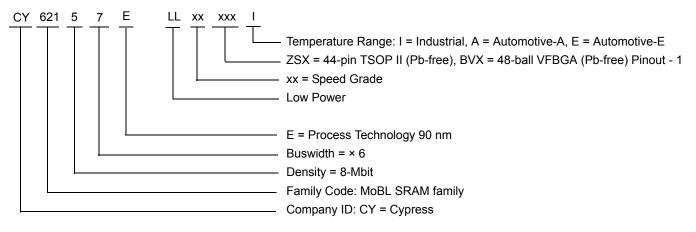


#### **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157ELL-45ZSXI	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	Industrial
55	CY62157ELL-55ZSXE	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	Automotive
	CY62157ELL-55BVXE	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

#### **Ordering Code Definitions**





### Package Diagrams

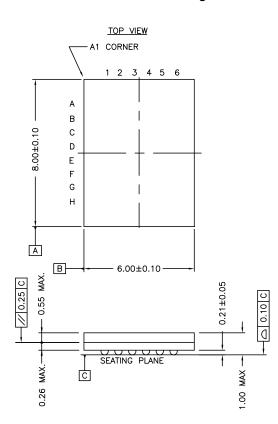
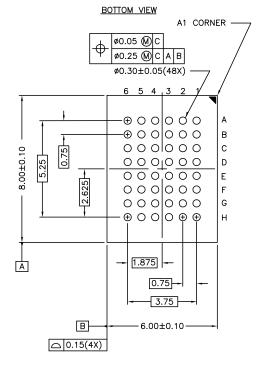


Figure 9. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



51-85150 \*F



### Package Diagrams (continued)

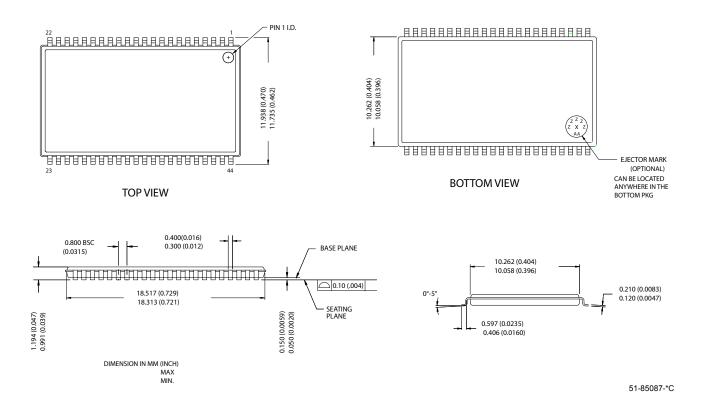


Figure 10. 44-Pin TSOP II, 51-85087



### **Document History Page**

Document Title: CY62157E MoBL <sup>®</sup> , 8-Mbit (512K x 16) Static RAM Document Number: 38-05695						
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change		
**	291273	See ECN	PCI	New data sheet		
*A	457689	See ECN	NXR	Added Automotive Product Removed Industrial Product Removed 35 ns and 45 ns speed bins Removed "L" bin Updated AC Test Loads table Corrected $t_R$ in Data Retention Characteristics from 100 µs to $t_{RC}$ ns Updated the Ordering Information and replaced the Package Name column with Package Diagram		
*B	467033	See ECN	NXR	Added Industrial Product (Final Information) Removed 48 ball VFBGA package and its relevant information Changed the $I_{CC(typ)}$ value of Automotive from 2 mA to 1.8 mA for f = 1MHz Changed the $I_{SB2(typ)}$ value of Automotive from 5 $\mu$ A to 1.8 $\mu$ A Modified footnote #4 to include current limit Updated the Ordering Information table		
*C	569114	See ECN	VKN	Added 48 ball VFBGA package Updated Logic Block Diagram Added footnote #3 Updated the Ordering Information table		
*D	925501	See ECN	VKN	Added footnote #9 related to I <sub>SB2</sub> and I <sub>CCDR</sub> Added footnote #14 related AC timing parameters		
*E	1045801	See ECN	VKN	Converted Automotive specs from preliminary to final		
*F	2934396	06/03/10	VKN	Added footnote #23 related to chip enable Updated package diagrams Updated template.		
*G	3110053	12/14/2010	PRAS	Changed Table Footnotes to Footnotes. Added Ordering Code Definitions.		



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#### Revised December 20, 2010

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