CY62158E MoBL®

8-Mbit (1M x 8) Static RAM

Features

- Very high speed: 45 ns
  - Wide voltage range: 4.5V – 5.5V
- Ultra low active power
  - Typical active current:1.8 mA at f = 1 MHz
  - Typical active current: 18 mA at f = f_{max}
- Ultra low standby power
  - Typical standby current: 2 μA
  - Maximum standby current: 8 μA
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 44-Pin TSOP II package

Functional Description

The CY62158E MoBL® is a high performance CMOS static RAM organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption significantly when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW).

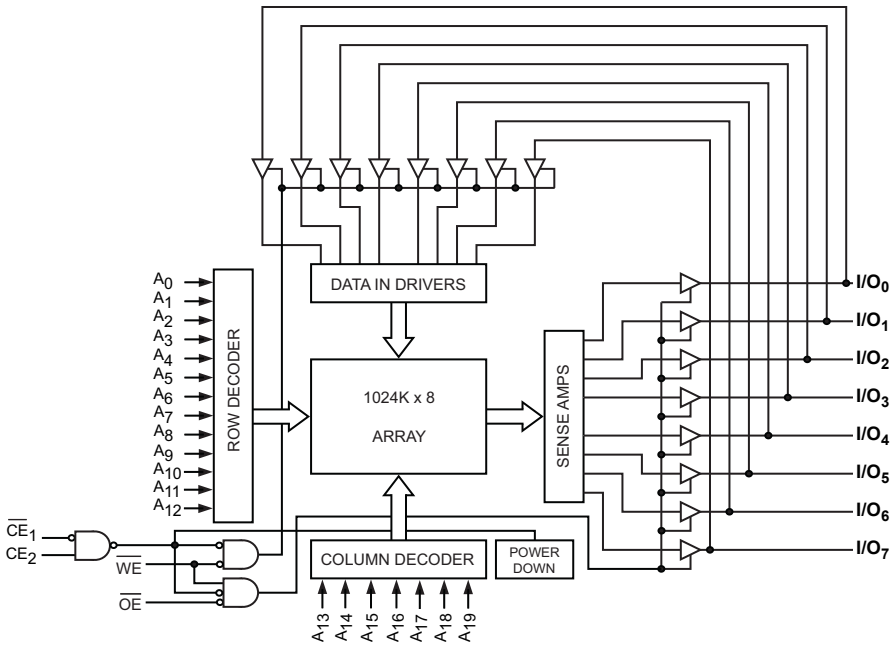
To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and $\overline{OE}$ LOW while forcing the $\overline{WE}$ HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the Truth Table on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines

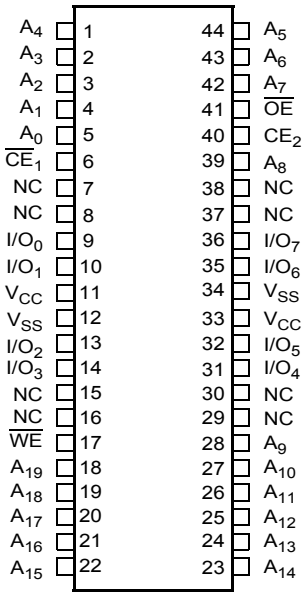
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 44-Pin TSOP II (Top View) [1]



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62158ELL	4.5	5.0	5.5	45	1.8	3	18	25	2	8

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to $V_{CC(max)}$ + 0.5V

DC Voltage Applied to Outputs in High-Z State [3, 4] ..... –0.5V to $V_{CC(max)}$ + 0.5V

DC Input Voltage [3, 4] ..... –0.5V to $V_{CC(max)}$ + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (MIL-STD-883, Method 3015)

Latch up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [5]
CY62158ELL	Industrial	–40°C to +85°C	4.5V – 5.5V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-45			Unit
			Min	Typ [2]	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –1 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 4.5V to 5.5V	2.2		V_{CC} + 0.5V	V
V_{IIL}	Input LOW Voltage	V_{CC} = 4.5V to 5.5V	–0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}; V_{CC} = V_{CCmax}, I_{OUT} = 0 mA, CMOS levels		18	25	mA
		f = 1 MHz; V_{CC} = V_{CCmax}, I_{OUT} = 0 mA, CMOS levels		1.8	3	mA
I_{SB1}	Automatic CE Power down Current — CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V, CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V), f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = V_{CCmax}		2	8	µA
I_{SB2} [6]	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = V_{CCmax}		2	8	µA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance

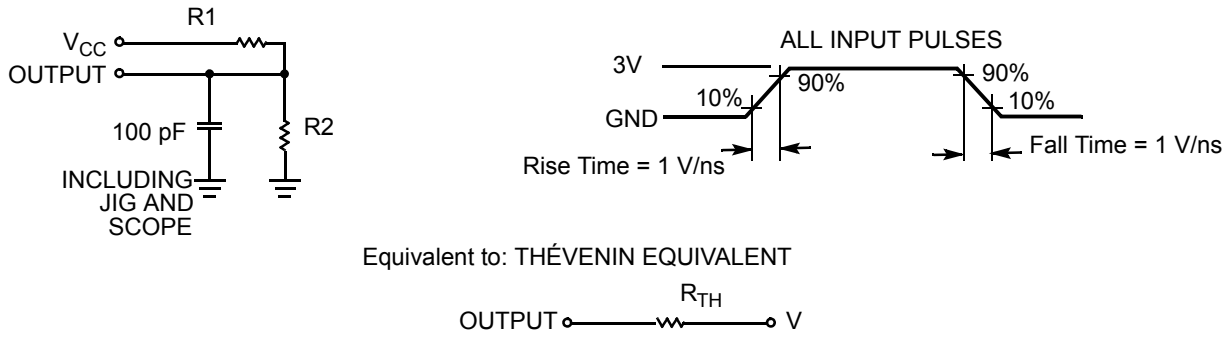
Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75.13	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		8.95	°C/W

Notes

3. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
4. V_{IH}(max) = V_{CC} + 0.75V for pulse durations less than 20 ns.
5. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
6. Chip enables ($\overline{CE_1}$ and CE_2), must be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Figure 2. AC Test Loads and Waveforms



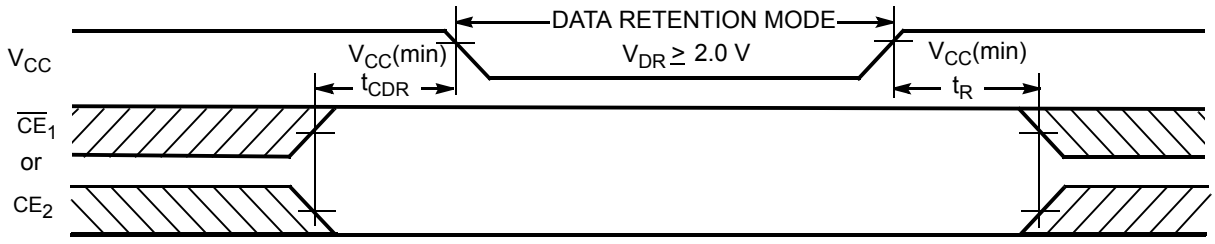
Parameters	5.0V	Unit
R1	1838	Ω
R2	994	Ω
R_{TH}	645	Ω
V_{TH}	1.75	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [7]	Max	Unit
V_{DR}	V_{CC} for Data Retention		2			V
I_{CCDR} [8]	Data Retention Current	$V_{CC} = V_{DR}$ $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			8	µA
t_{CDR} [9]	Chip Deselect to Data Retention Time		0			ns
t_R [10]	Operation Recovery Time		t_{RC}			ns

Figure 3. Data Retention Waveform



Notes

7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
8. Chip enables ($\overline{CE_1}$ and CE_2), must be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 100 µs or stable at V_{CC}(min) ≥ 100 µs.

Switching Characteristics

Over the Operating Range [11]

Parameter	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [12]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [12, 13]		18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z [12]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z [12, 13]		18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power Down		45	ns
Write Cycle [14]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35		ns
t_{AW}	Address Setup to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [12, 13]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [12]	10		ns

Notes

11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in "AC Test Loads and Waveforms" on page 5.
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
13. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
14. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4 shows address transition controlled read cycle waveforms.[15, 16]

Figure 4. Read Cycle No. 1

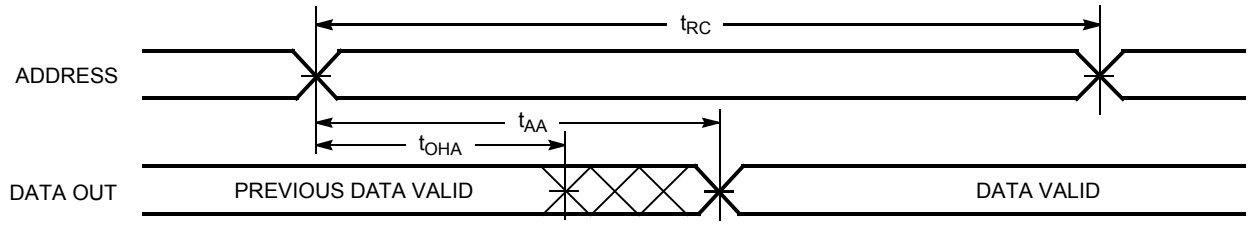
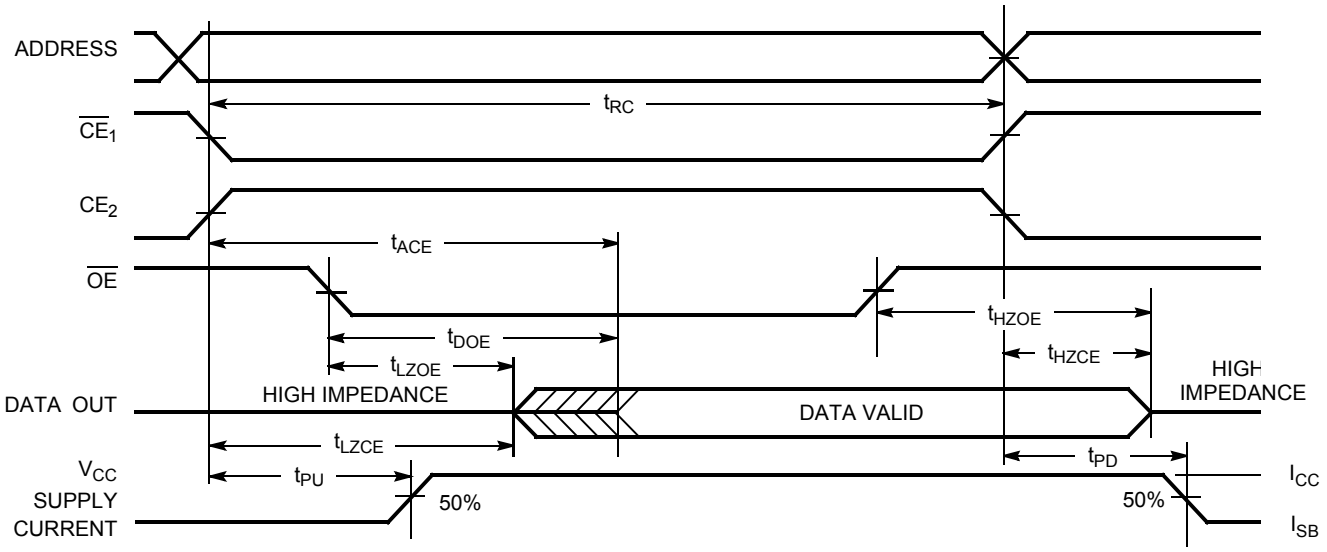


Figure 5 shows $\overline{OE}$ controlled read cycle waveforms.[16, 17]

Figure 5. Read Cycle No. 2



Notes
15. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid before or similar to $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6 shows $\overline{WE}$ controlled write cycle waveforms.[18, 19, 20]

Figure 6. Write Cycle No. 1

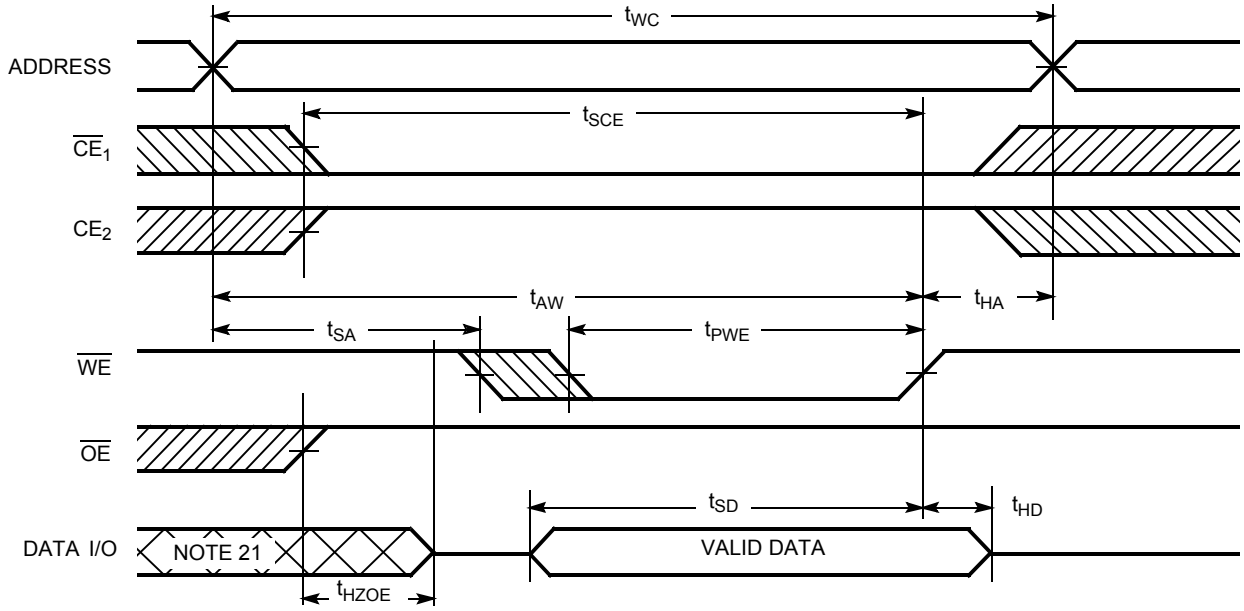
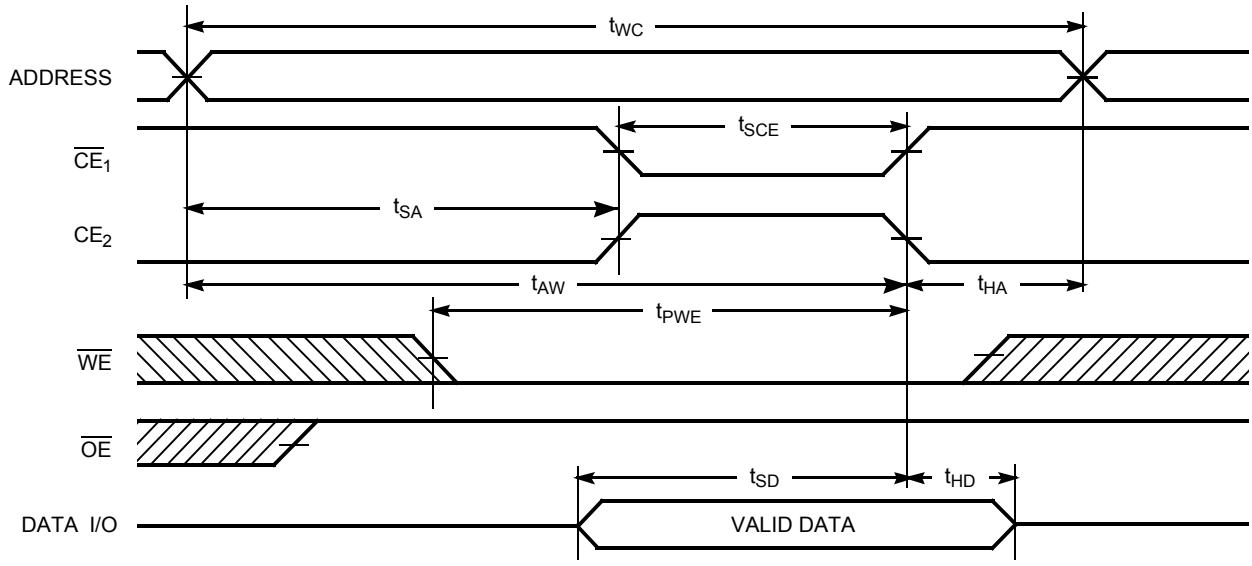


Figure 7 shows $\overline{CE}_1$ or CE_2 controlled write cycle waveforms.[18, 19, 20]

Figure 7. Write Cycle No. 2



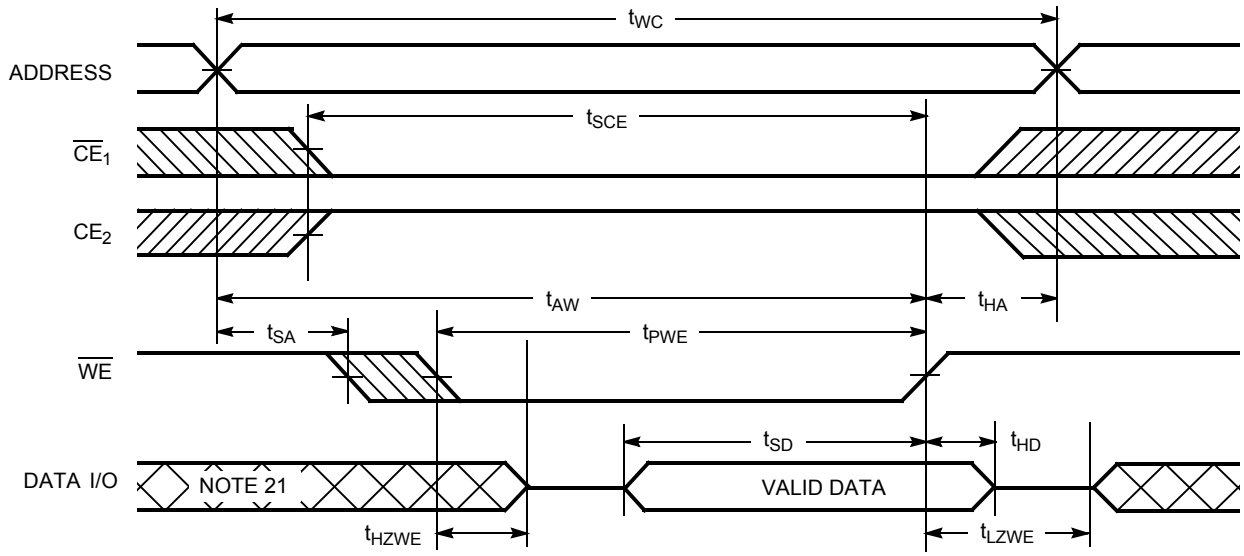
Notes

18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
20. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
21. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8 shows $\overline{WE}$ controlled, $\overline{OE}$ LOW write cycle waveforms.[20]

Figure 8. Write Cycle No. 3



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X[22]	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X[22]	L	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})

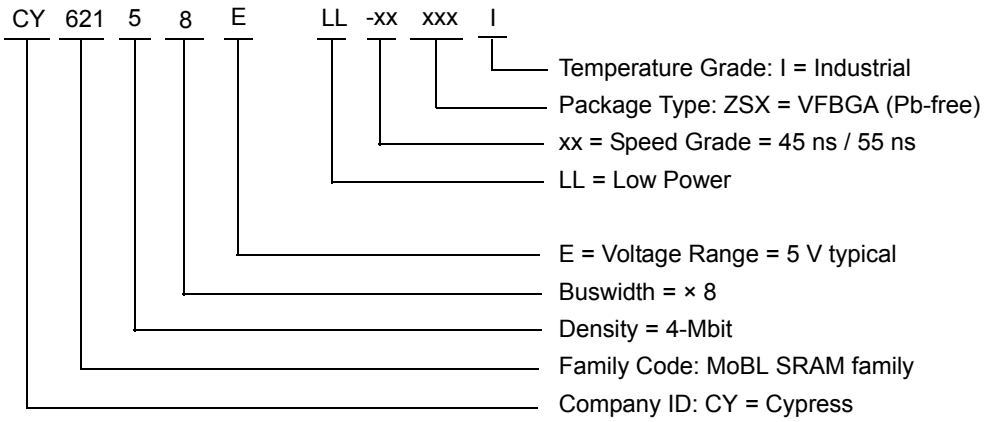
Note
22. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62158ELL-45ZSXI	51-85087	44-Pin TSOP II (Pb-free)	Industrial

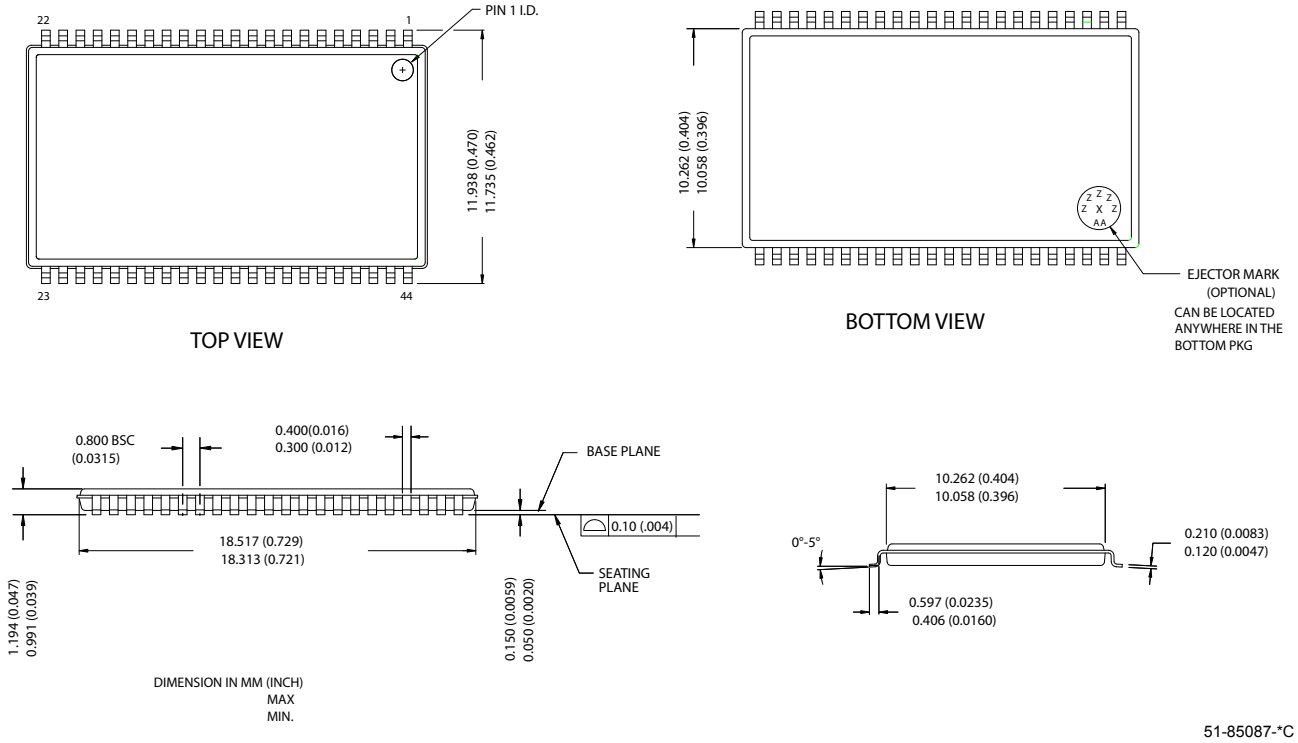
Contact your local Cypress sales representative for availability of this part.

Ordering Code Definitions



Package Diagrams

Figure 9. 44-Pin TSOP II, 51-85087



Document History Page

Document Title: CY62158E MoBL® 8-Mbit (1M x 8) Static RAM Document Number: 38-05684				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	270350	See ECN	PCI	New Data Sheet
*A	291271	See ECN	SYT	Converted from Advance Information to Preliminary Changed input pulse level from V_{CC} to 3V in the AC Test Loads and Waveforms Modified footnote #9 to include timing reference level of 1.5V and input pulse level of 3V
*B	1462592	See ECN	VKN/AESA	Converted from preliminary to final Removed 35 ns speed bin Removed “L” parts Removed 48-Ball VFBGA package Changed $I_{CC(max)}$ spec from 2.3 mA to 3 mA at f=1 MHz Changed $I_{CC(typ)}$ spec from 16 mA to 18 mA at f=f_{MAX} Changed $I_{CC(max)}$ spec from 28 mA to 25 mA at f=f_{MAX} Changed $I_{SB1(typ)}$ and $I_{SB2(typ)}$ spec from 0.9 μA to 2 μA Changed $I_{SB1(max)}$ and $I_{SB2(max)}$ spec from 4.5 μA to 8 μA Changed $I_{CCDR(max)}$ spec from 4.5 μA to 8 μA Changed t_{LZOE} spec from 3 ns to 5 ns Changed t_{LZCE} spec from 6 ns to 10 ns Changed t_{HZCE} spec from 22 ns to 18 ns Changed t_{PWE} spec from 30 ns to 35 ns Changed t_{SD} spec from 22 ns to 25 ns Changed t_{LZWE} spec from 6 ns to 10 ns Added footnote# 6 related to I_{SB2} and I_{CCDR} Updated Ordering information table
*C	2428708	See ECN	VKN/PYRS	Corrected typo in the Ordering Information table
*D	2516494	See ECN	PYRS	Corrected ECN number
*E	2934396	06/03/10	VKN	Added footnote #19 related to chip enable Updated package diagram Updated template
*F	3110202	12/14/2010	PRAS	Updated Logic Block Diagram. Added Ordering Code Definitions.
*G	3121955	12/28/2010	SRIH	Updated the missing header and footer in Pg 12.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5