

# 8-Mbit (1M x 8) Static RAM

## Features

- Very high speed: 45 ns
  - Wide voltage range: 4.5V – 5.5V
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
  - Typical active current: 18 mA at f = f<sub>max</sub>
- Ultra low standby power
  - Typical standby current: 2 μA
  - Maximum standby current: 8 μA
- Easy memory expansion with  $\overline{CE}_1$ , CE<sub>2</sub> and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 44-Pin TSOP II package

## Functional Description

The CY62158E MoBL<sup>®</sup> is a high performance CMOS static RAM organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This

is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption significantly when deselected (CE<sub>1</sub> HIGH or CE<sub>2</sub> LOW).

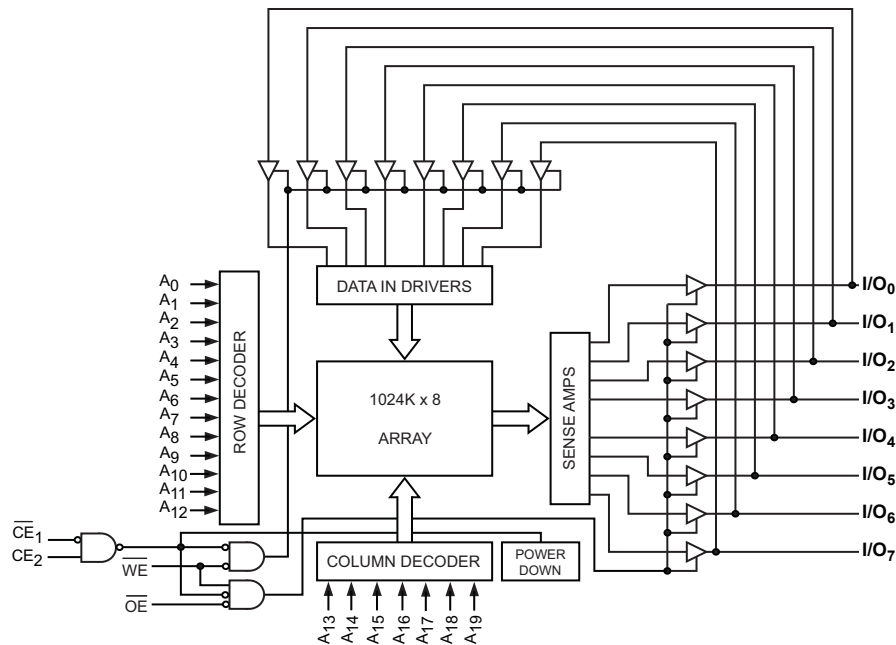
To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and CE<sub>2</sub> HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and CE<sub>2</sub> HIGH) and  $\overline{OE}$  LOW while forcing the  $\overline{WE}$  HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or CE<sub>2</sub> LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress (CE<sub>1</sub> LOW and CE<sub>2</sub> HIGH and  $\overline{WE}$  LOW). See the Truth Table on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines

## Logic Block Diagram

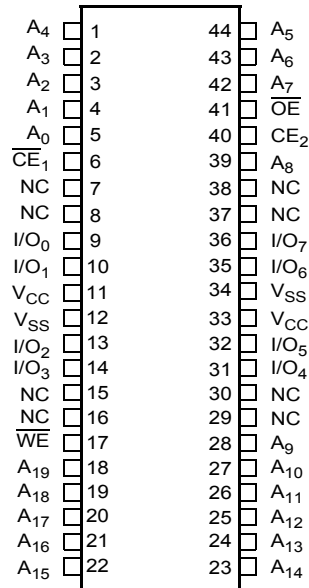


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## Pin Configuration

Figure 1. 44-Pin TSOP II (Top View)<sup>[1]</sup>



## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1 MHz		f = f <sub>max</sub>			
Min	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max		
CY62158ELL	4.5	5.0	5.5	45	1.8	3	18	25	2	8

### Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to $V_{CC(max)} + 0.5V$
DC Voltage Applied to Outputs in High-Z State <sup>[3, 4]</sup> .....	-0.5V to $V_{CC(max)} + 0.5V$

DC Input Voltage <sup>[3, 4]</sup> .....	-0.5V to $V_{CC(max)} + 0.5V$
Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage .....	>2001V (MIL-STD-883, Method 3015)
Latch up Current .....	>200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[5]</sup>
CY62158ELL	Industrial	-40°C to +85°C	4.5V – 5.5V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-45			Unit
			Min	Typ <sup>[2]</sup>	Max	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -1 \text{ mA}$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$			0.4	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = 4.5V \text{ to } 5.5V$	2.2		$V_{CC} + 0.5V$	V
$V_{IL}$	Input LOW Voltage	$V_{CC} = 4.5V \text{ to } 5.5V$	-0.5		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$		18	25	mA
		$f = 1 \text{ MHz}$	$V_{CC} = V_{CCmax}$ $I_{OUT} = 0 \text{ mA}$ CMOS levels	1.8	3	mA
$I_{SB1}$	Automatic CE Power down Current — CMOS Inputs	$CE_1 \geq V_{CC} - 0.2V$ , $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, and WE), $V_{CC} = V_{CCmax}$		2	8	$\mu\text{A}$
$I_{SB2}$ <sup>[6]</sup>	Automatic CE Power-down Current — CMOS Inputs	$CE_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = V_{CCmax}$		2	8	$\mu\text{A}$

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ ,	10	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = V_{CC(typ)}$	10	pF

## Thermal Resistance

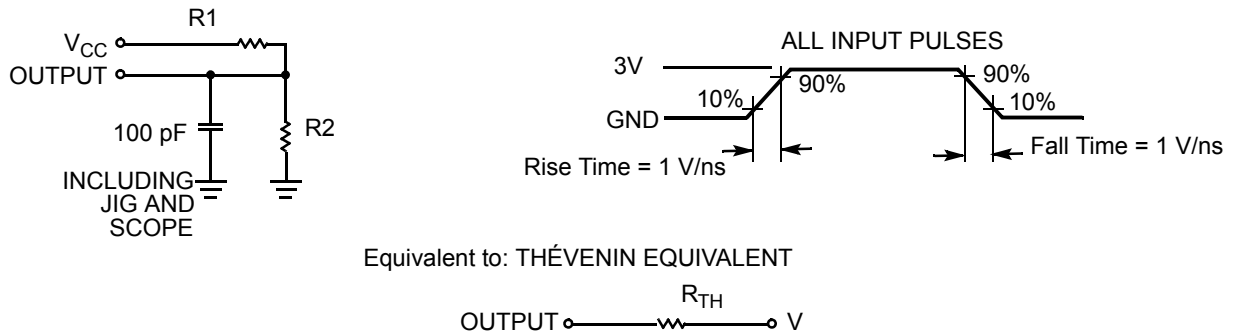
Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75.13	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		8.95	$^\circ\text{C/W}$

### Notes

- $V_{IL(min)}$  = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75V$  for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100  $\mu\text{s}$  ramp time from 0 to  $V_{CC}$  (min) and 200  $\mu\text{s}$  wait time after  $V_{CC}$  stabilization.
- Chip enables ( $CE_1$  and  $CE_2$ ), must be tied to CMOS levels to meet the  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.

Figure 2. AC Test Loads and Waveforms



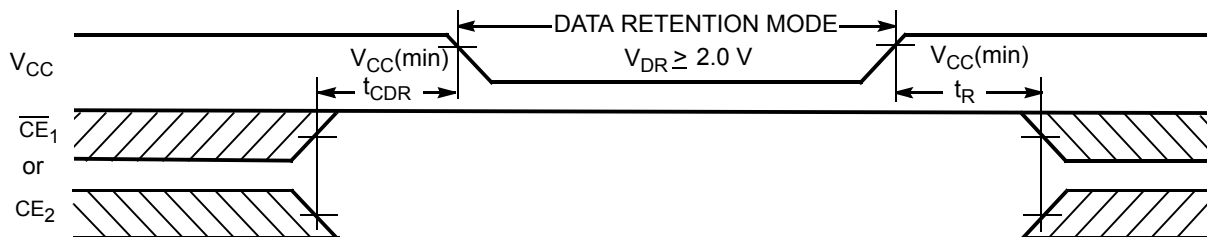
Parameters	5.0V	Unit
R1	1838	Ω
R2	994	Ω
R <sub>TH</sub>	645	Ω
V <sub>TH</sub>	1.75	V

### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[7]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2			V
I <sub>CCDR</sub> <sup>[8]</sup>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V			8	μA
t <sub>CDR</sub> <sup>[9]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[10]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

Figure 3. Data Retention Waveform



**Notes**

- 7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- 8. Chip enables (CE<sub>1</sub> and CE<sub>2</sub>), must be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.
- 9. Tested initially and after any design or process changes that may affect these parameters.
- 10. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

**Switching Characteristics**

 Over the Operating Range <sup>[11]</sup>

Parameter	Description	45 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	45		ns
$t_{AA}$	Address to Data Valid		45	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[12]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[12, 13]</sup>		18	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z <sup>[12]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to High Z <sup>[12, 13]</sup>		18	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up	0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to Power Down		45	ns
<b>Write Cycle <sup>[14]</sup></b>				
$t_{WC}$	Write Cycle Time	45		ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	35		ns
$t_{AW}$	Address Setup to Write End	35		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Setup to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		ns
$t_{SD}$	Data Setup to Write End	25		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[12, 13]</sup>		18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[12]</sup>	10		ns

**Notes**

11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in "AC Test Loads and Waveforms" on page 5.
12. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
13.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
14. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

Figure 4 shows address transition controlled read cycle waveforms.<sup>[15, 16]</sup>

Figure 4. Read Cycle No. 1

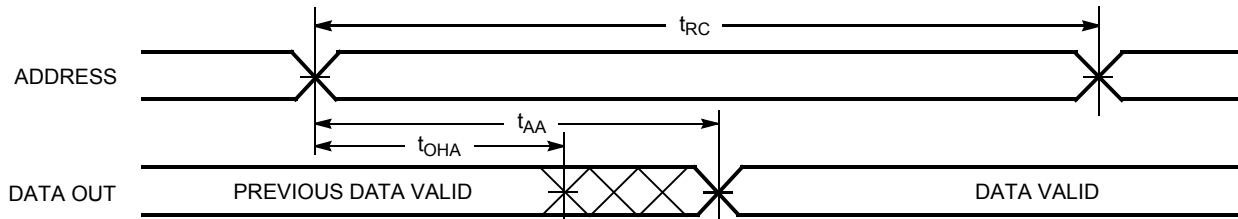
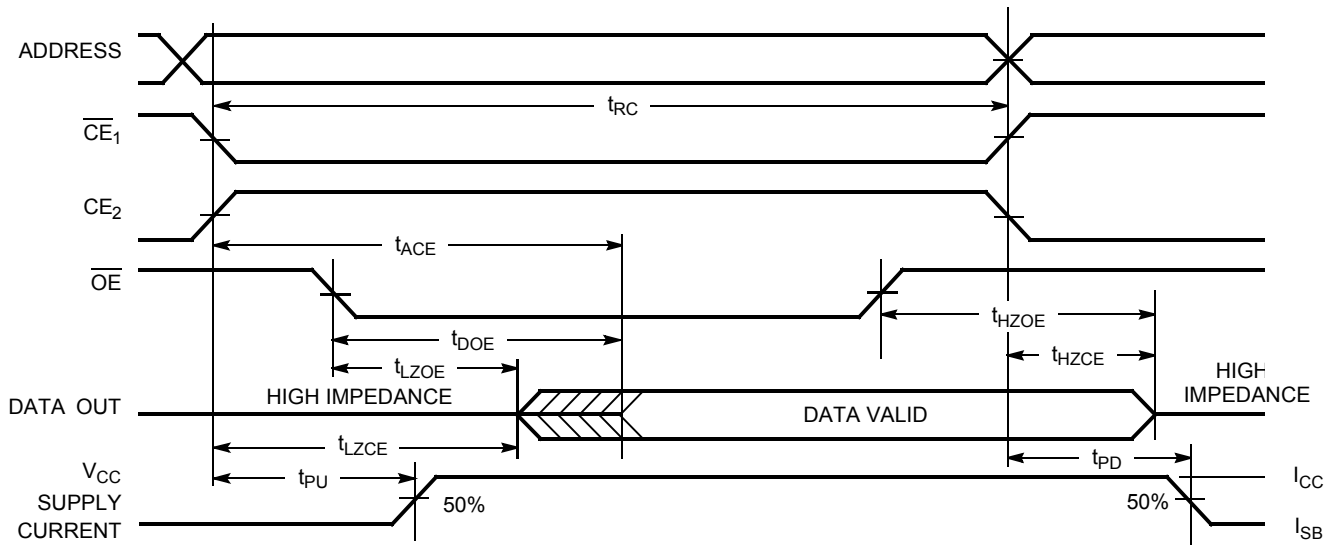


Figure 5 shows  $\overline{OE}$  controlled read cycle waveforms.<sup>[16, 17]</sup>

Figure 5. Read Cycle No. 2



### Notes

15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
16.  $\overline{WE}$  is HIGH for read cycle.
17. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 6 shows  $\overline{WE}$  controlled write cycle waveforms.<sup>[18, 19, 20]</sup>

Figure 6. Write Cycle No. 1

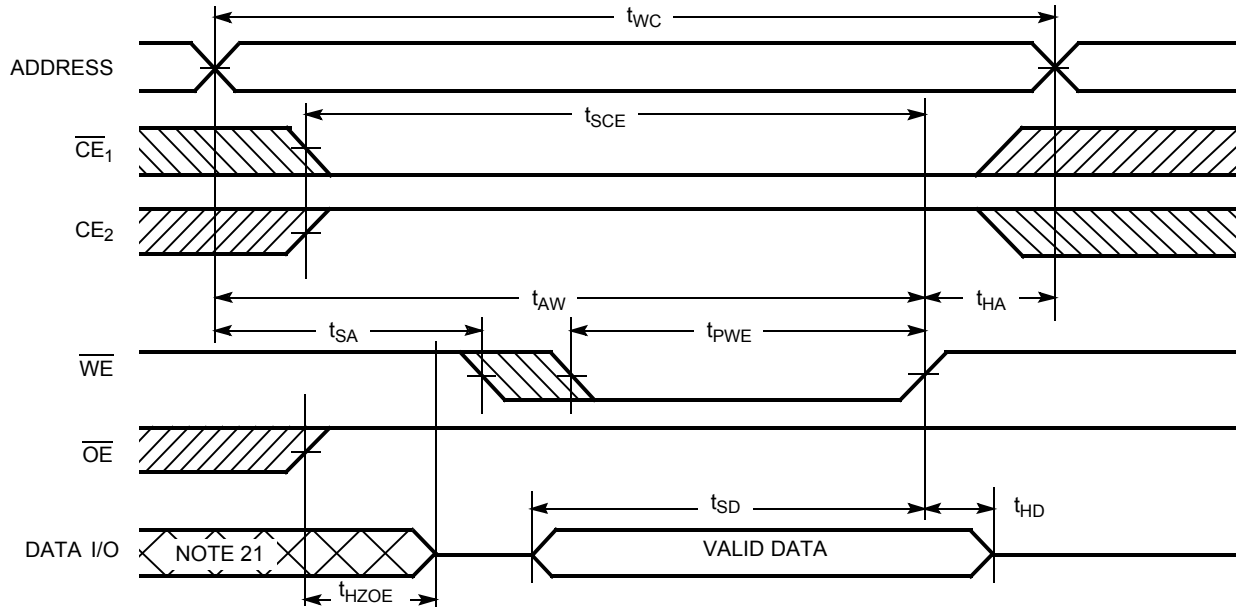
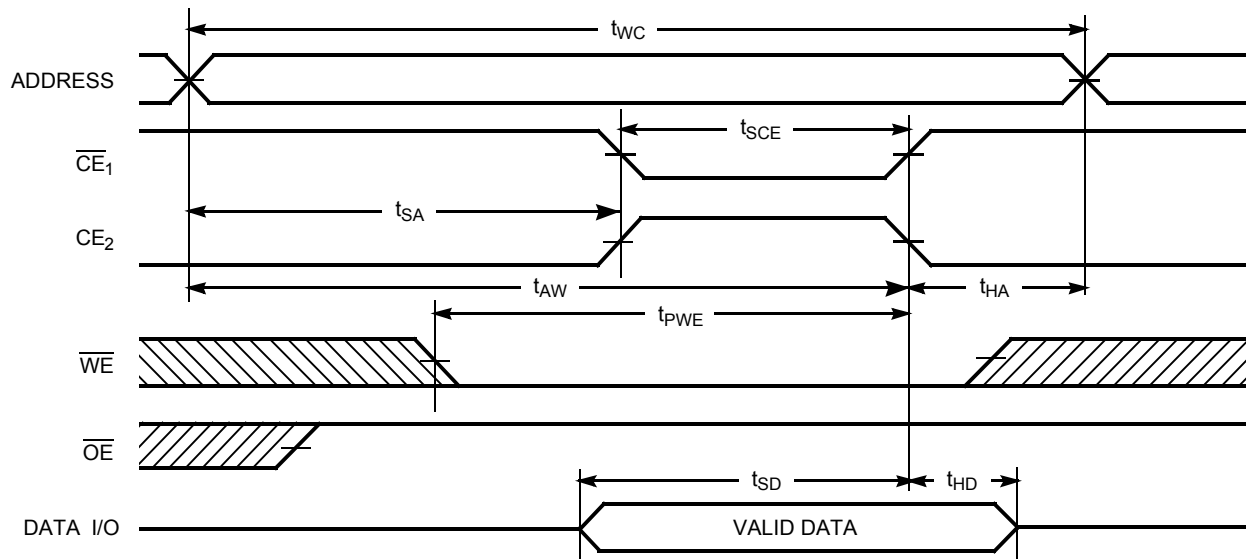


Figure 7 shows  $\overline{CE}_1$  or  $CE_2$  controlled write cycle waveforms.<sup>[18, 19, 20]</sup>

Figure 7. Write Cycle No. 2



Notes

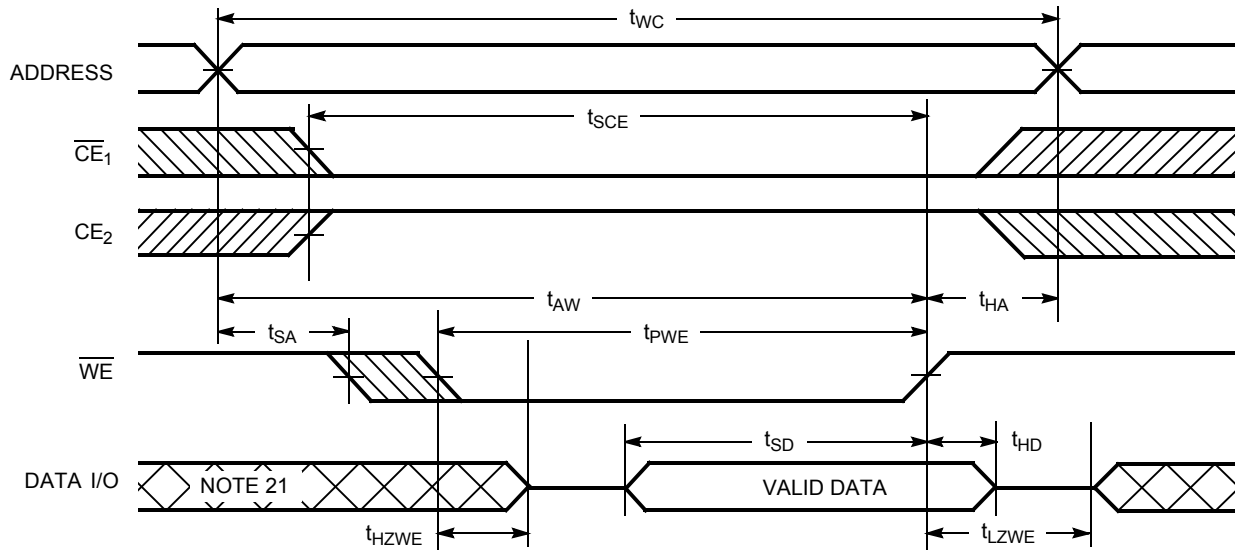
- 18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 19. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 20. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 21. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 8 shows  $\overline{WE}$  controlled,  $\overline{OE}$  LOW write cycle waveforms.<sup>[20]</sup>

Figure 8. Write Cycle No. 3



Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X <sup>[22]</sup>	X	X	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X <sup>[22]</sup>	L	X	X	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	H	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	H	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	Data in	Write	Active ( $I_{CC}$ )

Note

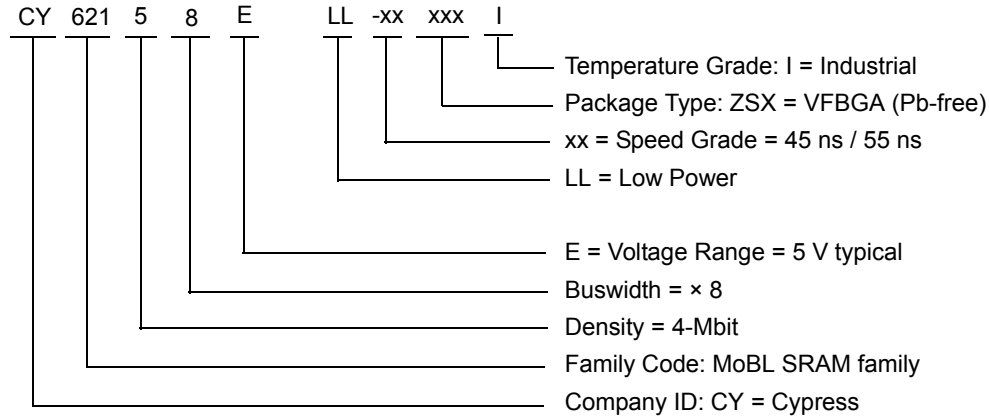
22. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62158ELL-45ZSXI	51-85087	44-Pin TSOP II (Pb-free)	Industrial

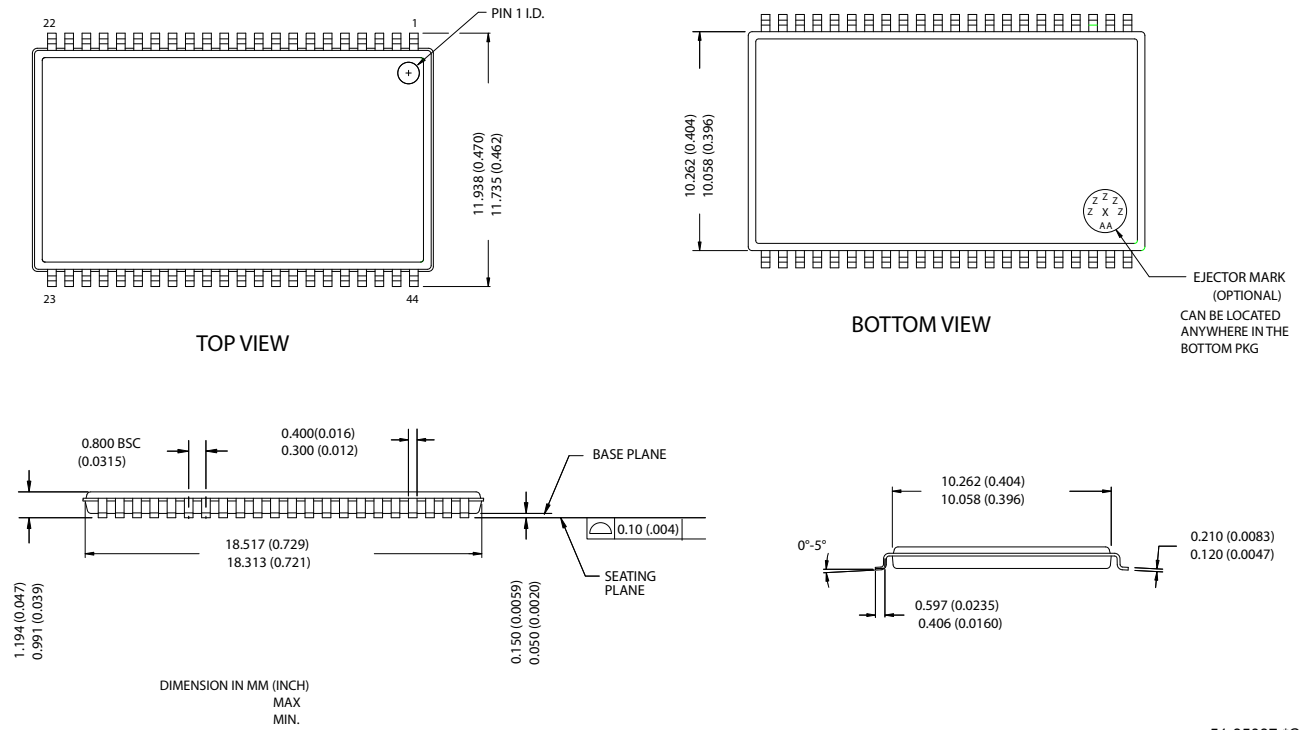
Contact your local Cypress sales representative for availability of this part.

## Ordering Code Definitions



Package Diagrams

Figure 9. 44-Pin TSOP II, 51-85087



51-85087-\*C

**Document History Page**

Document Title: CY62158E MoBL <sup>®</sup> 8-Mbit (1M x 8) Static RAM Document Number: 38-05684				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	270350	See ECN	PCI	New Data Sheet
*A	291271	See ECN	SYT	Converted from Advance Information to Preliminary Changed input pulse level from $V_{CC}$ to 3V in the AC Test Loads and Waveforms Modified footnote #9 to include timing reference level of 1.5V and input pulse level of 3V
*B	1462592	See ECN	VKN/AESA	Converted from preliminary to final Removed 35 ns speed bin Removed "L" parts Removed 48-Ball VFBGA package Changed $I_{CC(max)}$ spec from 2.3 mA to 3 mA at $f=1$ MHz Changed $I_{CC(typ)}$ spec from 16 mA to 18 mA at $f=f_{MAX}$ Changed $I_{CC(max)}$ spec from 28 mA to 25 mA at $f=f_{MAX}$ Changed $I_{SB1(typ)}$ and $I_{SB2(typ)}$ spec from 0.9 $\mu$ A to 2 $\mu$ A Changed $I_{SB1(max)}$ and $I_{SB2(max)}$ spec from 4.5 $\mu$ A to 8 $\mu$ A Changed $I_{CCDR(max)}$ spec from 4.5 $\mu$ A to 8 $\mu$ A Changed $t_{LZOE}$ spec from 3 ns to 5 ns Changed $t_{LZCE}$ spec from 6 ns to 10 ns Changed $t_{HZCE}$ spec from 22 ns to 18 ns Changed $t_{PWE}$ spec from 30 ns to 35 ns Changed $t_{SD}$ spec from 22 ns to 25 ns Changed $t_{LZWE}$ spec from 6 ns to 10 ns Added footnote# 6 related to $I_{SB2}$ and $I_{CCDR}$ Updated Ordering information table
*C	2428708	See ECN	VKN/PYRS	Corrected typo in the Ordering Information table
*D	2516494	See ECN	PYRS	Corrected ECN number
*E	2934396	06/03/10	VKN	Added footnote #19 related to chip enable Updated package diagram Updated template
*F	3110202	12/14/2010	PRAS	Updated Logic Block Diagram. Added Ordering Code Definitions.
*G	3121955	12/28/2010	SRIH	Updated the missing header and footer in Pg 12.

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