

# 16-Mbit (1M x 16) Static RAM

#### **Features**

- Thin small outline package (TSOP I) Configurable as 1M x 16 or as 2M x 8 SRAM
- Wide voltage range: 2.2 V 3.6 V
- Ultra-low active power: Typical active current: 2 mA at f = 1 MHz
- Ultra-low standby power
- Easy memory expansion with <del>CE</del><sub>1</sub>, CE<sub>2</sub> and <del>OE</del> features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed / power
- Available in Pb-free and non Pb-free 48-ball very fine ball grid array (VFBGA) and 48-pin TSOP I package

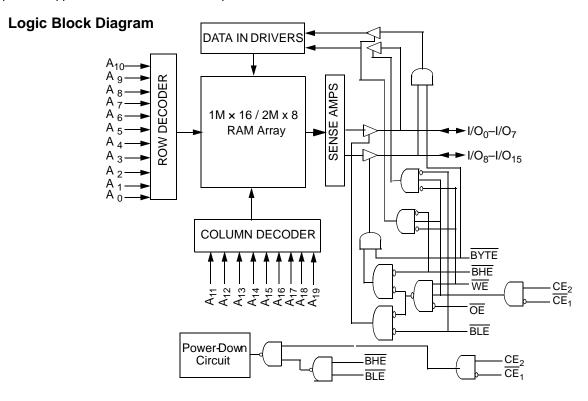
#### Functional Description[1]

The CY62167DV30 is a high-performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life<sup>™</sup> (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device

also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{\text{CE}}_1$  HIGH or  $\text{CE}_2$  LOW or both BHE and BLE are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}_1$  HIGH or  $\text{CE}_2$  LOW), outputs are disabled ( $\overline{\text{OE}}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a Write operation ( $\overline{\text{CE}}_1$  LOW,  $\text{CE}_2$  HIGH and  $\overline{\text{WE}}$  LOW).

Writing to the device is accomplished by taking Chip Enables ( $\overline{\text{CE}}_1$  LOW and  $\text{CE}_2$  <u>HIG</u>H) and Write Enable ( $\overline{\text{WE}}$ ) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified <u>on</u> the address pins (A<sub>0</sub> through A<sub>19</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

Reading from the device is accomplished by taking Chip Enables ( $CE_1$  LOW and  $CE_2$  HIGH) and Output Enable (OE) LOW while forcing the Write Enable (OE) HIGH. If Byte Low Enable (OE) is LOW, then data from the memory location specified by the address pins will appear on I/O0 to I/O7. If Byte High Enable (OE) is LOW, then data from memory will appear on I/O8 to I/O15. See the truth table at the back of this data sheet for a complete description of Read and Write modes.



#### Note

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Cypress Semiconductor Corporation
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### **Contents**

Product Portfolio	3
Pin Configuration	3
Maximum Ratings	4
Operating Range	
Electrical Characteristics	
Capacitance	5
Thermal Resistance	
AC Test Loads and Waveforms	5
Data Retention Characteristics	_
Data Retention Waveform	_
Switching Characteristics	

Switching waveforms	/
Truth Table	11
Ordering Information	12
Ordering Code Definition	12
Acronyms	15
Document Conventions	15
Units of Measure	15
Sales, Solutions, and Legal Information	17
Worldwide Sales and Design Support	17
Products	17
PSoC Solutions	17

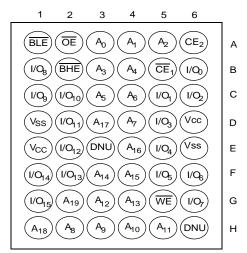


#### **Product Portfolio**

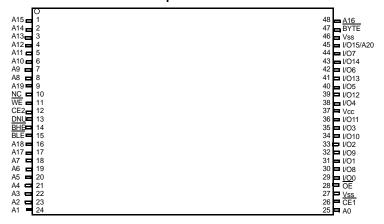
							Power D	issipatior	1	
V <sub>CC</sub> Range (V)		V)	Speed	Operating I <sub>CC</sub> (mA)			Standby I (A)			
Product			(ns)	f = 1MHz		f = f <sub>Max</sub>		Standby I <sub>SB2</sub> (μA)		
	Min	<b>Typ</b> <sup>[2]</sup>	Max		<b>Typ</b> <sup>[2]</sup>	Max	<b>Typ</b> <sup>[2]</sup>	Max	<b>Typ</b> <sup>[2]</sup>	Max
CY62167DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22
				70			12	25		

## **Pin Configuration**

Figure 1. 48- ball VFBGA Top View[3, 4, 5]



48-Pin TSOP I (Forward) (1M x 16/ 2M x 8)<sup>[6]</sup> **Top View** 



- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25 °C.
- NC pins are not connected on the die.
- DNU pins have to be left floating.
- Ball H6 for the FBGA package can be used to upgrade to a 32M density.

  The BYTE pin in the 48-TSOP I package has to be tied to V<sub>CC</sub> to use the device as a 1M X 16 SRAM. The 48-TSOPI package can also be used as a 2M X 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 2M x 8 configuration, Pin 45 is A20, while BHE, BLE and I/O8 to I/O14 pins are not used (DNU).

Document Number: 38-05328 Rev. \*I Page 3 of 17



#### **Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.) Storage temperature ......-65 °C to +150 °C Ambient temperature with power applied ...... -55 °C to +125 °C Supply voltage to ground potential ..... -0.2 V to  $V_{CC}$  + 0.3 V DC voltage applied to outputs in High-Z state  $^{[7, 8]}$  ...... –0.2 V to V<sub>CC</sub> + 0.3 V DC input voltage<sup>[7, 8]</sup>.....-0.2 V to  $V_{CC}$  + 0.3 V

Output current into outputs (LOW)	20 mA
Static discharge voltage(per MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 200 mA

### **Operating Range**

Device Range		Ambient Temperature	<b>V</b> CC <sup>[9]</sup>
CY62167DV30LL	Industrial	–40 °C to +85 °C	2.20 V to 3.60 V

### **Electrical Characteristics** Over the Operating Range

	<b>D</b>	T 0	Pet	CY6	2167DV	30-55	CY62167DV30-70			Unit
Parameter	Description	lest Con	Test Conditions		<b>Typ</b> [10]	Max	Min	<b>Typ</b> <sup>[10]</sup>	Typ <sup>[10]</sup> Max	
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> = 2.20 V	2.0	-	_	2.0	-	-	V
		I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.70 V	2.4			2.4			
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = 2.20 V	_	_	0.4		_	0.4	V
		I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.70 V							
V <sub>IH</sub>	Input HIGH voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$	,	1.8	_	V <sub>CC</sub>	1.8	_	V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.7 V to 3.6 V		2.2		+0.3 V	2.2		+0.3V	
V <sub>IL</sub>	Input LOW voltage	V <sub>CC</sub> = 2.2 V to 2.7 V	,	-0.3	_	0.6	-0.3	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V				0.8			0.8	
I <sub>IX</sub>	Input leakage current	$GND \le V_1 \le V_{CC}$		-1	_	+1	-1	-	+1	μΑ
I <sub>OZ</sub>	Output leakage current	$GND \le V_O \le V_{CC}, OU$	tput Disabled	-1	-	+1	-1	_	+1	μА
I <sub>CC</sub>	V <sub>CC</sub> Operating	$V_{CC} = V_{CC(max)}$	$f = f_{Max} = 1/t_{RC}$	_	15	30	_	12	25	mA
	supply current	I <sub>OUT</sub> = 0 mA CMOS levels	f = 1 MHz		2	4		2	4	
I <sub>SB1</sub>	Automatic Power-down current — CMOS inputs	$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V or } \text{CE}_2 \le 0.2 \text{ V},$ $\text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V}, \text{V}_{\text{IN}} \le 0.2 \text{ V},$ $\text{f} = \text{f}_{\text{Max}} \text{ (Address and data only)},$ $\text{f} = 0 \text{ (OE, WE), V}_{\text{CC}} = 3.60 \text{ V}$		-	2.5	22	-	2.5	22	μА
I <sub>SB2</sub>	Automatic Power-down current — CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2 \text{ V o}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V o}$ $f = 0, V_{CC} = 3.60 \text{ V}$	or $CE_2 \le 0.2 \text{ V}$ $V_{\text{IN}} \le 0.2 \text{V}$ ,	_	2.5	22	_	2.5	22	μА

- N<sub>IL(min.)</sub> = -2.0 V for pulse durations less than 20 ns.
   V<sub>IL(min.)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
   Full Device AC operation requires linear V<sub>CC</sub> ramp from 0 to V<sub>CC(min.)</sub> and V<sub>CC</sub> must be stable at V<sub>CC(min)</sub> for 500 μs.
   Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C

Document Number: 38-05328 Rev. \*I Page 4 of 17



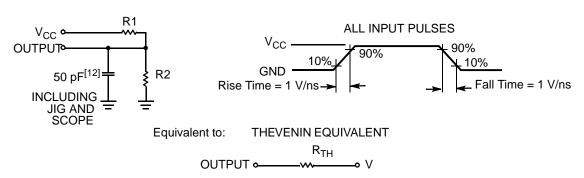
#### Capacitance

Parameter <sup>[11]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25$ °C, $f = 1$ MHz, $V_{CC} = V_{CC(typ)}$	8	pF
C <sub>OUT</sub>	Output capacitance		10	pF

#### **Thermal Resistance**

Parameter <sup>[11]</sup>	Description	Test Conditions	VFBGA	TSOP I	Unit
$\Theta_{JA}$		Still Air, soldered on a 3 x 4.5 inch, 2-layer printed circuit board	55	60	°C/W
$\Theta_{\sf JC}$	Thermal resistance (Junction to case)		16	4.3	°C/W

#### **AC Test Loads and Waveforms**



Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

#### Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Cone	ditions	Min	<b>Typ</b> <sup>[12]</sup>	Max	Unit
$V_{DR}$	V <sub>CC</sub> for Data retention			1.5	_	_	V
I <sub>CCDR</sub>	Data retention current	$V_{CC} = 1.5 \text{ V},$ $CE_1 \ge V_{CC} - 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V or}$	r CE <sub>2</sub> ≤ 0.2 V, r V <sub>IN</sub> ≤ 0.2 V	_	_	10	μΑ
t <sub>CDR</sub> <sup>[11]</sup>	Chip deselect to data retention time			0	_	_	ns
t <sub>R</sub> <sup>[13]</sup>	Operation recovery time		CY62167DV30LL-55	55	_	_	ns
			CY62167DV30LL-70	70			

- 11. Tested initially and after any design or process changes that may affect these parameters.

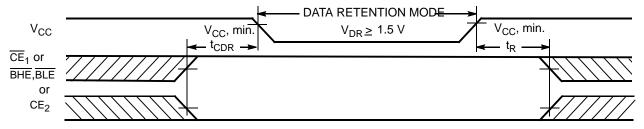
  12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C

  13. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 100 µs or stable at V<sub>CC(min.)</sub> ≥ 100 µs.

Document Number: 38-05328 Rev. \*I Page 5 of 17



#### Data Retention Waveform[14]



#### Switching Characteristics Over the Operating Range

Dava (15)	Description	55	ns	70	ns	l lmi4
Parameter <sup>[15]</sup>	Description	Min	Max	Min	Max	Unit
Read Cycle		<u>'</u>				
t <sub>RC</sub>	Read cycle time	55	_	70	_	ns
t <sub>AA</sub>	Address to data valid	_	55	_	70	ns
t <sub>OHA</sub>	Data hold from address change	10	_	10	_	ns
t <sub>ACE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to data valid	_	55	_	70	ns
t <sub>DOE</sub>	OE LOW to data valid	_	25	_	35	ns
t <sub>LZOE</sub>	OE LOW to LOW Z <sup>[16]</sup>	5	_	5	_	ns
t <sub>HZOE</sub>	OE HIGH to High Z[16, 17]	_	20	_	25	ns
t <sub>LZCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Low Z <sup>[16]</sup>	10	_	10	_	ns
t <sub>HZCE</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to High Z <sup>[16, 17]</sup>	_	20	_	25	ns
t <sub>PU</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Power-up	0	_	0	_	ns
t <sub>PD</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to Power-down	_	55	_	70	ns
t <sub>DBE</sub>	BLE/BHE LOW to data valid	_	55	_	70	ns
t <sub>LZBE</sub>	BLE/BHE LOW to Low Z <sup>[16]</sup>	10	_	10	_	ns
t <sub>HZBE</sub>	BLE/BHE HIGH to HIGH Z <sup>[16, 17]</sup>	_	20	_	25	ns
Write Cycle <sup>[18]</sup>			•	•	•	
t <sub>WC</sub>	Write cycle time	55	_	70	_	ns
t <sub>SCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to write end	40	_	60	_	ns
t <sub>AW</sub>	Address set-up to write end	40	_	60	_	ns
t <sub>HA</sub>	Address hold from write end	0	_	0	_	ns
t <sub>SA</sub>	Address set-up to write start	0	_	0	_	ns
t <sub>PWE</sub>	WE pulse width	40	-	45	-	ns
t <sub>BW</sub>	BLE/BHE LOW to write end	40	_	60	-	ns
t <sub>SD</sub>	Data set-up to write end	25	_	30	_	ns
t <sub>HD</sub>	Data hold from write end	0	_	0	-	ns
t <sub>HZWE</sub>	WE LOW to High-Z <sup>[16, 17]</sup>	_	20	_	25	ns
t <sub>LZWE</sub>	WE HIGH to Low-Z <sup>[16]</sup>	10	_	10	_	ns

Document Number: 38-05328 Rev. \*I Page 6 of 17

Notes
14. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

15. Test conditions for all parameters other than Tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0 to V<sub>CC(typ.)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in the "AC Test Loads and Waveforms" section.

16. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZDE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> for any given device

<sup>17.</sup> t<sub>HZOE</sub>, t<sub>HZEE</sub>, and t<sub>HZWE</sub> transitions are measured when the outp<u>uts enter</u> a high impedance state.

18. The internal Write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.



### **Switching Waveforms**

Figure 2. Read Cycle 1 (Address Transition Controlled)[19, 20]

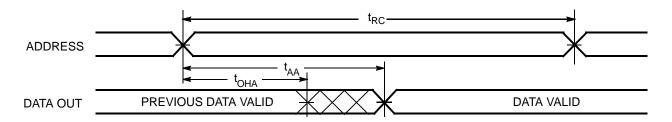
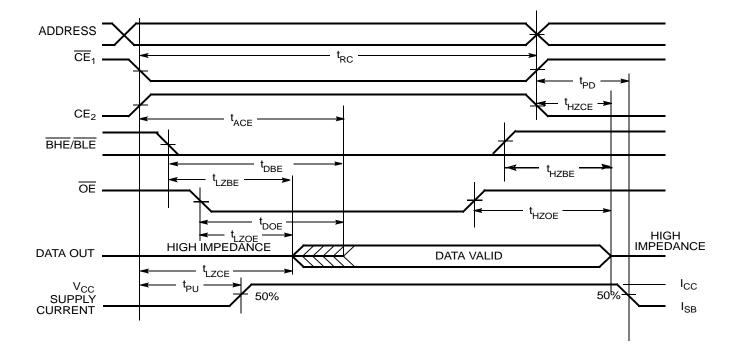


Figure 3. Read Cycle 2 (OE Controlled)[20, 21]



<sup>19.</sup> The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $\overline{CE}_2 = V_{IH}$ .

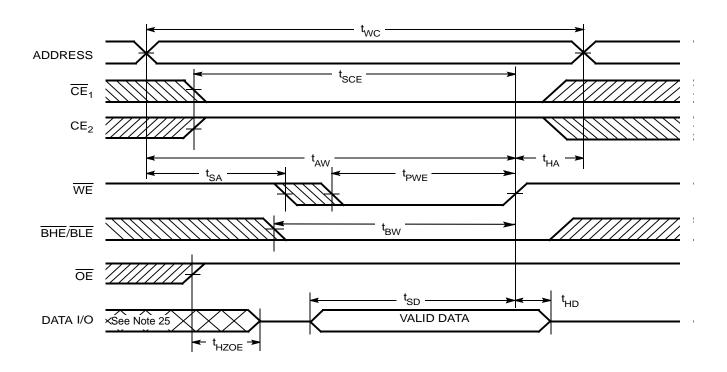
<sup>20.</sup> WE is HIGH for read cycle.

21. Address valid prior to or coincident with  $\overline{\text{CE}}_1$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW and  $\overline{\text{CE}}_2$  transition HIGH.



### Switching Waveforms (continued)

Figure 4. Write Cycle 1 (WE Controlled)[22, 23, 24]



#### Notes

<sup>22.</sup> The internal Write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

that terminates the write.

23. Data |/O is high-impedance if  $\overline{OE} = V_{IH}$ .

24. If  $\overline{CE}_1$  goes HIGH and  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.

25. During this period, the I/Os are in output state and input signals should not be applied.



#### Switching Waveforms (continued)

Figure 5. Write Cycle 2 (CE<sub>1</sub> or CE<sub>2</sub> Controlled)<sup>[26, 27, 28]</sup>

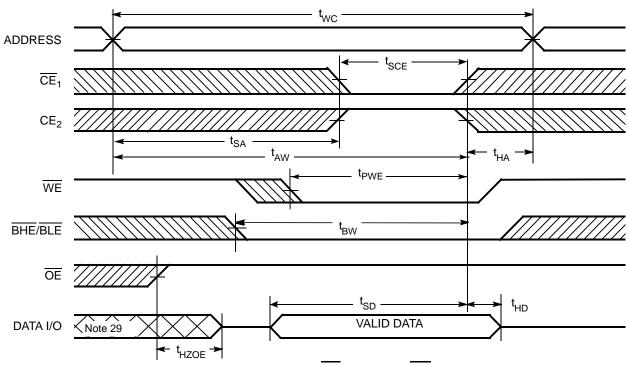
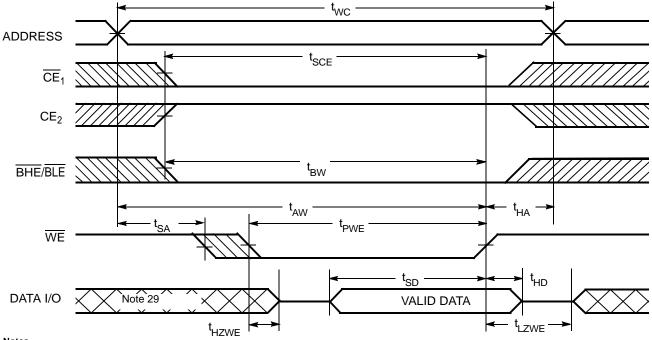


Figure 6. Write Cycle 3 (WE Controlled, OE LOW)[28]



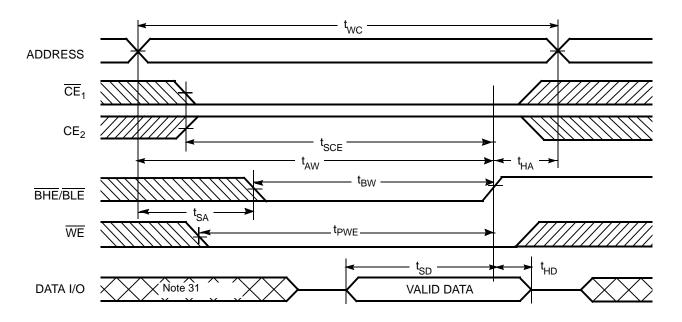
#### Notes

- 26. The internal Write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.
- 27. Data I/O is high-impedance if  $\overline{\text{OE}} = \text{V}_{\text{IH}}$ 28. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}} = \text{V}_{\text{IH}}$ , the output remains in a high-impedance state.
- 29. During this period, the I/Os are in output state and input signals should not be applied.



## Switching Waveforms (continued)

Figure 7. Write Cycle 4 (BHE/BLE Controlled, OE LOW)[30]



Document Number: 38-05328 Rev. \*I

Notes 30. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}} = \text{V}_{\text{IH}}$ , the output remains in a high-impedance state 31. During this period, the I/Os are in output state and input signals should not be applied.



## **Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	WE	ŌĒ	BHE	BLE	Inputs/Outputs	Mode	Power
Н	Х	Х	Х	Х	Х	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
Х	L	Х	Х	Х	Х	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
Х	Х	X	Х	Н	Н	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
L	Н	Η	L	L	L	Data out (I/O <sub>0</sub> -I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	L	Н	L	High Z (I/O <sub>8</sub> –I/O <sub>15</sub> ); Data out (I/O <sub>0</sub> –I/O <sub>7</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	L	L	Н	Data out (I/O <sub>8</sub> –I/O <sub>15</sub> ); High Z (I/O <sub>0</sub> –I/O <sub>7</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	L	Х	L	L	Data in (I/O <sub>0</sub> -I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	L	Х	Н	L	High Z (I/O <sub>8</sub> –I/O <sub>15</sub> ); Data in (I/O <sub>0</sub> –I/O <sub>7</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	L	Х	L	Н	Data in (I/O <sub>8</sub> -I/O <sub>15</sub> ); High Z (I/O <sub>0</sub> -I/O <sub>7</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	Н	Н	L	Н	High Z	Output disabled	Active (I <sub>CC</sub> )
L	Н	Н	Н	Н	L	High Z	Output disabled	Active (I <sub>CC</sub> )
L	Н	Н	Н	L	L	High Z	Output disabled	Active (I <sub>CC</sub> )

Document Number : 38-05328 Rev. \*I

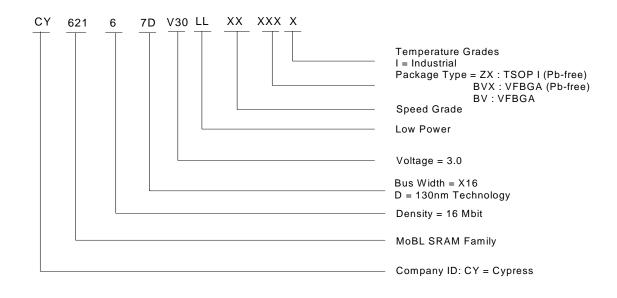


## **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167DV30LL-55BVI	51-85178	48-ball Fine Pitch BGA (8 x 9.5 x 1 mm)	Industrial
	CY62167DV30LL-55BVXI		48-ball Fine Pitch BGA (8 x 9.5 x 1 mm) (Pb-free)	
	CY62167DV30LL-55ZXI	51-85183	48-pin TSOP I (12 x 18.4 x 1 mm) (Pb-free)	
70	CY62167DV30LL-70BVI	51-85178	48-ball Fine Pitch BGA (8 x 9.5 x 1 mm)	

Please contact your local Cypress sales representative for availability of these parts

#### **Ordering Code Definition**

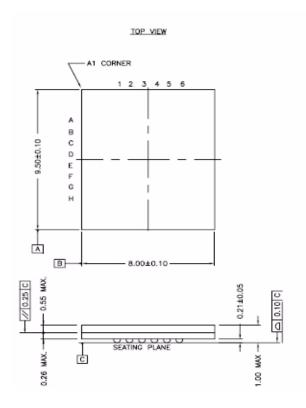


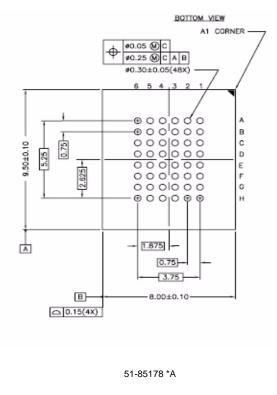
Document Number : 38-05328 Rev. \*I Page 12 of 17



## **Package Diagrams**

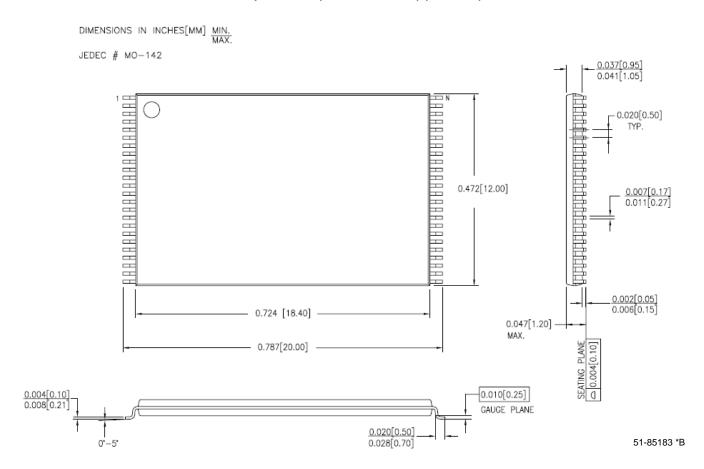
#### 48-ball VFBGA (8 x 9.5 x 1 mm) (51-85178)







#### 48-pin TSOP I (12 x 18.4 x 1 mm) (51-85183)



Document Number : 38-05328 Rev. \*I



## **Acronyms**

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball grid array
TSOP	thin small outline package

## **Document Conventions**

#### **Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
μΑ	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document Number : 38-05328 Rev. \*I



## **Document History Page**

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change	
**	118408	09/30/02	GUG	New Data Sheet	
*A	123692	02/11/03	DPM	Changed Advanced to Preliminary Added package diagram	
*B	126555	04/25/03	DPM	Minor change: Changed Sunset Owner from DPM to HRT	
*C	127841	09/10/03	XRJ	Added 48 TSOP I package	
*D	205701		AJU	Changed BYTE pin usage description for 48 TSOPI package	
*E	238050	See ECN	KKV/AJU	J Replaced 48-ball VFBGA package diagram; Modified Package Nam Ordering Information table from BV48A to BV48B	
*F	304054	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #12 on page #4 Added Pb-free packages on page # 10	
*G	492895	See ECN	VKN	Modified datasheet to explain x8 configurability Removed L power bin from the product offering Updated Ordering Information Table	
*H	2896036	03/19/2010	AJU	Removed 45-ns. Removed inactive parts from Ordering Information. Updated Packaging Information Updated links in Sales, Solutions, and Legal Information.	
*	3067267	11/08/2010	RAME	Updated datasheet as per new template Added Ordering Code Definition, Acronyms and Units of Measure. Updated all tablenotes to footnote. Package diagram updated 51-85178 from ** to *A	

Document Number : 38-05328 Rev. \*I Page 16 of 17



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Document Number: 38-05328 Rev. \*I Revised November 8, 2010 Page 17 of 17

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