CY62157EV30 MoBL®

8 Mbit (512K x 16) Static RAM

Features

- Thin small outline package (TSOP) I package configurable as 512K x 16 or 1M x 8 static RAM (SRAM)
- High speed: 45 ns
- Temperature ranges
  - Industrial: –40°C to +85°C
  - Automotive-A: –40°C to +85°C
  - Automotive-E: –40°C to +125°C
- Wide voltage range: 2.20V to 3.60V
- Pin compatible with CY62157DV30
- Ultra low standby power
  - Typical standby current: 2 µA
  - Maximum standby current: 8 µA (Industrial)
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary Metal Oxide Semiconductor (CMOS) for optimum speed and power
- Available in Pb-free and non Pb-free 48-Ball very fine ball grid array (VFBGA), Pb-free 44-Pin TSOP II and 48-Pin TSOP I packages

Functional Description

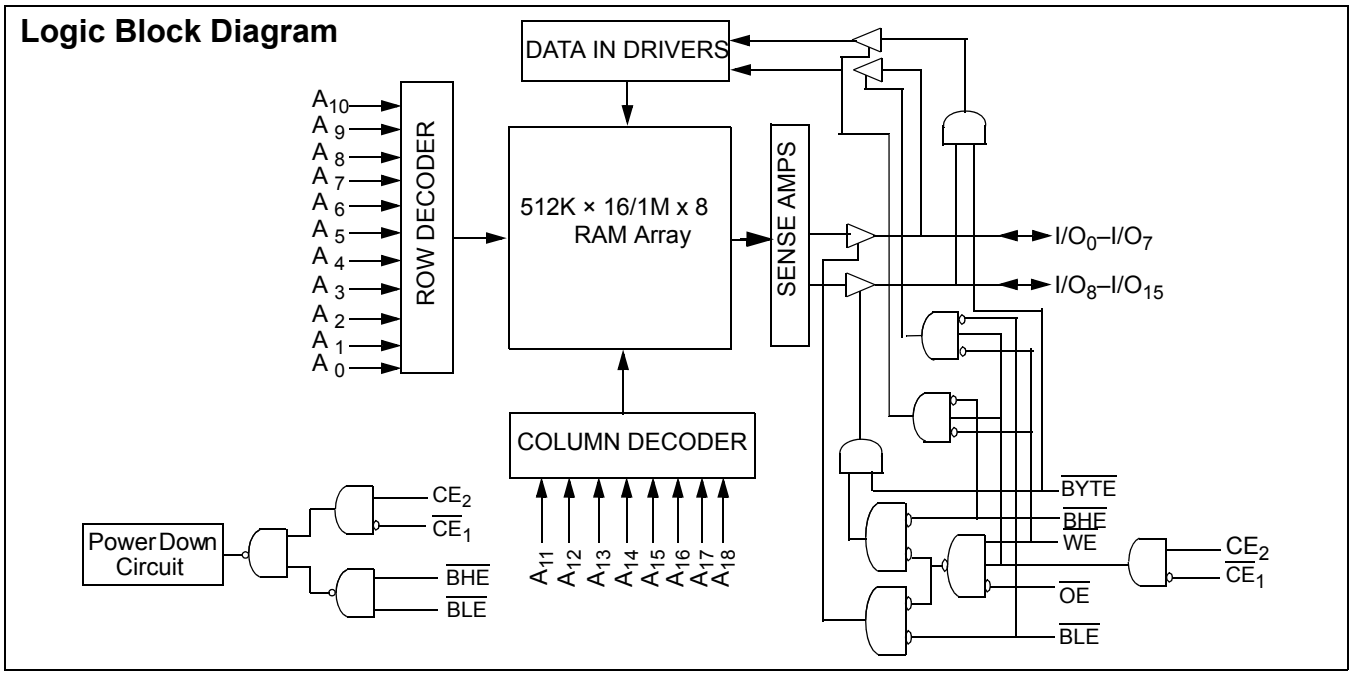
The CY62157EV30 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input or output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is active ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



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Contents

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Pin Configuration

Figure 1. 48-Ball VFBGA (Top View) [2]

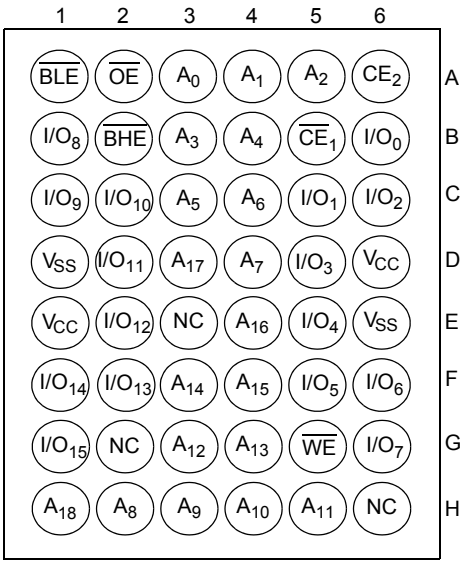


Figure 2. 44-Pin TSOP II (Top View) [3]

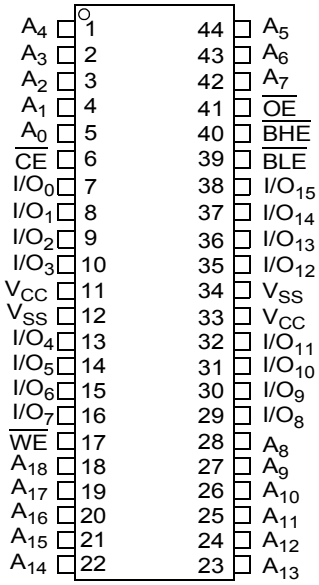
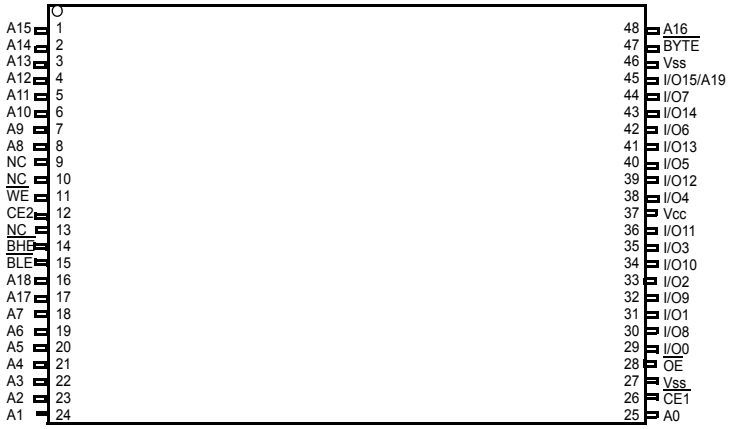


Figure 3. 48-Pin TSOP I (512K x 16/1M x 8) (Top View) [2, 4]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62157EV30LL	Industrial/ Auto-A	2.2	3.0	3.6	45	1.8	3	18	25	2	8
	Auto-E	2.2	3.0	3.6	55	1.8	4	18	35	2	30

Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.
2. NC pins are not connected on the die.
3. The 44-TSOP II package has only one chip enable ($\overline{CE}$) pin.
4. The BYTE pin in the 48-TSOP I package must be tied HIGH to use the device as a 512K × 16 SRAM. The 48-TSOP I package can also be used as a 1M × 8 SRAM by tying the BYTE signal LOW. In the 1M x 8 configuration, Pin 45 is A19, while BHE, BLE and I/O8 to I/O14 pins are not used (NC).

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Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.3V to 3.9V (V_{CCmax} + 0.3V)

DC Voltage Applied to Outputs in High-Z State [5, 6] ..... –0.3V to 3.9V (V_{CCmax} + 0.3V)

DC Input Voltage [5, 6] ..... –0.3V to 3.9V ($V_{CC\ max}$ + 0.3V)

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [7]
CY62157EV30LL	Industrial/ Auto-A	–40°C to +85°C	2.2V to 3.6V
	Auto-E	–40°C to +125°C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Ind'l/Auto-A)			55 ns (Auto-E)			Unit
			Min	Typ [8]	Max	Min	Typ [8]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	2.0			2.0			V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70V	2.4			2.4			V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA			0.4			0.4	V
		I_{OL} = 2.1mA, $V_{CC} \geq$ 2.70V			0.4			0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2V to 2.7V	1.8		V_{CC} + 0.3	1.8		V_{CC} + 0.3	V
		V_{CC} = 2.7V to 3.6V	2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2V to 2.7V	–0.3		0.6	–0.3		0.6	V
		V_{CC} = 2.7V to 3.6V	–0.3		0.8	–0.3		0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	–1		+1	–4		+4	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–1		+1	–4		+4	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$; V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels		18	25		18	35	mA
		f = 1 MHz; V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels		1.8	3		1.8	4	mA
I_{SB1}	Automatic CE power down current — CMOS inputs	$\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$ ($V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$) f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60V		2	8		2	30	µA
I_{SB2} [9]	Automatic CE power down current — CMOS inputs	$\overline{CE_1} \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, ($V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$), f = 0, V_{CC} = 3.60V		2	8		2	30	µA

Notes

5. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
7. Full device AC operation assumes a 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
9. Chip enables ($\overline{CE_1}$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ (48 TSOP I only) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

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Capacitance

Tested initially and after any design or process changes that may affect these parameters.

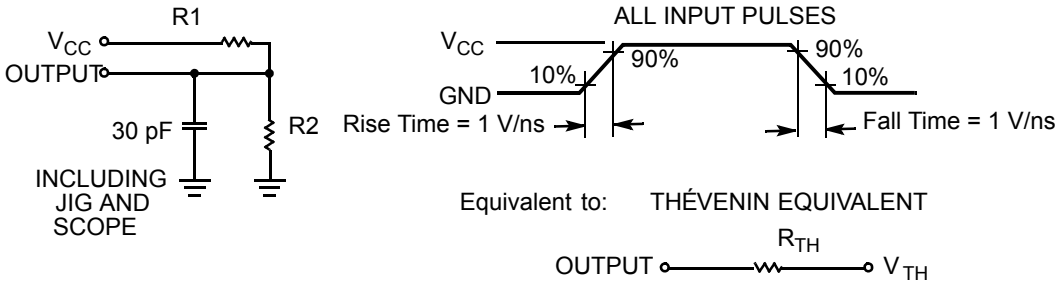
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	BGA	TSOP I	TSOP II	Unit
Θ_{JA}	Thermal resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	72	74.88	76.88	°C/W
Θ_{JC}	Thermal resistance (Junction to Case)		8.86	8.6	13.52	°C/W

Figure 4. AC Test Loads and Waveforms



Parameters	2.5V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

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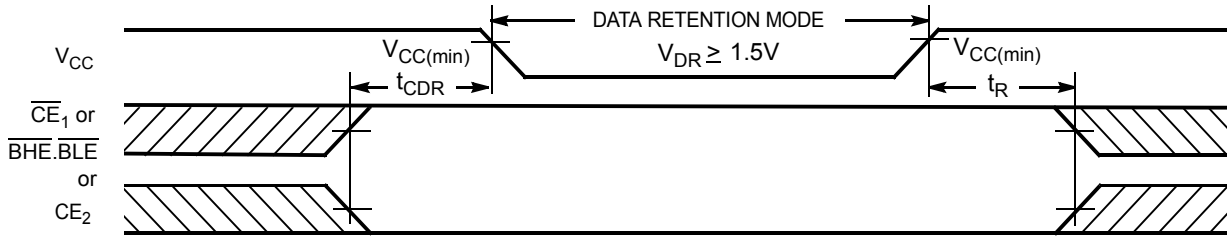
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5			V
I_{CCDR}	Data retention current	V_{CC}= 1.5V, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Industrial/ Auto-A		2	5	µA
			Auto-E			30	
t_{CDR} [11]	Chip deselect to data retention time			0			ns
t_R [12]	Operation recovery time			t_{RC}			ns

Data Retention Waveform

Figure 5. Data Retention Waveform [13]



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

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Switching Characteristics

Over the Operating Range[14, 15]

Parameter	Description	45 ns (Ind'l/Auto-A)		55 ns (Auto-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45		55		ns
t_{AA}	Address to data valid		45		55	ns
t_{OHA}	Data hold from address change	10		10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid		22		25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW-Z[16]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[16, 17]		18		20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low-Z[16]	10		10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High-Z[16, 17]		18		20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power down		45		55	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid		45		55	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low-Z[16, 18]	5		10		ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH-Z[16, 17]		18		20	ns
Write Cycle[19]						
t_{WC}	Write cycle time	45		55		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35		40		ns
t_{AW}	Address setup to write end	35		40		ns
t_{HA}	Address hold from write end	0		0		ns
t_{SA}	Address setup to write start	0		0		ns
t_{PWE}	$\overline{WE}$ pulse width	35		40		ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35		40		ns
t_{SD}	Data setup to write end	25		25		ns
t_{HD}	Data hold from write end	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[16, 17]		18		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[16]	10		10		ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the AC Test Loads and Waveforms on page 5.
15. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. See application note AN13842 for further clarification.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
18. If both byte enables are toggled together, this value is 10 ns.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

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Switching Waveforms

Figure 6 shows Address Transition Controlled read cycle waveforms.[20, 21]

Figure 6. Read Cycle No. 1

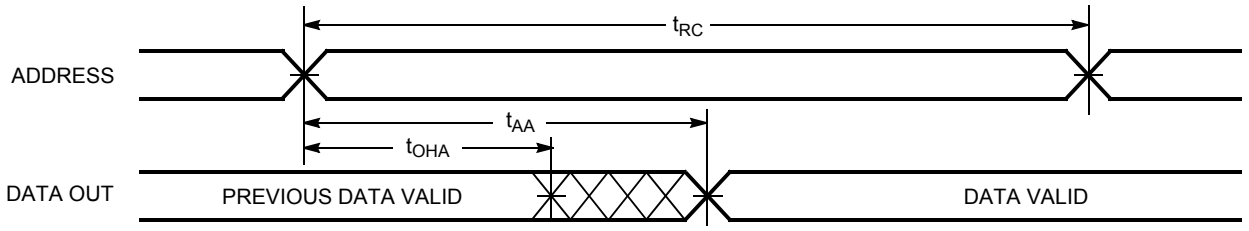
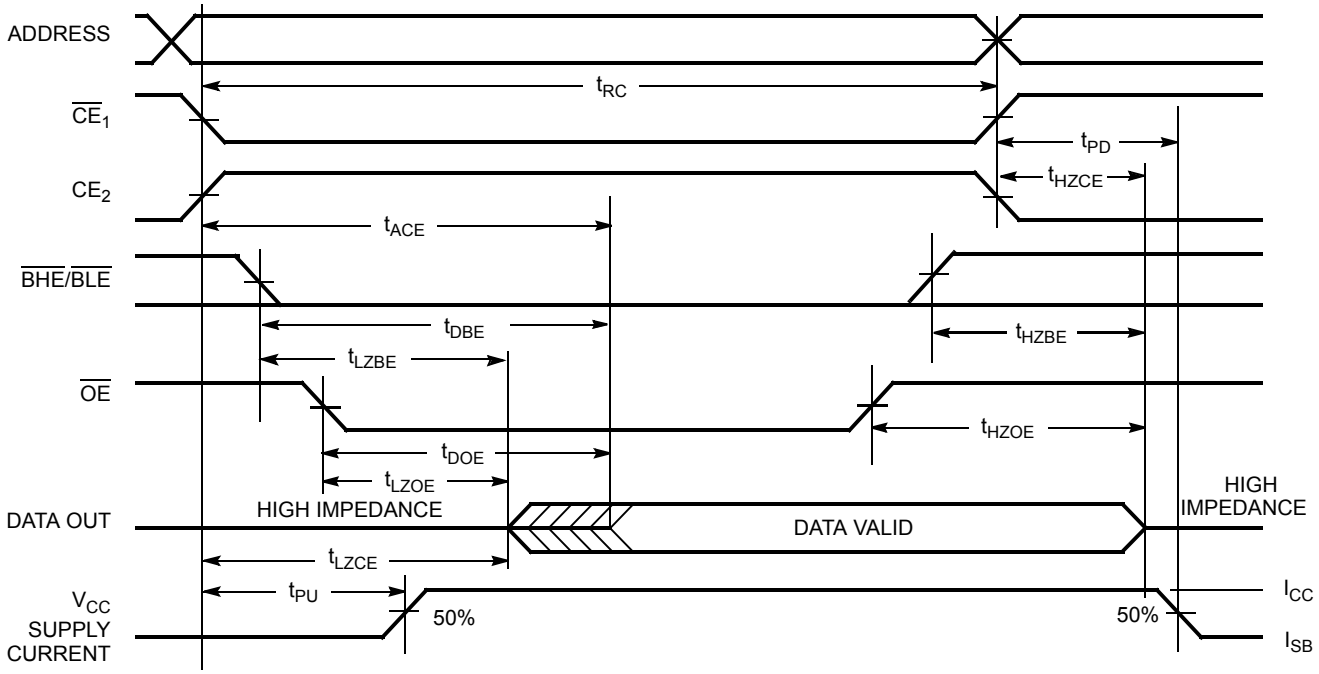


Figure 7 shows $\overline{OE}$ Controlled read cycle waveforms. [21, 22]

Figure 7. Read Cycle No. 2



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}, and CE_2 = V_{IH}.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

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Switching Waveforms (continued)

Figure 8 shows $\overline{WE}$ Controlled write cycle waveforms.[23, 24, 25]

Figure 8. Write Cycle No. 1

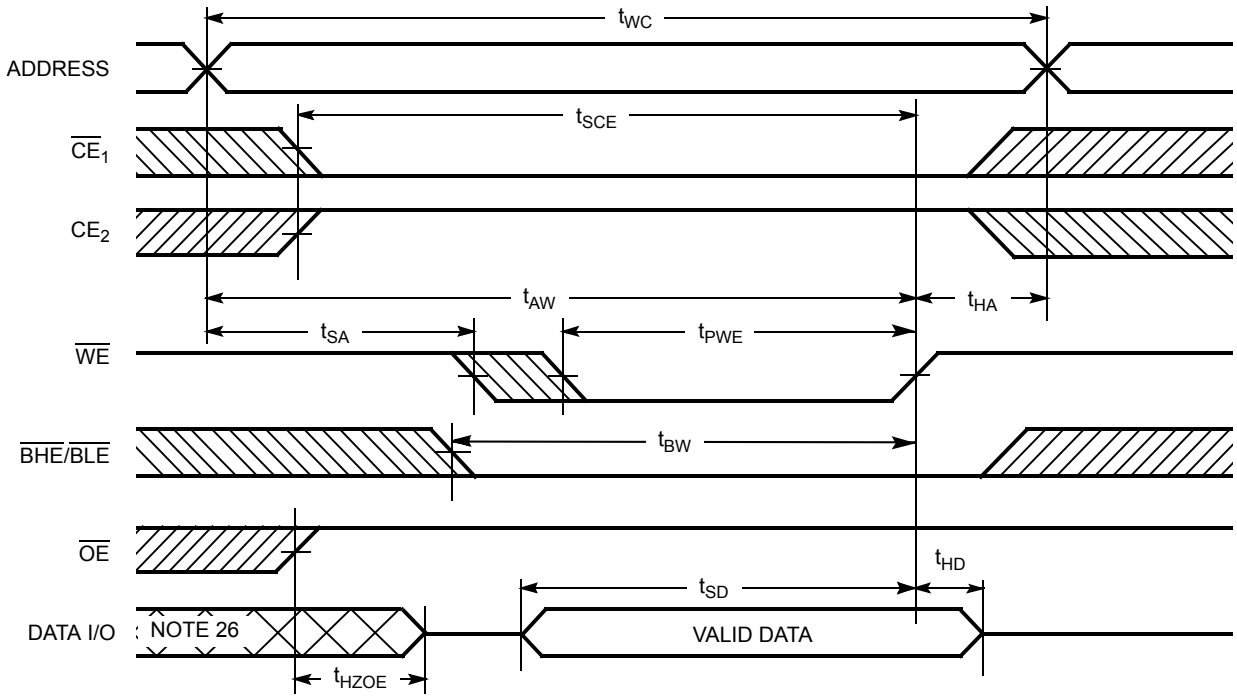
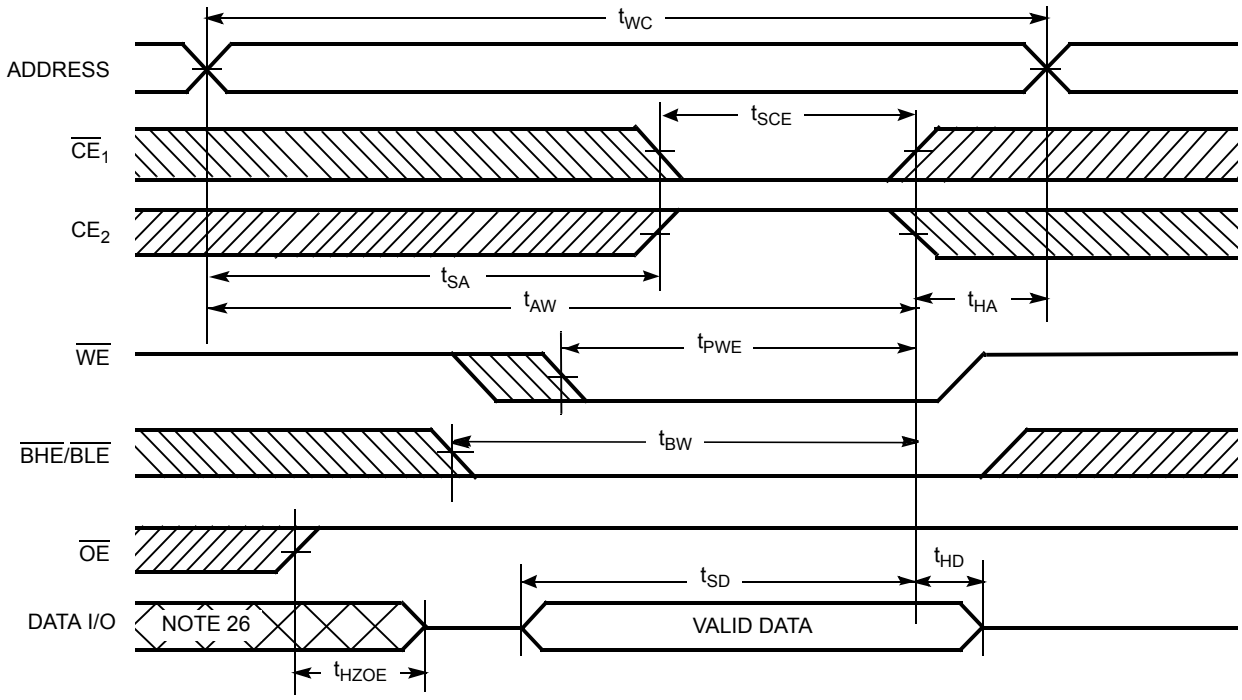


Figure 9 shows $\overline{CE}_1$ or CE_2 Controlled write cycle waveforms.[23, 24, 25]

Figure 9. Write Cycle No. 1



Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
25. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.

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Switching Waveforms (continued)

Figure 10 shows $\overline{WE}$ Controlled, $\overline{OE}$ LOW write cycle waveforms.[27]

Figure 10. Write Cycle No. 3

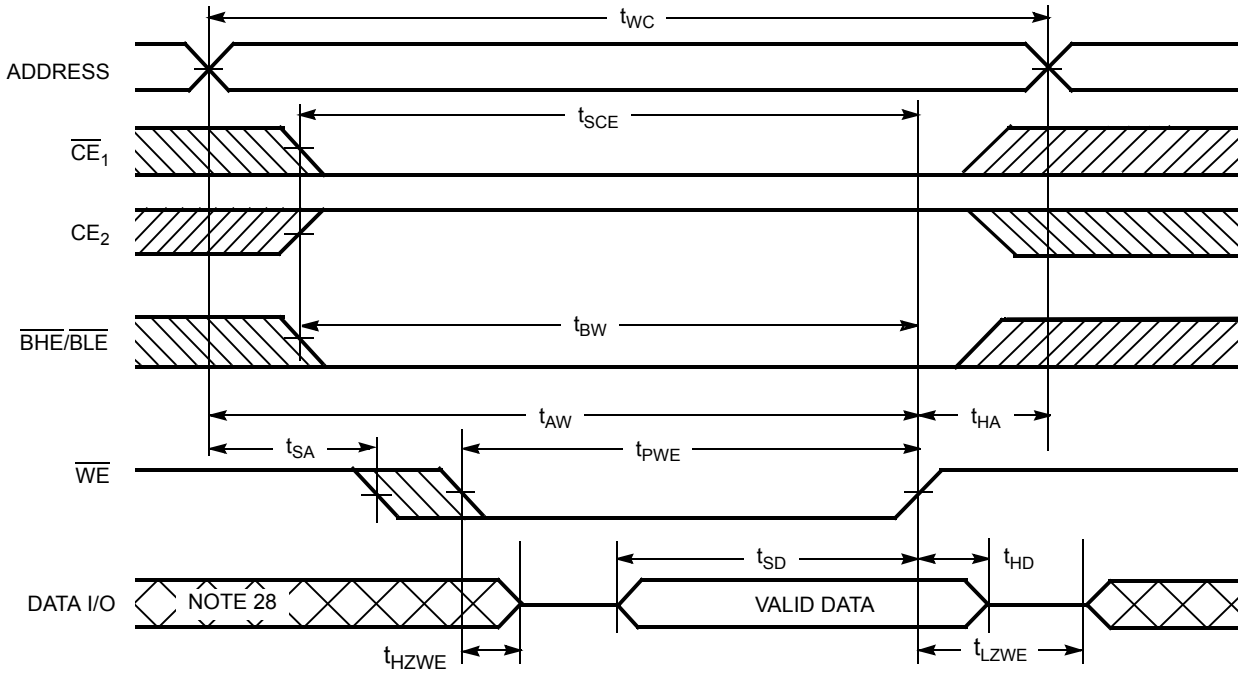
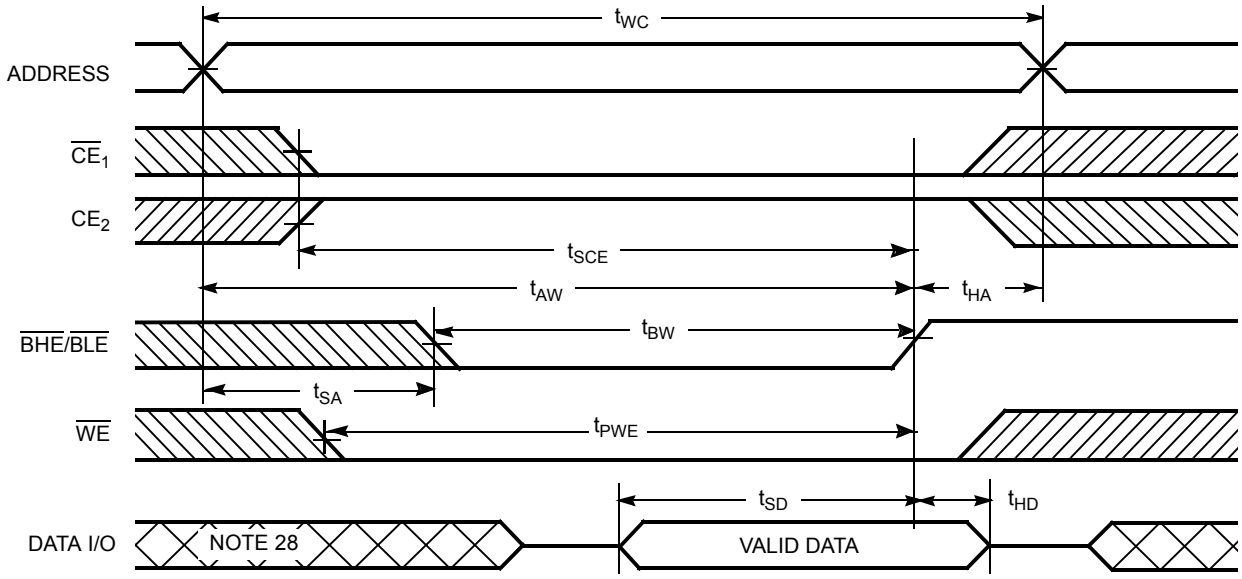


Figure 11 shows $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW write cycle waveforms.[27]

Figure 11. Write Cycle No. 4



Notes
27. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

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Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[29]	X	X	X	X	High-Z	Deselect/power down	Standby (I_{SB})
X[29]	L	X	X	X	X	High-Z	Deselect/power down	Standby (I_{SB})
X[29]	X[29]	X	X	H	H	High-Z	Deselect/power down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High-Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High-Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Note
29. The ‘X’ (Don’t care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted

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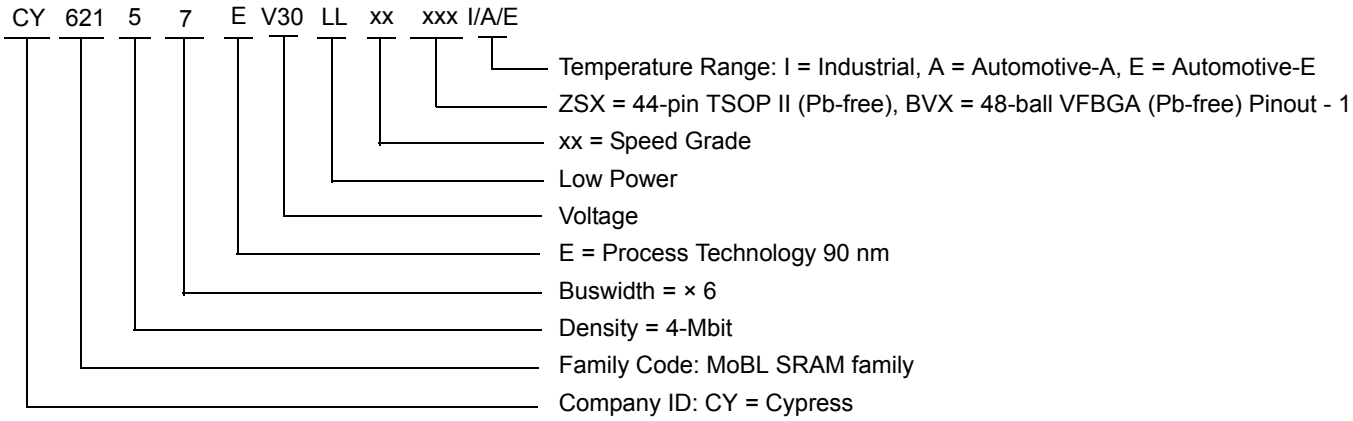
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157EV30LL-45BVI	51-85150	48-ball very fine pitch ball grid array	Industrial
	CY62157EV30LL-45BVXI	51-85150	48-ball very fine pitch ball grid array (Pb-free)	
	CY62157EV30LL-45ZSXI	51-85087	44-pin thin small outline package type II (Pb-free)	
	CY62157EV30LL-45ZXI	51-85183	48-pin thin small outline package type I (Pb-free)	
	CY62157EV30LL-45BVXA	51-85150	48-ball very fine pitch ball grid array (Pb-free)	Automotive-A
	CY62157EV30LL-45ZSXA	51-85087	44-pin thin small outline package type II (Pb-free)	
	CY62157EV30LL-45ZXA	51-85183	48-pin thin small outline package type I (Pb-free)	
55	CY62157EV30LL-55ZSXE	51-85087	44-pin thin small outline package type II (Pb-free)	Automotive-E
	CY62157EV30LL-55ZXE	51-85183	48-pin thin small outline package type I (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



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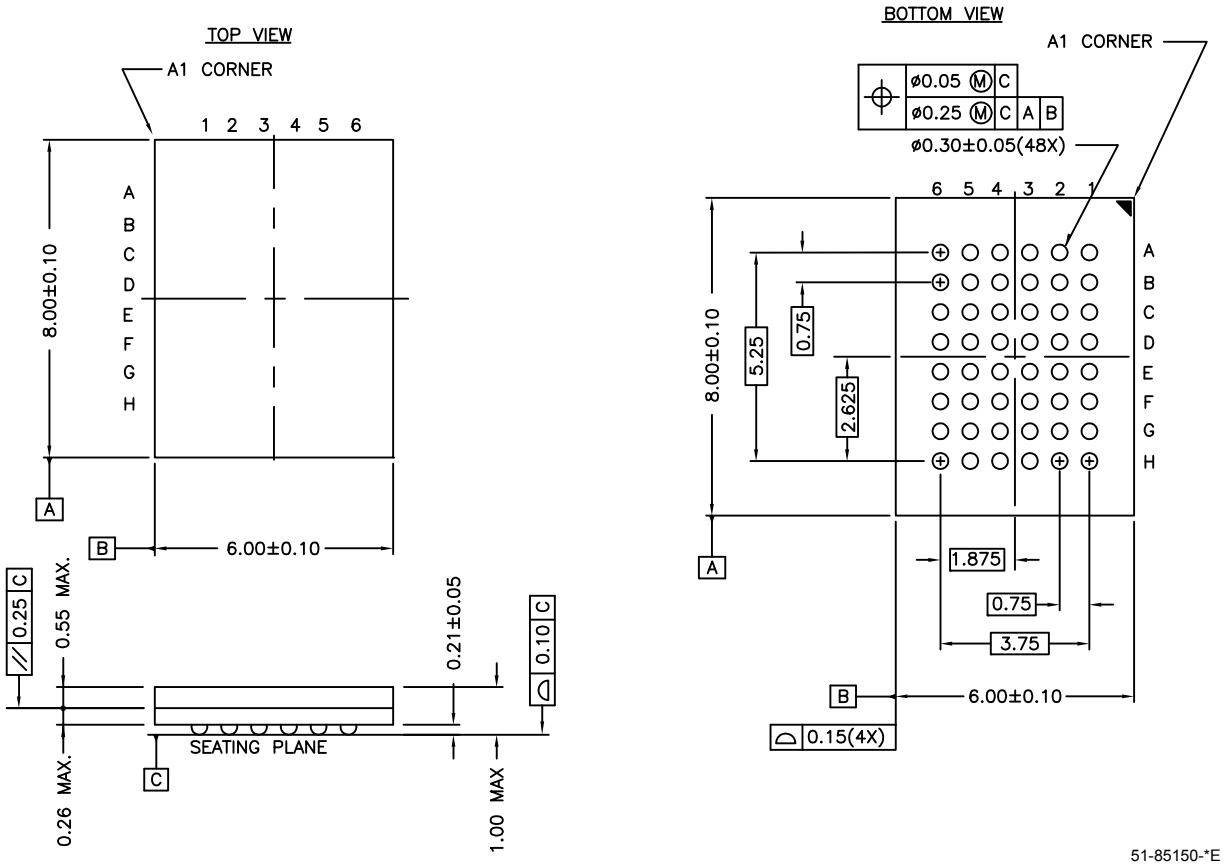
Package Diagrams

Figure 12. 48-Pin VFBGA (6 x 8 x 1 mm), 51-85150



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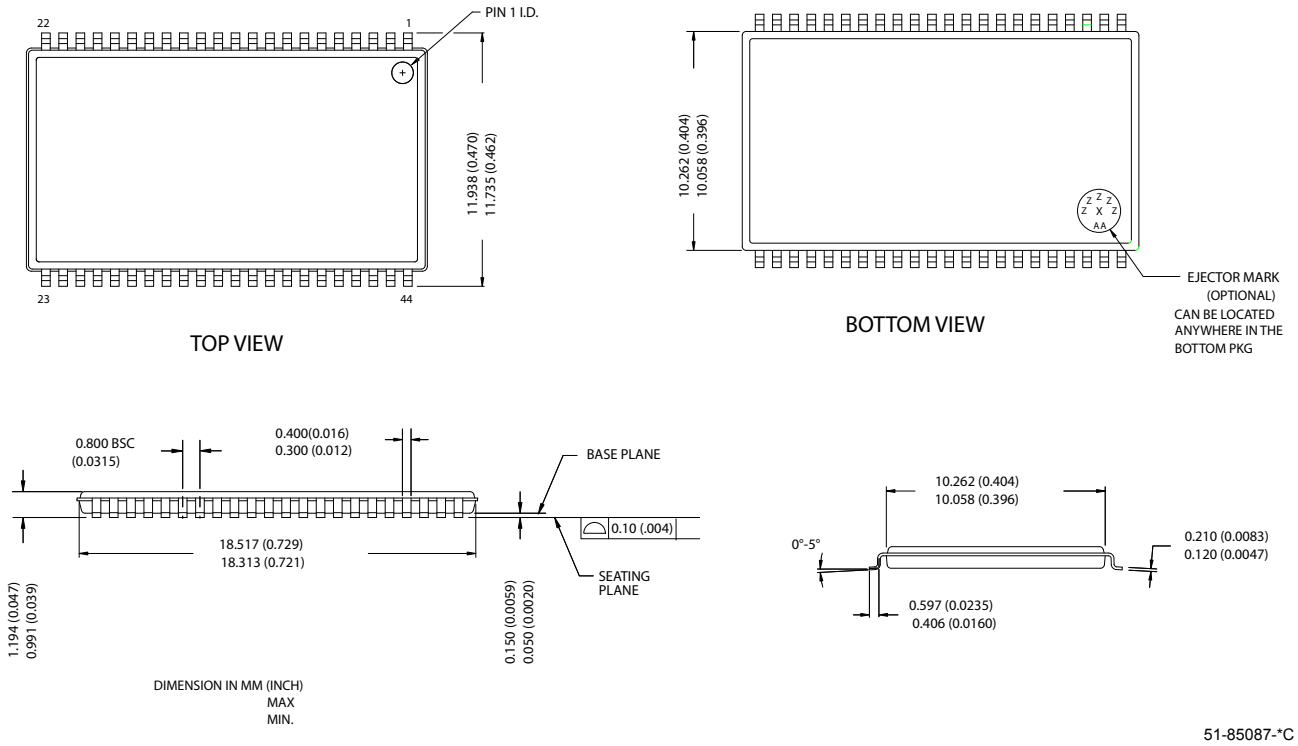
Package Diagrams (continued)

Figure 13. 44-Pin TSOP II, 51-85087



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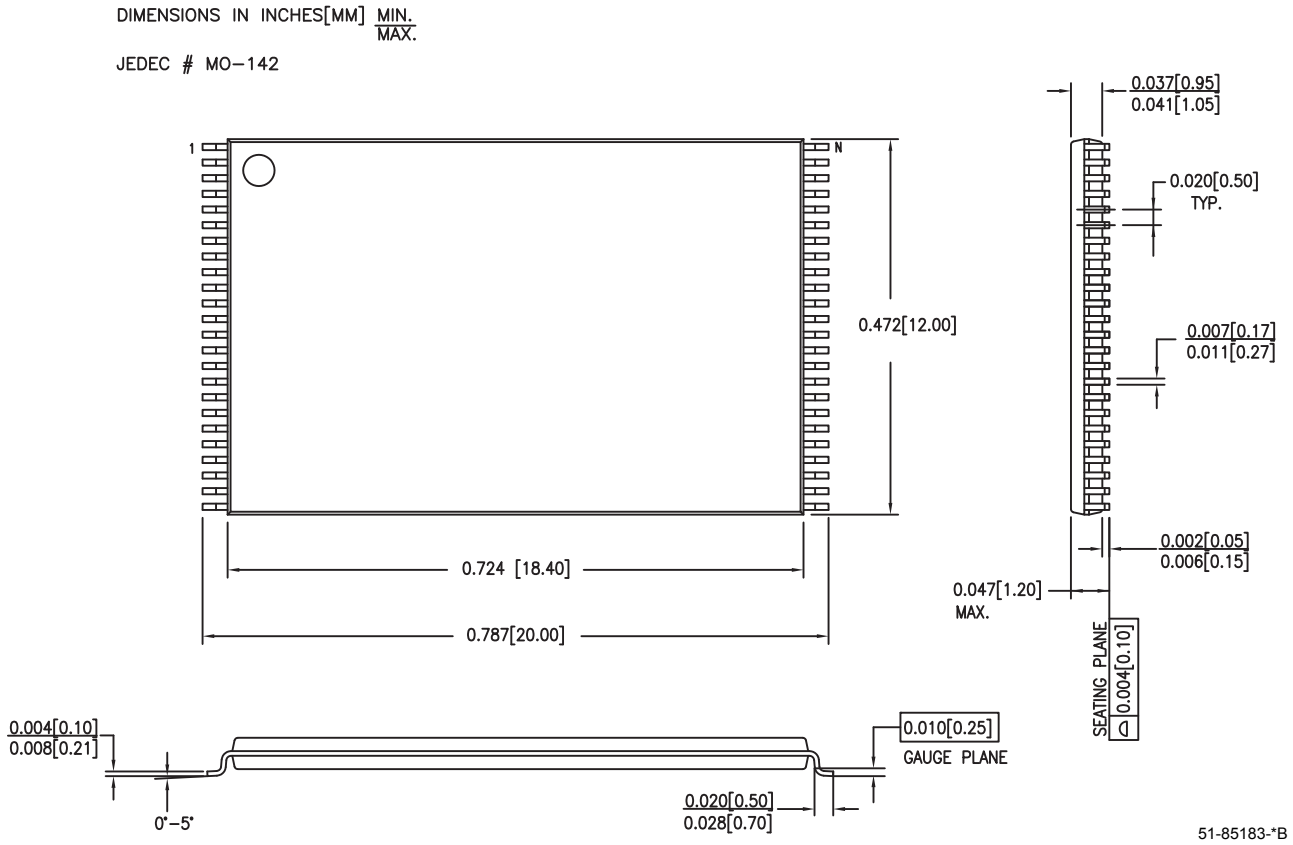
Package Diagrams (continued)

Figure 14. 48-Pin TSOP I (12 mm x 18.4 mm x 1.0 mm), 51-85183



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Document History Page

Document Title: CY62157EV30 MoBL®, 8 Mbit (512K x 16) Static RAM Document Number: 38-05445				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	202940	AJU	See ECN	New Data Sheet
*A	291272	SYT	See ECN	Converted from Advance Information to Preliminary Removed 48-TSOP I Package and the associated footnote Added footnote stating 44 TSOP II Package has only one CE on Page # 2 Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed I_{CCDR} from 4 to 4.5 μA Changed t_{OHA} from 6 to 10 ns for both 35 and 45 ns Speed Bins Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Changed t_{HZOE}, t_{HZBE} and t_{HZWE} from 12 and 15 ns to 15 and 18 ns for 35 and 45 ns Speed Bins respectively Changed t_{HZCE} from 12 and 15 ns to 18 and 22 ns for 35 and 45 ns Speed Bins respectively Changed t_{SCE}, t_{AW} and t_{BW} from 25 and 40 ns to 30 and 35 ns for 35 and 45 ns Speed Bins respectively Changed t_{SD} from 15 and 20 ns to 18 and 22 ns for 35 and 45 ns Speed Bins respectively Added Lead-Free Package Information
*B	444306	NXR	See ECN	Converted from Preliminary to Final. Changed ball E3 from DNU to NC Removed redundant footnote on DNU. Removed 35 ns speed bin Removed “L” bin Added 48 pin TSOP I package Added Automotive product information. Changed the I_{CC} Typ value from 16 mA to 18 mA and I_{CC} Max value from 28 mA to 25 mA for test condition f = fax = $1/t_{RC}$. Changed the I_{CC} Max value from 2.3 mA to 3 mA for test condition f = 1MHz. Changed the I_{SB1} and I_{SB2} Max value from 4.5 μA to 8 μA and Typ value from 0.9 μA to 2 μA respectively. Modified ISB_1 test condition to include $\overline{BHE}$, $\overline{BLE}$ Updated Thermal Resistance table. Changed Test Load Capacitance from 50 pF to 30 pF. Added Typ value for I_{CCDR} . Changed the I_{CCDR} Max value from 4.5 μA to 5 μA Corrected t_R in Data Retention Characteristics from 100 μs to t_{RC} ns. Changed t_{LZOE} from 3 to 5 Changed t_{LZCE} from 6 to 10 Changed t_{HZCE} from 22 to 18 Changed t_{LZBE} from 6 to 5 Changed t_{PWE} from 30 to 35 Changed t_{SD} from 22 to 25 Changed t_{LZWE} from 6 to 10 Added footnote #15 Updated the ordering Information and replaced the Package Name column with Package Diagram.
*C	467052	NXR	See ECN	Modified Data sheet to include x8 configurability. Updated the Ordering Information table
*D	925501	VKN	See ECN	Removed Automotive-E information Added Preliminary Automotive-A information Added footnote #10 related to I_{SB2} and I_{CCDR} Added footnote #15 related AC timing parameters
*E	1045801	VKN	See ECN	Converted Automotive-A specs from preliminary to final Updated footnote #9

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	2724889	NXR/AESA	06/26/09	Added Automotive-E information Included -45ZXA/-55ZSXE/-55ZXE parts in the Ordering Information table
*G	2927528	VKN	05/04/2010	Renamed “DNU” pins as “NC” for 48 TSOP I package Added footnote #24 related to chip enable Updated Package Diagrams Added Contents Updated links in Sales, Solutions, and Legal Information
*H	3110053	12/14/2010	PRAS	Changed Table Footnotes to Footnotes. Added Ordering Code Definitions.

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