

8-Mbit (1024K x 8) Static RAM

Features

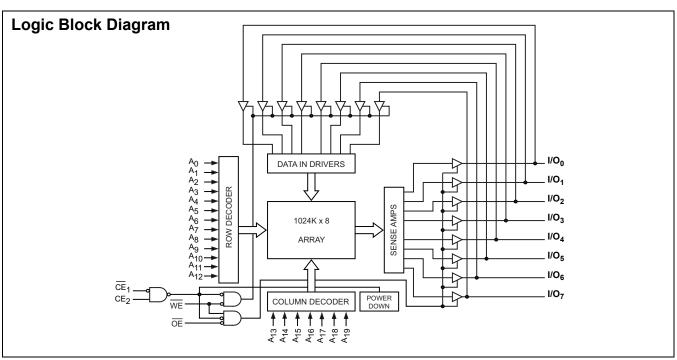
- Very high speed: 45 ns
 - □ Wide voltage range: 2.20V–3.60V
- Pin compatible with CY62158DV30
- Ultra low standby power
 - Typical standby current: 2 μA
 - Maximum standby current: 8 μA
- Ultra low active power
 - □ Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball VFBGA, 44-pin TSOP II and 48-pin TSOP I packages^[1]

Functional Description [2]

The CY62158EV30 is a high performance CMOS static RAM organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life $^{\rm TM}$ (MoBL $^{\rm S}$) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption significantly when deselected (CE $_1$ HIGH or CE $_2$ LOW). The eight input and output pins (I/O $_0$ through I/O $_7$) are placed in a high impedance state when the device is deselected (CE $_1$ HIGH or CE $_2$ LOW), the outputs are disabled (OE HIGH), or a write operation is in progress (CE $_1$ LOW and CE $_2$ HIGH and WE LOW).

To write to the device, take Chip Enables ($\overline{\text{CE}}_1$ LOW and CE₂ HIGH) and Write Enable ($\overline{\text{WE}}$) input LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₉).

To read from the device, take Chip Enables (\overline{CE}_1 LOW and \overline{CE}_2 HIGH) and \overline{OE} LOW while forcing the \overline{WE} HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See the "Truth Table" on page 9 for a complete description of read and write modes.



Notes

- 1. For 48 pin TSOP I pin configuration and ordering information, please refer to CY62157EV30 Data sheet.
- 2. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at http://www.cypress.com.

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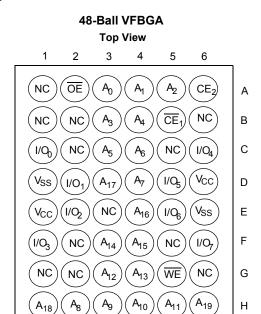
Contents

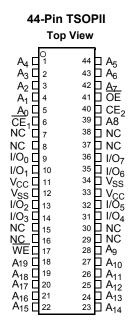
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Pin Configurations [3]





Product Portfolio

							Power	Dissipatio	n	
Product	V _{CC} Range (V)		Speed	Operating I _{CC} (mA)			Standby, I _{SB2} (μΑ)			
Floudet				(ns)	f = 1 MHz		f = 1 MHz f = f _{max}		Stariuby,	ISB2 (µA)
	Min	Typ ^[4]	Max		Typ ^[4]	Max	Typ ^[4]	Max	Typ ^[4]	Max
CY62158EV30LL	2.2	3.0	3.6	45	1.8	3	18	25	2	8

- 3. NC pins are not connected on the die.
- 4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^{\circ}C$.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested. Storage Temperature –65°C to +150°C Ambient Temperature with

Supply Voltage to Ground Potential – 0.3V to V_{CC(max)} + 0.3V

DC Voltage Applied to Outputs in High-Z State $^{[5,\ 6]}$ -0.3V to $V_{CC(max)}$ + 0.3V

DC Input Voltage ^[5, 6]	$-0.3V$ to $V_{CC(max)} + 0.3V$
Output Current into Outputs (LOW))20 mA
Static Discharge Voltage(MIL-STD-883, Method 3015)	>2001V
Latch up Current	>200 mA

Operating Range

Product	Range	Ambient Temperature (T _A)	V cc ^[7]	
CY62158EV30LL	Industrial	–40°C to +85°C	2.2V - 3.6V	

Electrical Characteristics (Over the Operating Range)

D	December 1 and	To ad O a maj	1141		Unit		
Parameter	Description	Test Conditions		Min	Typ ^[8]	Max	Oilit
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA		2.0			V
		I_{OH} = -1.0 mA, V_{CC}	; <u>≥</u> 2.70V	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA				0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \ge$	<u>2</u> .70V			0.4	V
V _{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V		1.8		V _{CC} + 0.3V	V
		V_{CC} = 2.7V to 3.6V		2.2		V _{CC} + 0.3V	V
V _{IIL}	Input LOW Voltage	V _{CC} = 2.2V to 2.7V		-0.3		0.6	V
		V _{CC} = 2.7V to 3.6V		-0.3		0.8	V
I _{IX}	Input Leakage Current	$GND \le V_1 \le V_{CC}$		– 1		+1	μΑ
I _{OZ}	Output Leakage Current	GND \leq V _O \leq V _{CC} , C	Output Disabled	– 1		+1	μΑ
I _{CC}	V _{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$ V	CC = V _{CCmax}		18	25	mA
		f = 1 MHz	_{DUT} = 0 mA MOS levels		1.8	3	mA
I _{SB1}	Automatic CE Power down Current — CMOS Inputs	$\begin{array}{ c c c c c c }\hline \hline CE_1 \geq V_{CC} - 0.2V, \ CE_2 \leq 0.2V \\ V_{IN} \geq V_{CC} - 0.2V, \ V_{IN} \leq 0.2V) \\ f = f_{max} \ (Address \ and \ Data \ Only), \\ f = 0 \ (OE \ and \ WE), \ V_{CC} = 3.60V \end{array}$			2	8	μА
I _{SB2} ^[9]	Automatic CE Power down Current — CMOS Inputs	$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{V o}$ $\text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{V or}$ $\text{f} = 0, \text{V}_{\text{CC}} = 3.60 \text{V}$	or $CE_2 \le 0.2V$, $V_{IN} \le 0.2V$,		2	8	μА

Capacitance^[10]

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz},$	10	pF
C _{OUT}	Output Capacitance	$V_{CC} = V_{CC(typ)}$	10	pF

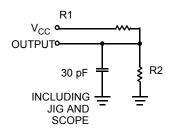
- Notes
 V_{IL(min)} = -2.0V for pulse durations less than 20 ns.
 V_{IH(max)} = V_{CC} + 0.75V for pulse duration less than 20 ns.
 Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.
 Chip enables (CE₁ and CE₂) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
 Tested initially and after any design or process changes that may affect these parameters.

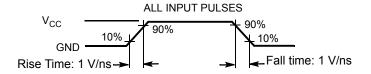


Thermal Resistance^[12]

Parameter	Description	Test Conditions	BGA	TSOP II	Unit
Θ_{JA}		Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	72	76.88	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		8.86	13.52	°C/W

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

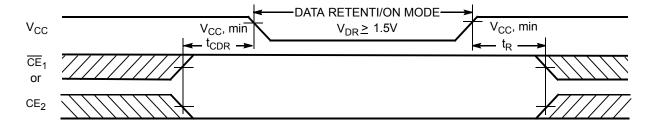
OUTPUT• V_{TH}

Parameters	2.5V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ ^[4]	Max	Unit
V_{DR}	V _{CC} for Data Retention		1.5			V
I _{CCDR} ^[11]	Data Retention Current	$V_{CC} = 1.5V, \overline{CE}_1 \ge V_{CC} - 0.2V$ or $CE_2 \le 0.2V, V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$		2	5	μА
t _{CDR} ^[12]	Chip Deselect to Data Retention Time		0			ns
t _R ^[13]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform



Note

- 11. Chip enables ($\overline{\text{CE}}_1$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- 12. Tested initially and after any design or process changes that may affect these parameters.
- 13. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \ge 100 \ \mu s$ or stable at $V_{CC(min)} \ge 100 \ \mu s$.



Switching Characteristics (Over the Operating Range) [14]

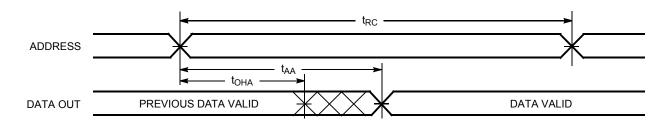
D	Decemention	45	ns	1114
Parameter	Description	Min	Max	Unit
Read Cycle		<u>'</u>	•	
t _{RC}	Read Cycle Time	45		ns
t _{AA}	Address to Data Valid		45	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	CE ₁ LOW and CE ₂ HIGH to Data Valid		45	ns
t _{DOE}	OE LOW to Data Valid		22	ns
t _{LZOE}	OE LOW to Low Z ^[15]	5		ns
t _{HZOE}	OE HIGH to High Z ^[15, 16]		18	ns
t _{LZCE}	CE ₁ LOW and CE ₂ HIGH to Low Z ^[15]	10		ns
t _{HZCE}	CE ₁ HIGH or CE ₂ LOW to High Z ^[15, 16]		18	ns
t _{PU}	CE ₁ LOW and CE ₂ HIGH to Power Up	0		ns
t _{PD}	CE ₁ HIGH or CE ₂ LOW to Power Down		45	ns
Write Cycle ^[17]	·		•	•
t_{WC}	Write Cycle Time	45		ns
t _{SCE}	CE ₁ LOW and CE ₂ HIGH to Write End	35		ns
t _{AW}	Address Setup to Write End	35		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Setup to Write Start	0		ns
t _{PWE}	WE Pulse Width	35		ns
t _{SD}	Data Setup to Write End	25		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	WE LOW to High Z ^[15, 16]		18	ns
t _{LZWE}	WE HIGH to Low Z ^[15]	10		ns

 ^{14.} Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1V/ns), timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified l_{OL}/I_{OH} as shown in "AC Test Loads and Waveforms" on page 5.
 15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} for any given device.
 16. t_{HZCE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
 17. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

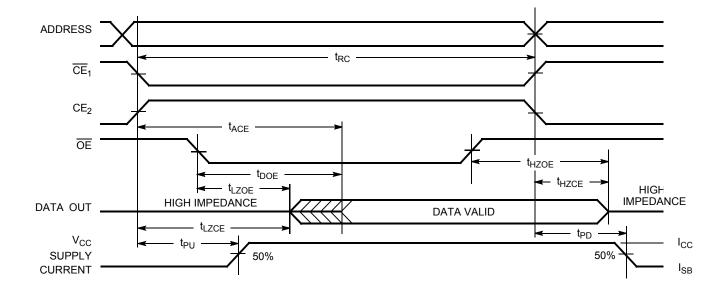


Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) $^{[18,\ 19]}$



Read Cycle No. 2 (OE Controlled)[19, 20]

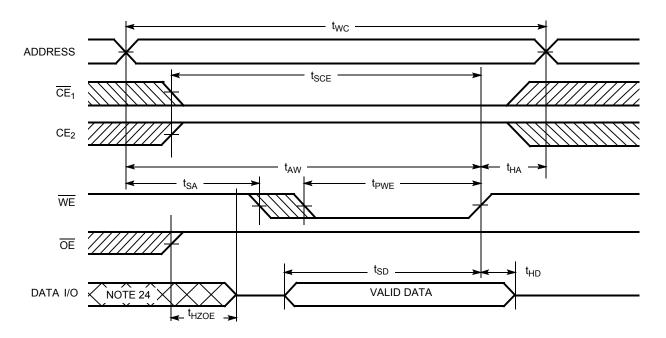


- 18. <u>Device</u> is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- 19. WE is HIGH for read cycle.
- 20. Address valid before or similar to \overline{CE}_1 transition LOW and CE_2 transition HIGH.

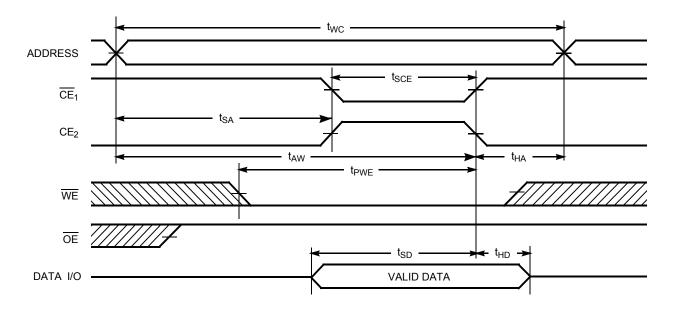


Switching Waveforms (continued)

Write Cycle No. 1 $(\overline{WE} \ \text{Controlled})^{[21,\ 22,\ 23]}$



Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled)[21, 22, 23]



- 21. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

 22. Data I/O is high impedance if OE = V_{IH}.

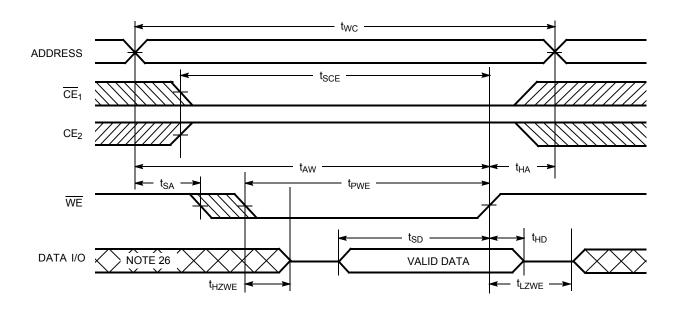
 23. If CE₁ goes HIGH or CE₂ goes LOW simultaneously with WE HIGH, the output remains in high impedance state.

 24. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Write Cycle No. 3 (WE Controlled, OE LOW)[25]



Truth Table

CE ₁	CE ₂	WE	OE	Inputs/Outputs	Mode	Power
Н	X ^[27]	Х	Х	High-Z	Deselect/Power down	Standby (I _{SB})
X ^[27]	L	Х	Х	High-Z	Deselect/Power down	Standby (I _{SB})
L	Н	Н	L	Data Out	Read	Active (I _{CC})
L	Н	L	Х	Data In	Write	Active (I _{CC})
L	Н	Н	Н	High-Z	Selected, Outputs Disabled	Active (I _{CC})

Notes

25. If $\overline{\text{CE}}_1$ goes HIGH or $\overline{\text{CE}}_2$ goes LOW simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in high impedance state.

26. During this period, the I/Os are in output state. Do not apply input signals.

27. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

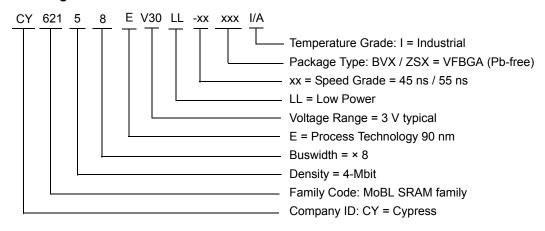


Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62158EV30LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62158EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

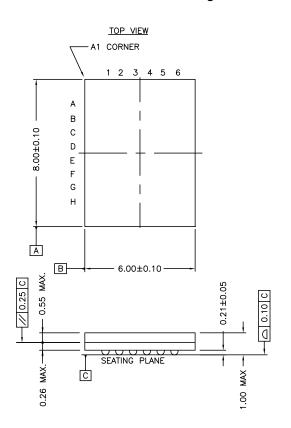


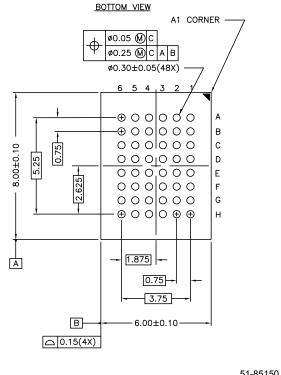
[+] Feedback



Package Diagrams

Figure 1. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



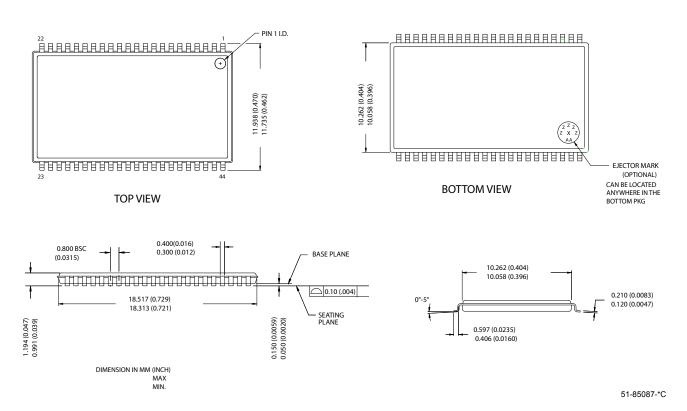


51-85150 *F



Package Diagrams (continued)

Figure 2. 44-Pin TSOP II, 51-85087



[+] Feedback



Document History Page

Document Title: CY62158EV30 MoBL [®] , 8-Mbit (1024K x 8) Static RAM Document Number: 38-05578						
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change		
**	270329	See ECN	PCI	New Data Sheet		
*A	291271	See ECN	SYT	Converted from Advance Information to Preliminary Changed I $_{CCDR}$ from 4 to 4.5 μA		
*B	444306	See ECN	NXR	Converted from Preliminary to Final. Removed 35 ns speed bin Removed "L" bin. Removed 44 pin TSOP II package Included 48 pin TSOP I package Changed the I_{CC} Typ value from 16 mA to 18 mA and I_{CC} max value from 28 mA to 25 mA for test condition f = fax = $1/t_{RC}$. Changed the I_{CC} max value from 2.3 mA to 3 mA for test condition f = 1MHz. Changed the I_{SB1} and I_{SB2} max value from 4.5 μ A to 8 μ A and Typ value from 0.9 μ A to 2 μ A respectively. Updated Thermal Resistance table Changed Test Load Capacitance from 50 pF to 30 pF. Added Typ value for I_{CCDR} . Changed the I_{CCDR} max value from 4.5 μ A to 5 μ A Corrected I_{R} in Data Retention Characteristics from 100 μ s to I_{RC} ns Changed I_{LZOE} from 3 to 5 Changed I_{LZCE} from 6 to 10 Changed I_{RCE} from 22 to 18 Changed I_{RCE} from 30 to 35 Changed I_{RCE} from 6 to 10 Updated the ordering Information and replaced the Package Name column with Package Diagram.		
*C	467052	See ECN	NXR	Included 44 pin TSOP II package in Product Offering. Removed TSOP I package; Added reference to CY62157EV30 TSOP I Updated the ordering Information table		
*D	1015643	See ECN	VKN	Added footnote #8 related to I _{SB2} and I _{CCDR}		
*E	2934396	06/03/10	VKN	Added footnote #21 related to chip enable Updated package diagrams Updated template		
*F	3110202	12/14/2010	PRAS	Updated Logic Block Diagram and Package Diagram. Added Ordering Code Definitions.		

[+] Feedback



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