CY7C1325G

4-Mbit (256 K × 18) Flow through Sync SRAM

Features

- 256 K × 18 common I/O
- 3.3 V core power supply (V_{DD})
- 2.5 V or 3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
- 6.5 ns (133 MHz version)
- Provide high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed write
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package, Pb-free and non Pb-free 119-ball BGA Package
- “ZZ” sleep mode option

Functional Description

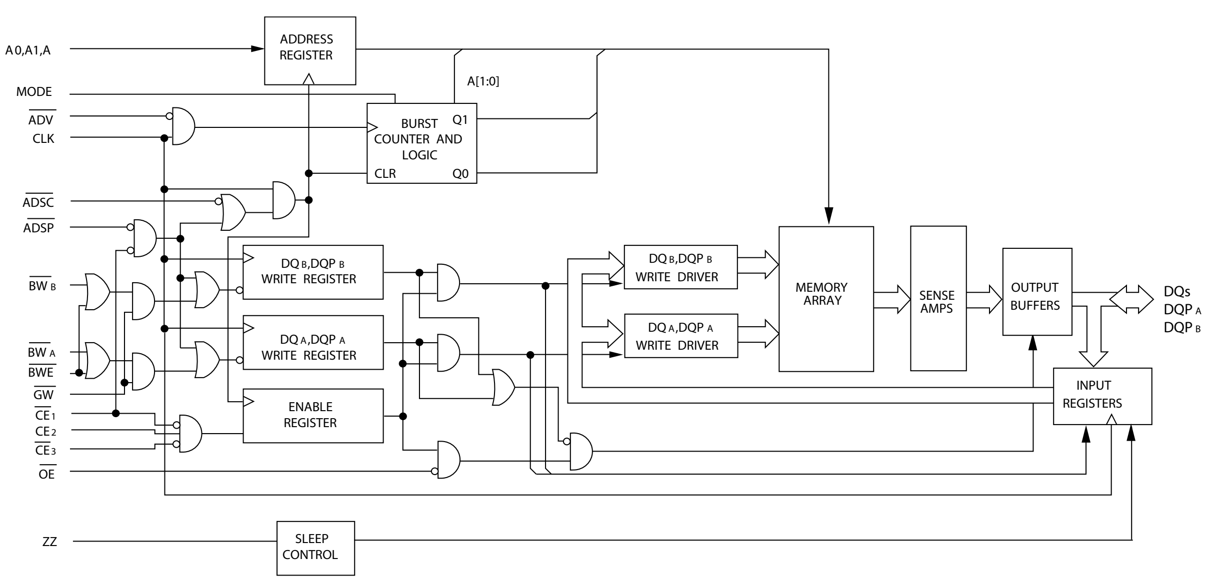
The CY7C1325G[1] is a 256 K × 18 synchronous cache RAM designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2 bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE_1}$), depth-expansion chip enables (CE_2 and $\overline{CE_3}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW_{[A:B]}}$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

The CY7C1325G allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ($\overline{ADV}$).

The CY7C1325G operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

Logic Block Diagram



Note
1. For best practice recommendations, refer to the Cypress application note “*System Design Guidelines*” on www.cypress.com.

[+] Feedback

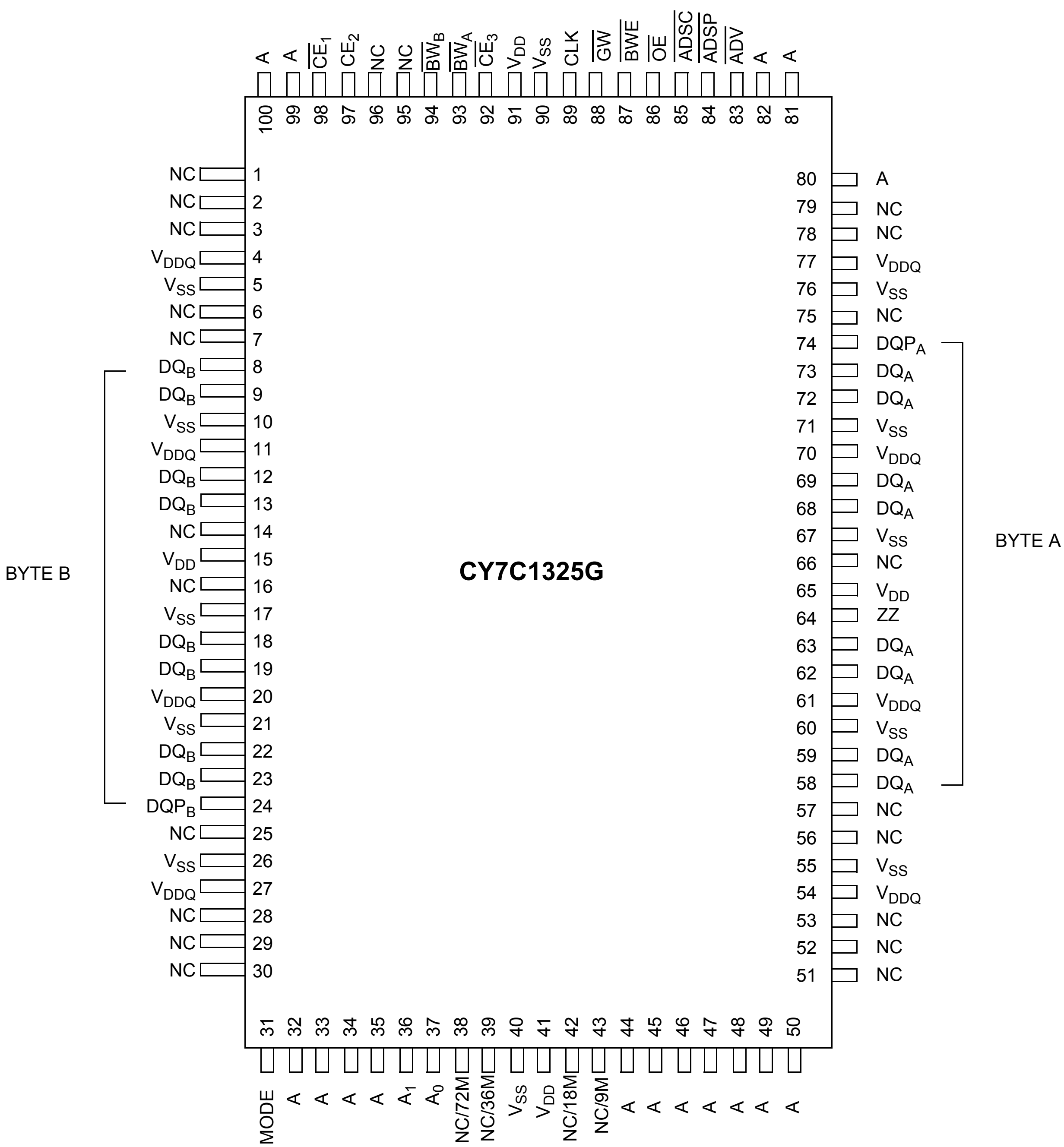
Contents

Selection Guide

Description	133 MHz	100 MHz	Unit
Maximum access time	6.5	8.0	ns
Maximum operating current	225	205	mA
Maximum standby current	40	40	mA

Pin Configurations

Figure 1. 100-pin TQFP Pinout



Pin Configurations *(continued)*

Figure 2. 119-ball BGA Pinout

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC/288M	CE_2	A	$\overline{ADSC}$	A	$\overline{CE_3}$	NC/576M
C	NC/144M	A	A	V_{DD}	A	A	NC/1G
D	DQ_B	NC	V_{SS}	NC	V_{SS}	DQP_A	NC
E	NC	DQ_B	V_{SS}	$\overline{CE_1}$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{BW_B}$	$\overline{ADV}$	V_{SS}	NC	DQ_A
H	DQ_B	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CLK	V_{SS}	NC	DQ_A
L	DQ_B	NC	V_{SS}	NC	$\overline{BW_A}$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	DQ_B	NC	V_{SS}	A1	V_{SS}	DQ_A	NC
P	NC	DQP_B	V_{SS}	A0	V_{SS}	NC	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC/72M	A	A	NC/36M	A	A	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Pin Definitions

Name	I/O	Description
A0, A1, A	Input-synchronous	**Address inputs used to select one of the 256 K address locations.** Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are sampled active. $A_{[1:0]}$ feed the 2 bit counter.
$\overline{BW_A}$, $\overline{BW_B}$	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_{[A:B]}$ and $\overline{BWE}$).
$\overline{BWE}$	Input-synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE_1}$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. $\overline{CE_1}$ is sampled only when a new external address is loaded.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE_3}$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device. $\overline{CE_3}$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.

Pin Definitions *(continued)*

Name	I/O	Description
$\overline{ADV}$	Input-synchronous	**Advance input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-asynchronous	**ZZ "sleep" input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved.During normal operation, this pin has to be low or left floating. ZZ pin has an internal pull-down.
DQs $DQP_{A,}$ DQP_B	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and $DQP_{[A:B]}$ are placed in a tristate condition.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
MODE	Input-static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.
NC		**No connects**. Not Internally connected to the die.
NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**No connects**. Not internally connected to the die. NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins that are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

The CY7C1325G supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable (BWE) and byte write select ($BW_{[A:B]}$) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip selects (CE_1, CE_2, CE_3) and an asynchronous output enable (OE) provide for easy bank selection and output tristate control. ADSP is ignored if CE_1 is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) CE_1, CE_2, and CE_3 are all asserted active, and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the OE input is asserted LOW, the requested data is available at the data outputs, a maximum to t_{CDV} after clock rise. ADSP is ignored if CE_1 is HIGH.

Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1) CE_1, CE_2, CE_3 are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and $BW_{[A:B]}$) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data is latched and written into the device. Byte writes are allowed. During byte writes, BW_A controls DQ_A and BW_B controls DQ_B. All I/Os are tristated during a byte write.Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQ_s. As a safety precaution, the data lines are tristated after a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at clock rise: (1) CE_1, CE_2, and CE_3 are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deasserted HIGH, and (4) the write input signals (GW, BWE, and $BW_{[A:B]}$) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to $DQ_{[A:D]}$ is written into the specified address location. Byte writes are allowed. During byte writes, BW_A controls DQ_A, BW_B controls DQ_B. All I/Os are tristated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQ_s. As a safety precaution, the data lines are tristated after a write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1325G provides an on-chip two bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. CEs, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD}$ – 0.2 V	–	40	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD}$ – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The Truth Table for part CY7C1325G is as follows. [2, 3, 4, 5, 6]

Cycle Description	Address Used	$\overline{CE}_1$	CE_2	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	X	X	X	L	H	L	X	X	X	L-H	Tri-state
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-state
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-state
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-state
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-state
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-state
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-state
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes

2. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
3. $\overline{WRITE}$ = L when any one or more Byte Write enable signals ($\overline{BW}_A$, $\overline{BW}_B$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte write enable signals ($\overline{BW}_A$, $\overline{BW}_B$), $\overline{BWE}$, $\overline{GW}$ = H.
4. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{[A:B]}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The Truth Table for Read/Write for part CY7C1325G is as follows. [7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write byte A – (DQ_A and DQP_A)	H	L	H	L
Write byte B – (DQ_B and DQP_B)	H	L	L	H
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

Note
7. X = “Don’t Care.” H = Logic HIGH, L = Logic LOW.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with
power applied .... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND ....–0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND....... –0.5 V to $+V_{DD}$

DC voltage applied to outputs
in tristate ....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage ....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage... > 2001 V
(per MIL-STD-883, method 3015)

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature]	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single bit upsets	25 °C	361	394	FIT/ Mb
LMBU	Logical multi bit upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single event latch up	85 °C	0	0.1	FIT/ Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN 54908 “Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates”

Electrical Characteristics

Over the Operating Range [8, 9]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[8]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	$GND \le V_I \le V_{DDQ}$		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output leakage current	$GND \le V_I \le V_{DDQ}$, output disabled		–5	5	µA
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{CYC}$	7.5 ns cycle, 133 MHz	–	225	mA
			10 ns cycle, 100 MHz	–	205	mA

Notes
8. Overshoot: $V_{IH}(AC) < V_{DD}$ + 1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2$ V (Pulse width less than $t_{CYC}/2$).
9. $T_{power\ up}$: Assumes a linear ramp from 0 V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.

Electrical Characteristics *(continued)*

Over the Operating Range [8, 9]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{SB1}	Automatic CE power-down current—TTL inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	90	mA
			10 ns cycle, 100 MHz	–	80	mA
I_{SB2}	Automatic CE power-down current—CMOS inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = 0, inputs static	All speeds	–	40	mA
I_{SB3}	Automatic CE power-down current—CMOS inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{DDQ} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	75	mA
			10 ns cycle, 100 MHz	–	65	mA
I_{SB4}	Automatic CE power-down current—TTL inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = 0, inputs static	All speeds	–	45	mA

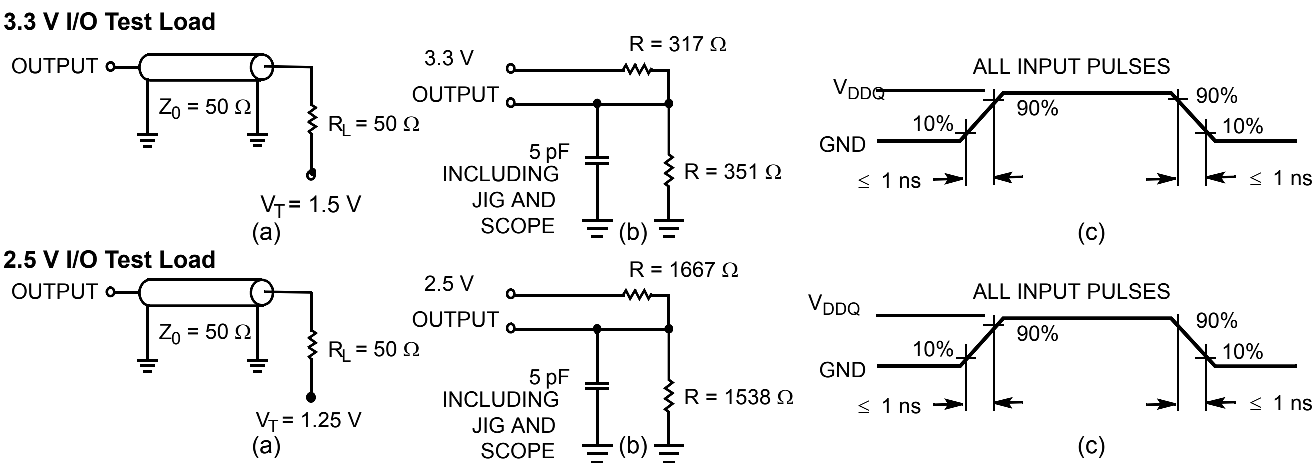
Capacitance[10]

Parameter	Description	Test Conditions	100-pin TQFP Max	119-ball BGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 3.3 V	5	5	pF
C_{CLK}	Clock input capacitance		5	5	pF
$C_{I/O}$	Input/output capacitance		5	7	pF

Thermal Resistance[10]

Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	30.32	34.1	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.85	14.0	°C/W

Figure 3. AC Test Loads and Waveforms



Note

10. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range[11, 12]

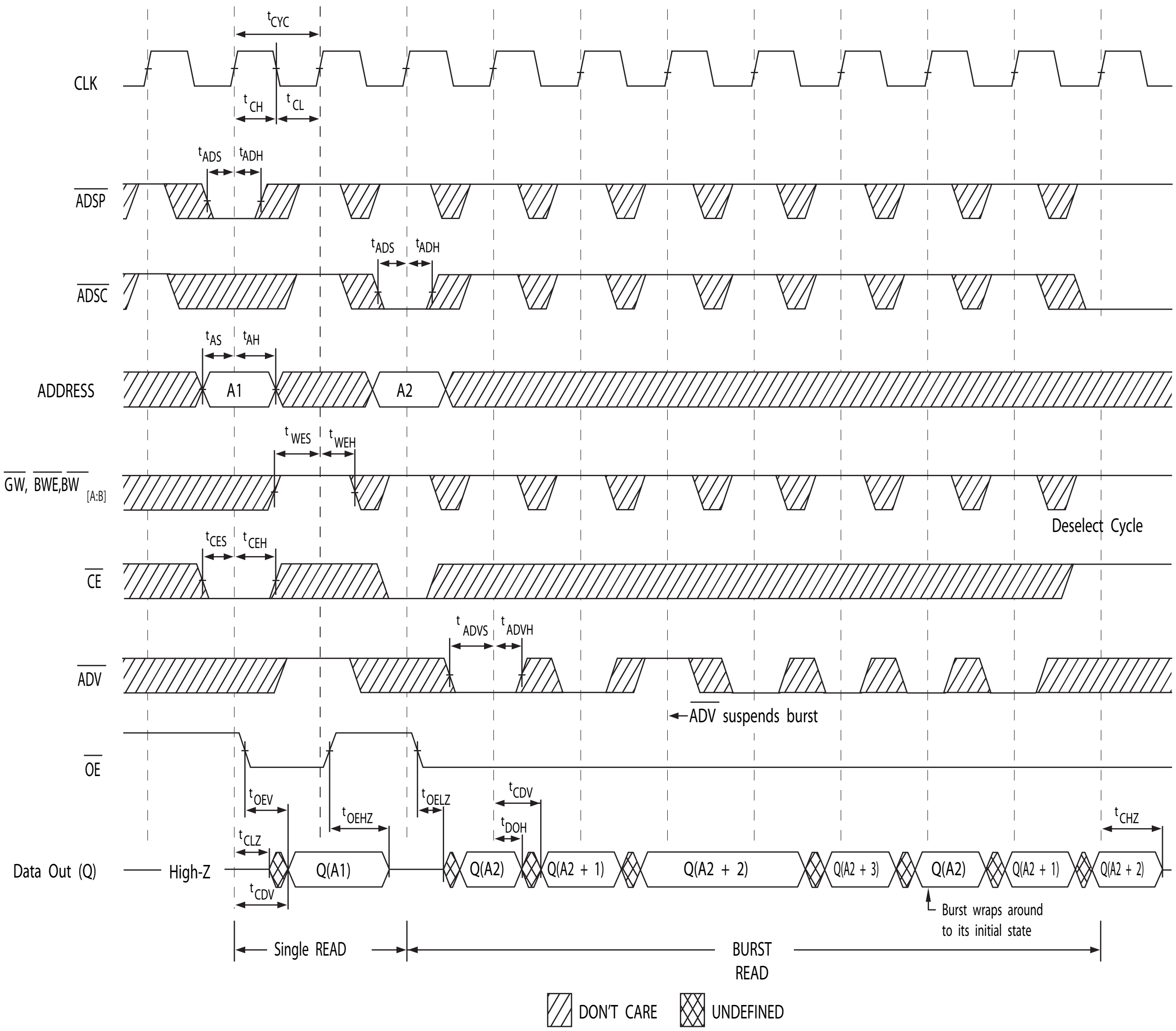
Parameter	Description	–133		–100		Unit
		Min	Max	Min	Max	
t_{POWER}	V_{DD}(Typical) to the first access[13]	1	–	1	–	ms
Clock						
t_{CYC}	Clock cycle time	7.5	–	10	–	ns
t_{CH}	Clock HIGH	2.5	–	4.0	–	ns
t_{CL}	Clock LOW	2.5	–	4.0	–	ns
Output Times						
t_{CDV}	Data output valid after CLK rise	–	6.5	–	8.0	ns
t_{DOH}	Data output hold after CLK rise	2.0	–	2.0	–	ns
t_{CLZ}	Clock to low Z[14, 15, 16]	0	–	0	–	ns
t_{CHZ}	Clock to high Z[14, 15, 16]	–	3.5	–	3.5	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.5	–	3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z[14, 15, 16]	0	–	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z[14, 15, 16]	–	3.5	–	3.5	ns
Setup Times						
t_{AS}	Address setup before CLK rise	1.5	–	2.0	–	ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ setup before CLK rise	1.5	–	2.0	–	ns
t_{ADVS}	$\overline{ADV}$ setup before CLK rise	1.5	–	2.0	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_X$ setup before CLK rise	1.5	–	2.0	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	2.0	–	ns
t_{CES}	Chip enable setup	1.5	–	2.0	–	ns
Hold Times						
t_{AH}	Address hold after CLK rise	0.5	–	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_X$ hold after CLK rise	0.5	–	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	0.5	–	ns

Notes

11. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
12. Test conditions shown in (a) of Figure 3 on page 11 unless otherwise noted.
13. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially before a read or write operation can be initiated.
14. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 3 on page 11. Transition is measured ± 200 mV from steady-state voltage.
15. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
16. This parameter is sampled and not 100% tested.

Timing Diagrams

Figure 4. Read Cycle Timing[17]

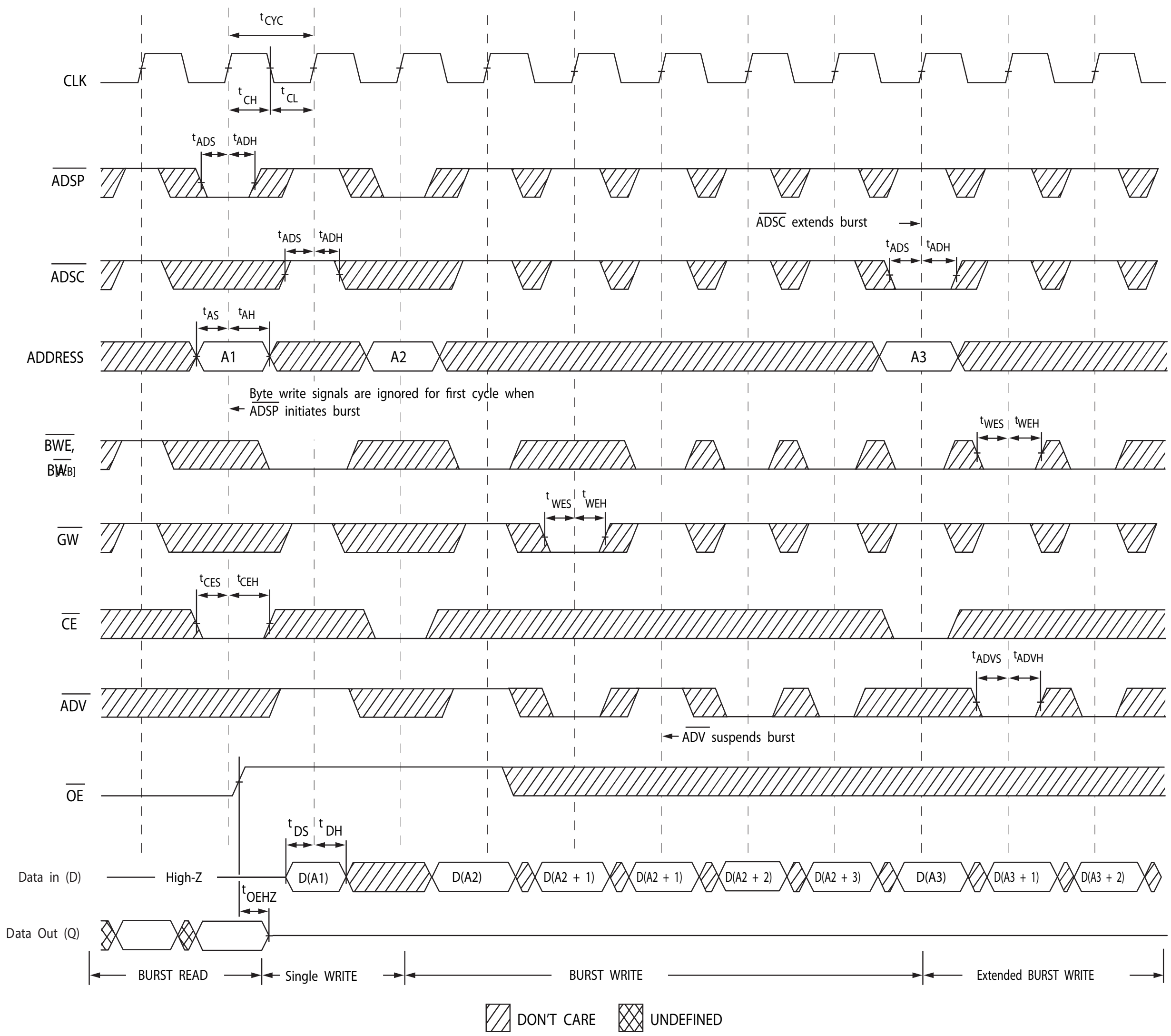


Note

17. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Timing Diagrams *(continued)*

Figure 5. Write Cycle Timing[18, 19]

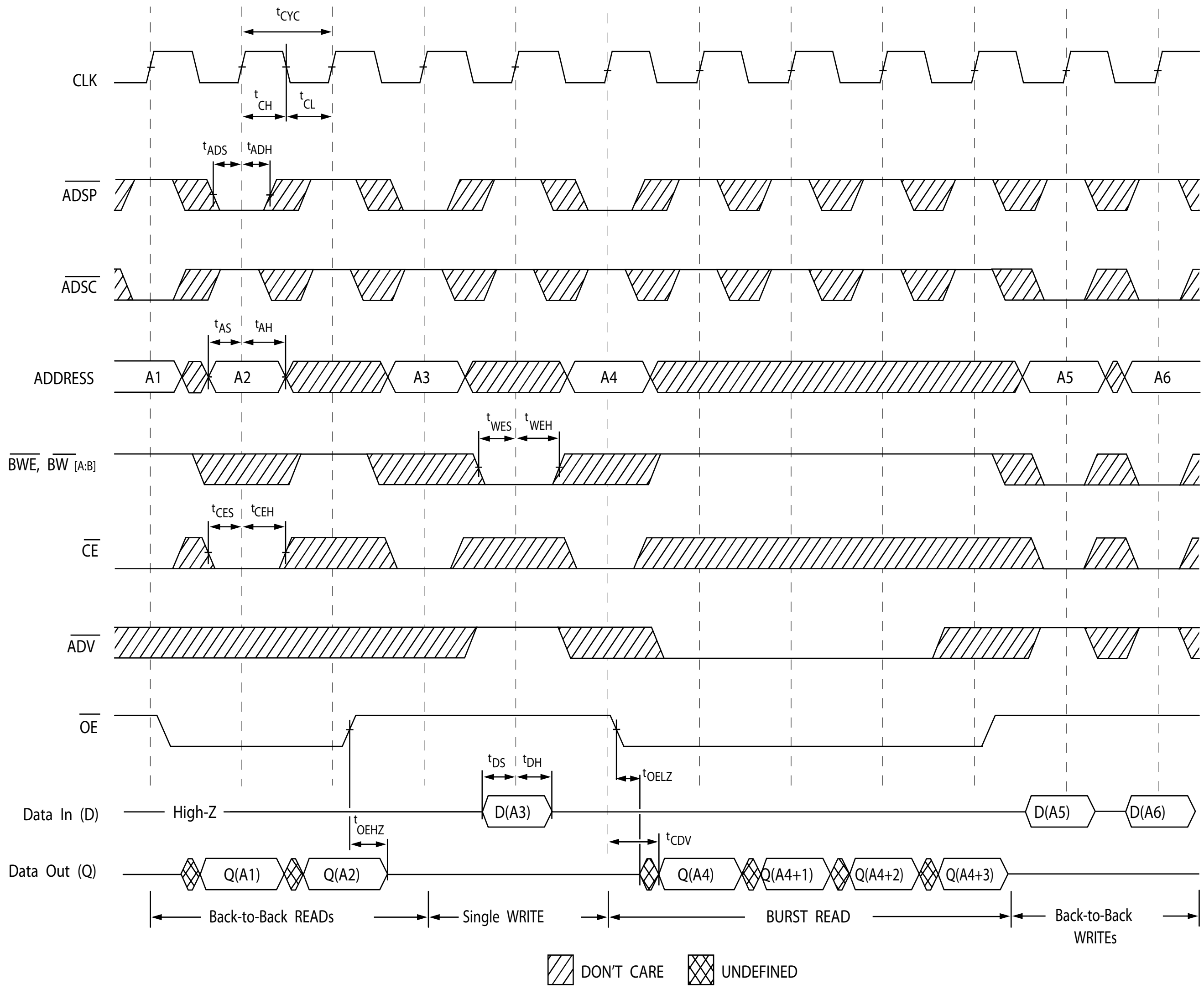


Notes

18. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
19. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_{[A:B]}$ LOW.

Timing Diagrams *(continued)*

Figure 6. Read/Write Timing[20, 21, 22]

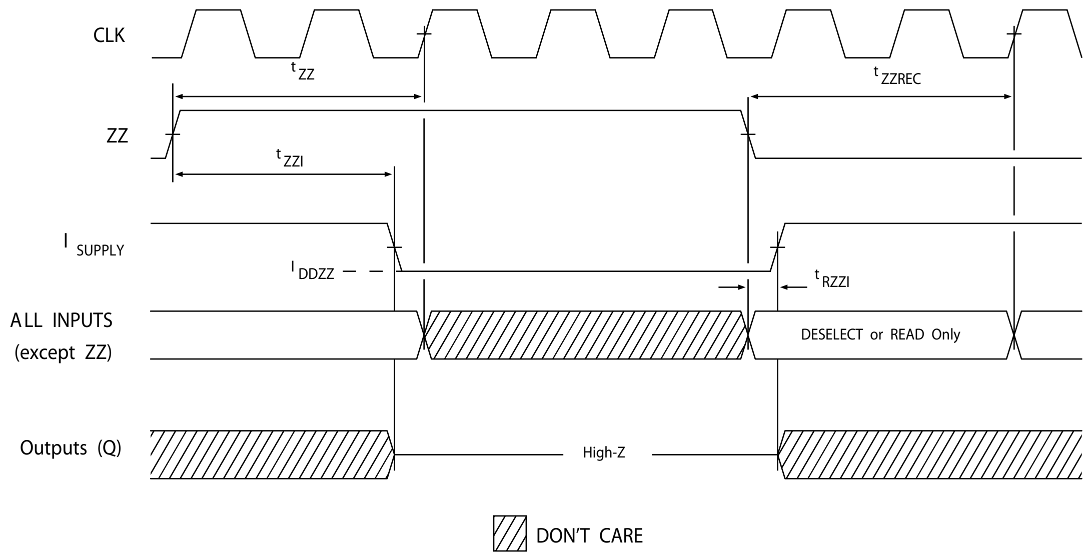


Notes

20. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
21. The data bus (Q) remains in High Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
22. $\overline{GW}$ is HIGH.

Timing Diagrams *(continued)*

Figure 7. ZZ Mode Timing[23, 24]



Notes

23. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
24. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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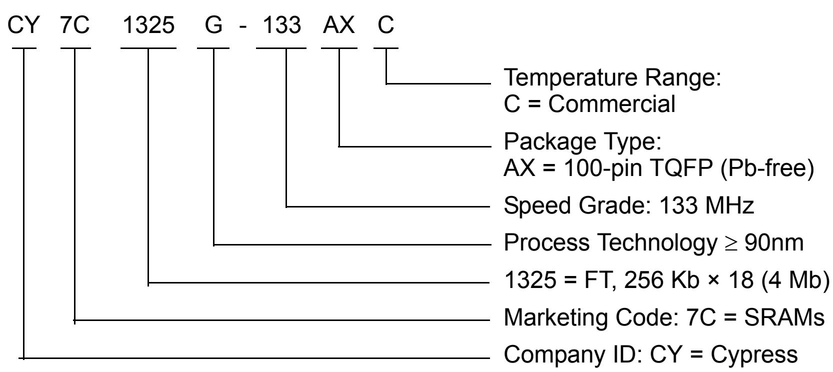
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1325G-133AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial

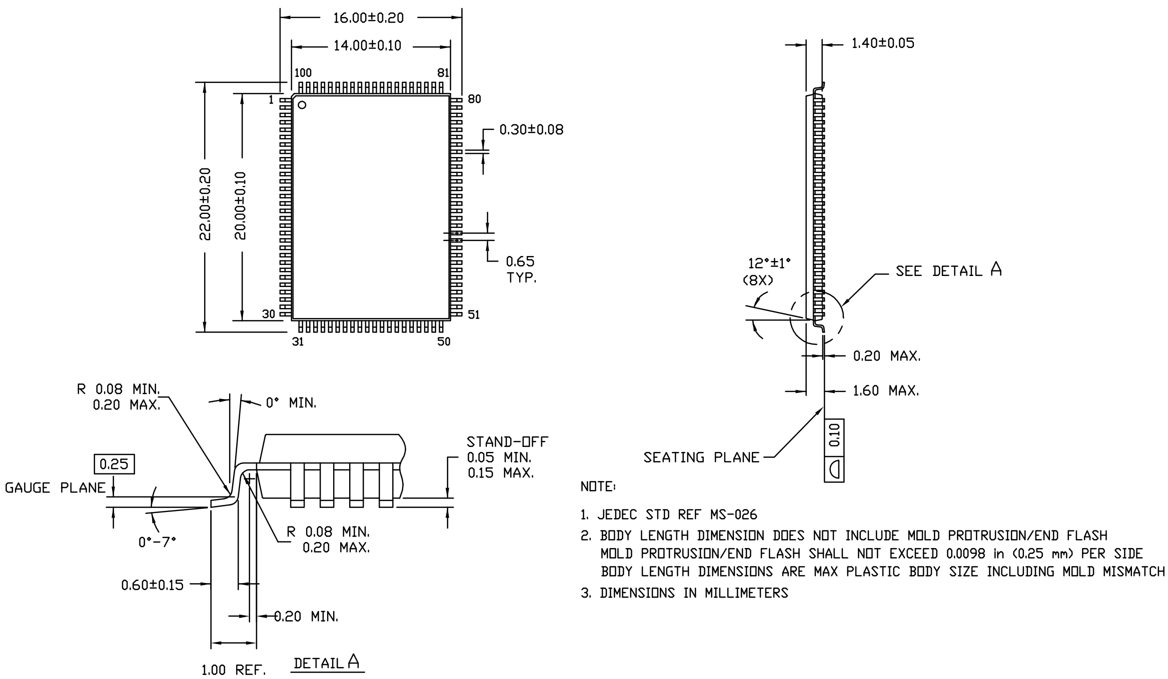
Ordering Code Definitions



[+] Feedback

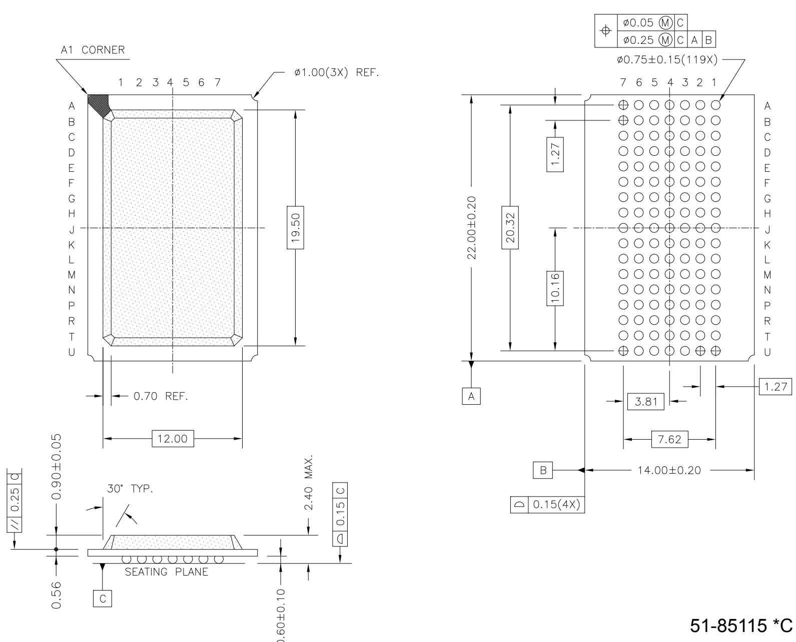
Package Diagrams

Figure 8. 100-pin TQFP (14 × 20 × 1.4 mm), 51-85050



51-85050 *D

Figure 9. 119-ball BGA (14 × 22 × 2.4 mm), 51-85115



51-85115 *C

Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
CE	chip enable
CEN	clock enable
I/O	input/output
OE	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

Document History Page

Revision	ECN	Orig. of Change	Submission Date	Description of Change
Document Title: CY7C1325G, 4-Mbit (256 K × 18) Flow through Sync SRAM Document Number: 38-05518				
**	224366	RKF	See ECN	New datasheet
*A	283775	VBL	See ECN	Deleted 66 MHz Changed TQFP package to Pb-Free TQFP in Ordering Information section Added BG Pb-Free package
*B	333626	SYT	See ECN	Removed 117 MHz speed bin Modified Address Expansion balls in the pinouts for 100 TQFP and 119 BGA Packages as per JEDEC standards and updated the Pin Definitions accordingly Modified $V_{OL,}$ V_{OH} test conditions Replaced 'Snooze' with 'Sleep' Replaced TBD's for Θ_{JA} and Θ_{JC} to their respective values on the Thermal Resistance table Changed the package name for 100 TQFP from A100RA to A101 Removed comment on the availability of BG Pb-Free package Updated the Ordering Information by shading and unshading MPNs as per availability
*C	418633	RXU	See ECN	Converted From Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Modified test condition in Footnote from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$ Modified "Input Load" to "Input Leakage Current except ZZ and MODE" in the Electrical Characteristics Table. Replaced Package Name column with Package Diagram in the Ordering Information table Replaced Package Diagram of 51-85050 from *A to *B Updated the Ordering Information
*D	480124	VKN	See ECN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND. Updated the Ordering Information table.
*E	2756998	VKN	08/28/09	Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information.
*F	3036073	NJY	09/22/2010	Added Ordering Code Definitions. Updated Package Diagrams. Added Acronyms and Units of Measure. Minor edits and updated in new template.
*G	3052903	NJY	10/08/10	Removed the following pruned part from the ordering information table. CY7C1325G-100AXI
*H	3208774	NJY	03/29/2011	Updated Ordering Information. Updated Package Diagrams.

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