4-Mbit (128 K × 36) Pipelined Sync SRAM

Features

- Fully registered inputs and outputs for pipelined operation
- 128 K × 36 common I/O architecture
- 3.3 V core power supply (V_{DD})
- 2.5- / 3.3-V I/O power supply (V_{DDQ})
- Fast clock to output times: 2.6 ns (for 250 MHz device)
- User selectable burst counter supporting Intel Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed writes
- Asynchronous output enable
- Offered in Pb-free 100-pin TQFP, Pb-free and non Pb-free 119-ball BGA package, and 165-ball FBGA package
- "ZZ" sleep mode option and stop clock option
- Available in Industrial and commercial temperature ranges

Functional Description

The CY7C1347G[1] is a 3.3 V, 128 K × 36 synchronous pipelined SRAM designed to support zero-wait-state secondary cache with minimal glue logic. CY7C1347G I/O pins can operate at either the 2.5 V or the 3.3 V level. The I/O pins are 3.3 V tolerant when V_{DDQ} = 2.5 V. All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 2.6 ns (250 MHz device). CY7C1347G supports either the interleaved burst sequence used by the Intel Pentium processor or a linear burst sequence used by processors such as the PowerPC. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the address strobe from processor ($\overline{ADSP}$) or the address strobe from controller ($\overline{ADSC}$) at clock rise. Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the four Byte Write Select ($\overline{BW}_{[A:D]}$) inputs. A global write enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self timed write circuitry.

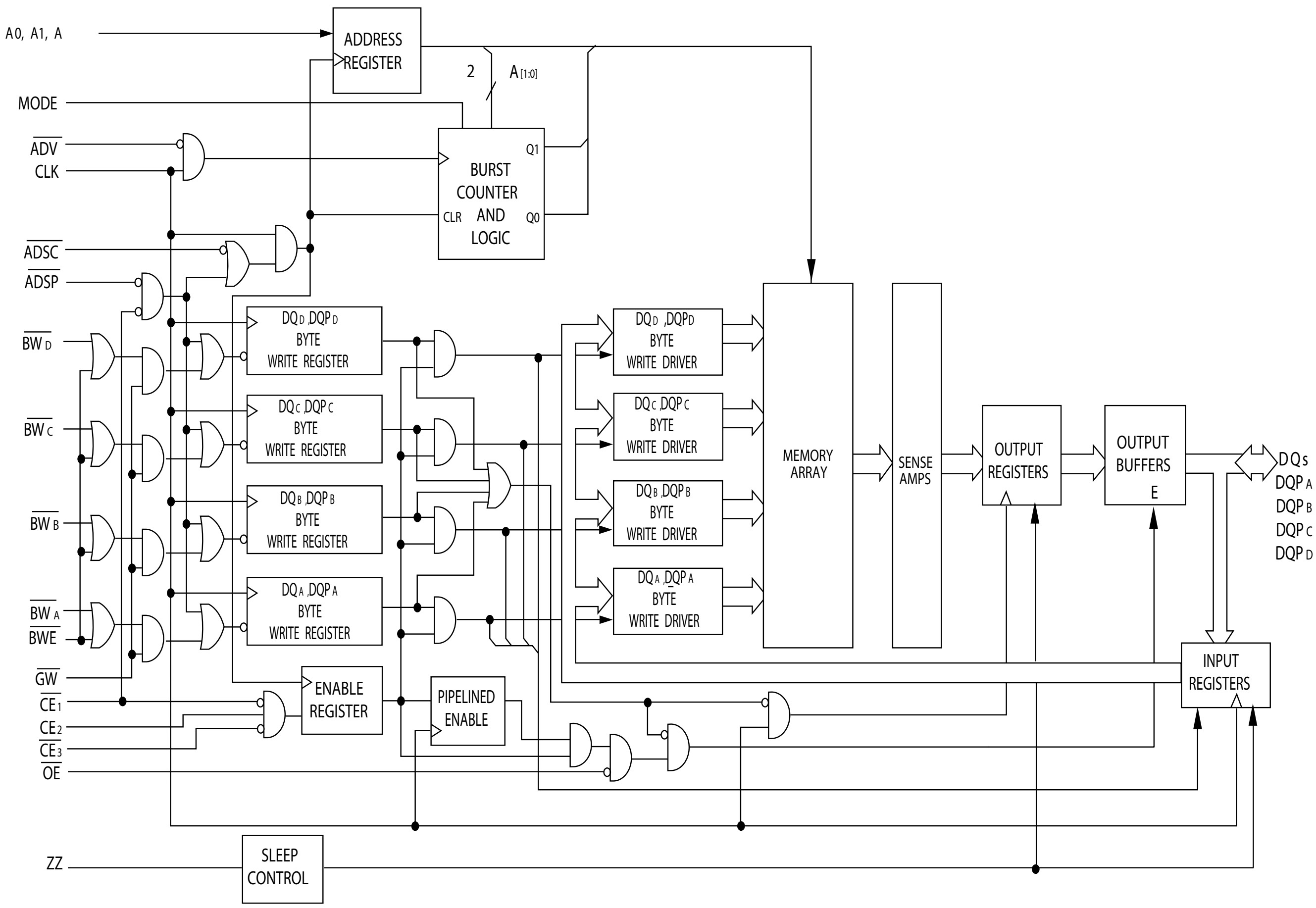
Three synchronous chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tristate control. To provide proper data during depth expansion, $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.

Selection Guide

Description	250 MHz	200 MHz	166 MHz	133 MHz	Unit
Maximum access time	2.6	2.8	3.5	4.0	ns
Maximum operating current	325	265	240	225	mA
Maximum CMOS standby current	40	40	40	40	mA

Note
1. For best practice recommendations, refer to the Cypress application note, SRAM System Guidelines – AN1064.

Logic Block Diagram



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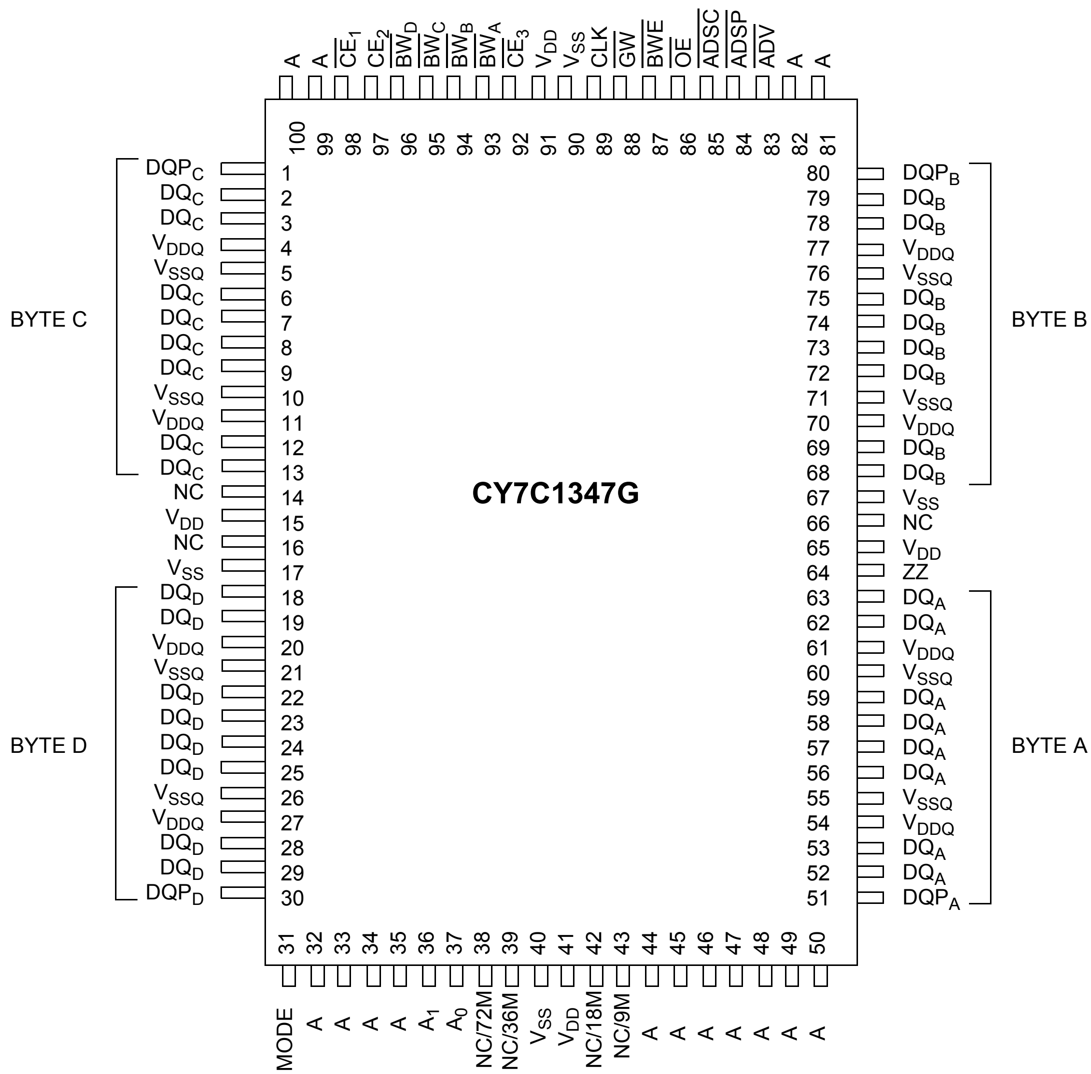
Pin Configurations

Figure 1. 100-pin TQFP Pinout



Pin Configurations (continued)

Figure 2. 119-ball BGA Pinout

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC/288 M	CE_2	A	$\overline{ADSC}$	A	$\overline{CE_3}$	NC/576 M
C	NC/144 M	A	A	V_{DD}	A	A	NC/1G
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE_1}$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW_C}$	$\overline{ADV}$	$\overline{BW_B}$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW_D}$	NC	$\overline{BW_A}$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BWE}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Figure 3. 165-ball FBGA Pinout

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288 M	A	$\overline{CE1}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{CE_3}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144 M	A	CE2	$\overline{BW_D}$	$\overline{BW_A}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576 M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	NC/18M	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72 M	A	A	NC	A1	NC	A	A	A	NC/9 M
R	MODE	NC/36 M	A	A	NC	A0	NC	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0,A_1,A	Input-Synchronous	**Address Inputs Used to Select One of the 128 K Address Locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feeds the 2-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, Active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input Signal, Sampled on the Rising Edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, Sampled on the Rising Edge of CLK**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, Sampled on the Rising Edge of CLK**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non-time-critical "sleep" condition with data integrity preserved. During normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull-down.
DQ_A, DQ_B, DQ_C, DQ_D, DQP_A, DQP_B, DQP_C, DQP_D	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQPs are placed in a tristate condition.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O circuitry**.
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**.
MODE	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DDQ} or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull-up.

Pin Definitions (continued)

Name	I/O	Description
NC, NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**No Connects**. Not internally connected to the die. NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, and NC/1G are address expansion pins that are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.6 ns (250 MHz device).

The CY7C1347G supports secondary cache in systems using either a linear or interleaved burst sequence. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Address Strobe from Processor (ADSP) or the Address Strobe from Controller (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ($BW_{[A:D]}$) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable (OE) provide for easy bank selection and output tristate control. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (3) the write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs ($A_{[16:0]}$) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the Output Register and onto the data bus within 2.6 ns (250 MHz device) if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tristated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single read cycles are supported. After the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output tristates immediately.

Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active. The address presented to $A_{[16:0]}$ is loaded into the Address Register and the address advancement logic while being delivered to the RAM core. The write signals (GW, BWE, and $BW_{[A:D]}$) and ADV inputs are ignored during this first cycle.

ADSP-triggered write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQs and DQPs inputs is written into the corresponding address location in the RAM core. If GW is HIGH, then the write operation is controlled by BWE and $BW_{[A:D]}$ signals. The CY7C1347G provides byte write capability that is described in Partial Truth Table for Read/Write on page 10. Asserting the Byte Write Enable input (BWE) with the selected Byte Write ($BW_{[A:D]}$) input selectively writes to only the desired bytes.

Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism is provided to simplify the write operations.

Because the CY7C1347G is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs and DQPs inputs. Doing so tristates the output drivers. As a safety precaution, DQs and DQPs are automatically tristated whenever a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (4) the appropriate combination of the write inputs (GW, BWE, and $BW_{[A:D]}$) are asserted active to conduct a write to the desired byte(s). ADSC-triggered write accesses require a single clock cycle to complete. The address presented to $A_{[16:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The ADV input is ignored during this cycle. If a global write is conducted, the data presented to the DQs and DQPs is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations.

Because the CY7C1347G is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs and DQPs inputs. Doing so tristates the output drivers. As a safety precaution, DQs and DQPs are automatically tristated whenever a write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1347G provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user-selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the "sleep" mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	40	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ Active to snooze current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit snooze current	This parameter is sampled	0	–	ns

Truth Table

The truth table for part number CY7C1347G follow. [2, 3, 4, 5, 6]

Next Cycle	Add. Used	$\overline{CE}_1$	CE_2	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	X	H	L	H	L	X	X	X	L-H	Tristate

Notes

2. X = "Do not Care." H = Logic HIGH, L = Logic LOW.
3. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals ($\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals ($\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$), $\overline{BWE}$, $\overline{GW}$ = H.
4. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{[A:D]}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH before the start of the write cycle to allow the outputs to tristate. $\overline{OE}$ is a do not care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table (continued)

The truth table for part number CY7C1347G follow. [2, 3, 4, 5, 6]

Next Cycle	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Snooze mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tristate
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tristate
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tristate
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tristate
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tristate
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tristate
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Partial Truth Table for Read/Write

The partial truth table for read/write for part number CY7C1347G follow. [7, 8]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A – DQ_A	H	L	H	H	H	L
Write byte B – DQ_B	H	L	H	H	L	H
Write bytes B, A	H	L	H	H	L	L
Write byte C – DQ_C	H	L	H	L	H	H
Write bytes C, A	H	L	H	L	H	L
Write bytes C, B	H	L	H	L	L	H
Write bytes C, B, A	H	L	H	L	L	L
Write byte D – DQ_D	H	L	L	H	H	H
Write bytes D, A	H	L	L	H	H	L
Write bytes D, B	H	L	L	H	L	H
Write bytes D, B, A	H	L	L	H	L	L
Write bytes D, C	H	L	L	L	H	H
Write bytes D, C, A	H	L	L	L	H	L
Write bytes D, C, B	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

Notes
7. X = “Do not Care.” H = Logic HIGH, L = Logic LOW.
8. This table is only a partial listing of the byte write combinations. Any combination of BW_x is valid. Appropriate write is based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND .... –0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND .... –0.5 V to $+V_{DD}$

DC voltage applied to outputs in high Z State .... –0.5 V to V_{DD} + 0.5 V

DC input voltage .... –0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage .... > 2001 V (MIL-STD-883, Method 3015)

Latch-up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	361	394	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch-up	85 °C	0	0.1	FIT/Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note, Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates – AN54908.

Electrical Characteristics

Over the Operating Range[9, 10]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage		3.135	3.6	V
V_{DDQ}	I/O supply voltage		2.375	V_{DD}	V
V_{OH}	Output HIGH voltage	For 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		For 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW voltage	For 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		For 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage[9]	For 3.3 V I/O	2.0	V_{DD} + 0.3 V	V
		For 2.5 V I/O	1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[9]	For 3.3 V I/O	–0.3	0.8	V
		For 2.5 V I/O	–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input current of MODE	Input = V_{SS}	–30	–	µA
		Input = V_{DD}	–	5	µA
	Input current of ZZ	Input = V_{SS}	–5	–	µA
		Input = V_{DD}	–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ $V_{DDQ,}$ output disabled	–5	5	µA

Notes
9. Overshoot: $V_{IH}(AC) < V_{DD}$ +1.5 V (pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL}(AC) > -2$ V (pulse width less than $t_{CYC}/2$).
10. $t_{power-up}$: assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Electrical Characteristics (continued)

Over the Operating Range[9, 10]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{DD}	V_{DD} operating supply current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz	–	325	mA
			5 ns cycle, 200 MHz	–	265	mA
			6 ns cycle, 166 MHz	–	240	mA
			7.5 ns cycle, 133 MHz	–	225	mA
I_{SB1}	Automatic CE power-down current—TTL inputs	Max. V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz	–	120	mA
			5 ns cycle, 200 MHz	–	110	mA
			6 ns cycle, 166 MHz	–	100	mA
			7.5 ns cycle, 133 MHz	–	90	mA
I_{SB2}	Automatic CE power-down current—CMOS inputs	Max. V_{DD}, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = 0	All speeds	–	40	mA
I_{SB3}	Automatic CE power-down current—CMOS inputs	Max. V_{DD}, device deselected, or $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz	–	105	mA
			5 ns cycle, 200 MHz	–	95	mA
			6 ns cycle, 166 MHz	–	85	mA
			7.5 ns cycle, 133 MHz	–	75	mA
I_{SB4}	Automatic CE power-down current—TTL inputs	Max. V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0		–	45	mA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

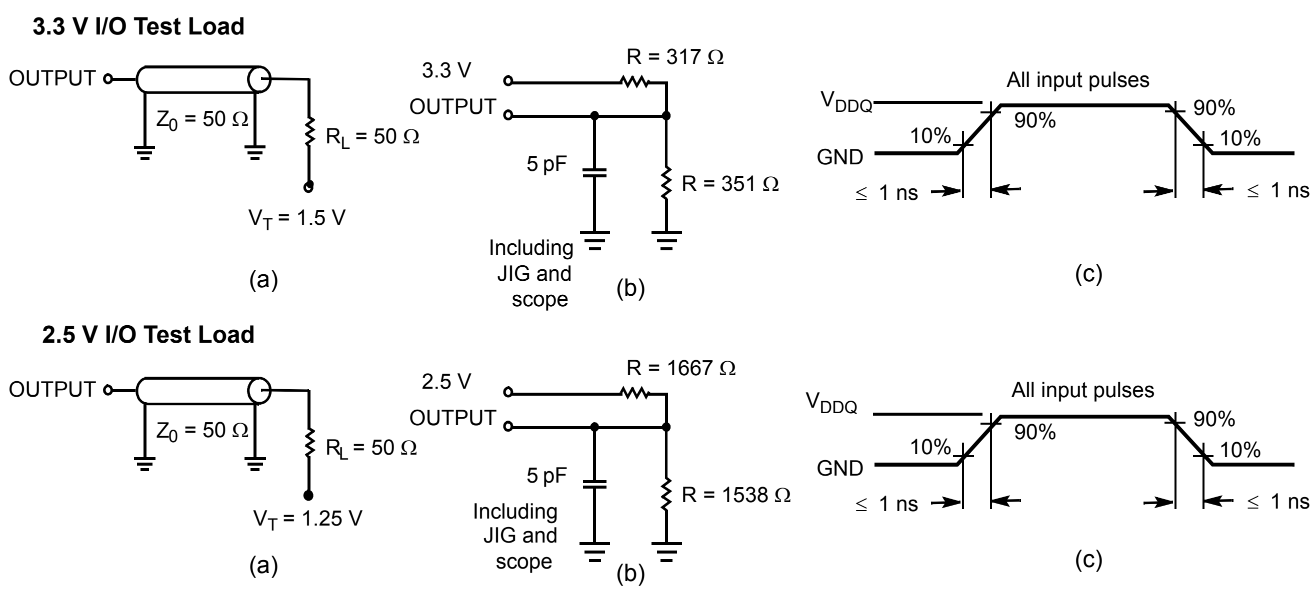
Parameter	Description	Test Conditions	100-pin TQFP Max	119-ball BGA Max	165-ball FBGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V. V_{DDQ} = 3.3 V	5	5	5	pF
C_{CLK}	Clock input capacitance		5	5	5	pF
C_{IO}	I/O capacitance		5	7	7	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	100-pin TQFP Package	119-ball BGA Package	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	30.32	34.1	20.3	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.85	14.0	4.6	°C/W

Figure 4. AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range[11, 12]

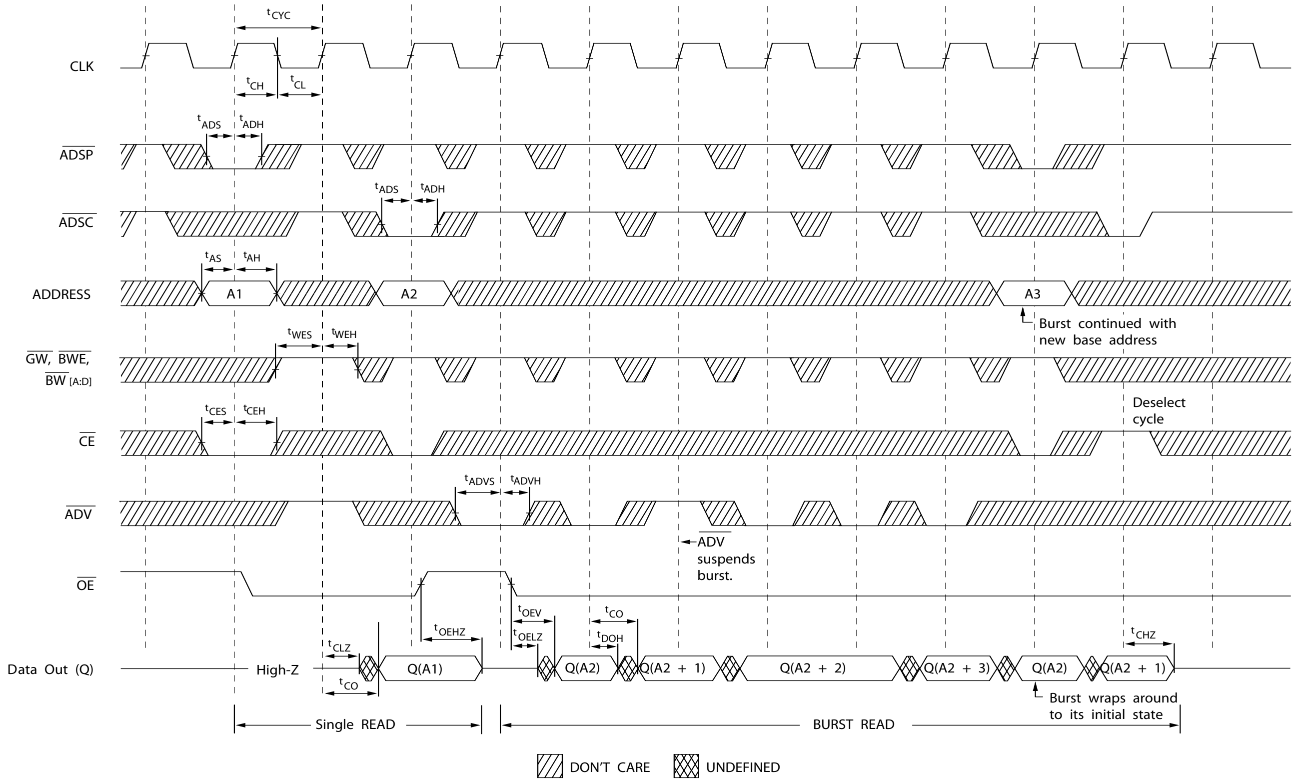
Parameter	Description	–250		–200		–166		–133		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{POWER}	V_{DD}(Typical) to the first Access[13]	1	–	1	–	1	–	1	–	ms
Clock										
t_{CYC}	Clock cycle time	4.0	–	5.0	–	6.0	–	7.5	–	ns
t_{CH}	Clock HIGH	1.7	–	2.0	–	2.5	–	3.0	–	ns
t_{CL}	Clock LOW	1.7	–	2.0	–	2.5	–	3.0	–	ns
Output Times										
t_{CO}	Data output valid after CLK rise	–	2.6	–	2.8	–	3.5	–	4.0	ns
t_{DOH}	Data output hold after CLK rise	1.0	–	1.0	–	1.5	–	1.5	–	ns
t_{CLZ}	Clock to low Z[14, 15, 16]	0	–	0	–	0	–	0	–	ns
t_{CHZ}	Clock to high Z[14, 15, 16]	–	2.6	–	2.8	–	3.5	–	4.0	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	2.6	–	2.8	–	3.5	–	4.5	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z[14, 15, 16]	0	–	0	–	0	–	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z[14, 15, 16]	–	2.6	–	2.8	–	3.5	–	4.0	ns
Setup Times										
t_{AS}	Address setup before CLK rise	1.2	–	1.2	–	1.5	–	1.5	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ setup before CLK rise	1.2	–	1.2	–	1.5	–	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ setup before CLK rise	1.2	–	1.2	–	1.5	–	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ setup before CLK rise	1.2	–	1.2	–	1.5	–	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.2	–	1.2	–	1.5	–	1.5	–	ns
t_{CES}	Chip enable setup before CLK rise	1.2	–	1.2	–	1.5	–	1.5	–	ns
Hold Times										
t_{AH}	Address hold after CLK rise	0.3	–	0.5	–	0.5	–	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.3	–	0.5	–	0.5	–	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK Rise	0.3	–	0.5	–	0.5	–	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ hold after CLK rise	0.3	–	0.5	–	0.5	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.3	–	0.5	–	0.5	–	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.3	–	0.5	–	0.5	–	0.5	–	ns

Notes

11. Timing references level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V on all datasheets.
12. Test conditions shown in (a) of Figure 4 on page 13 unless otherwise noted.
13. This part has an internal voltage regulator; t_{POWER} is the time that the power must be supplied above V_{DD}(min) initially before a read or write operation can be initiated.
14. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 4 on page 13. Transition is measured ±200 mV from steady-state voltage.
15. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z before Low Z under the same system conditions.
16. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 5. Read Cycle Timing[17]

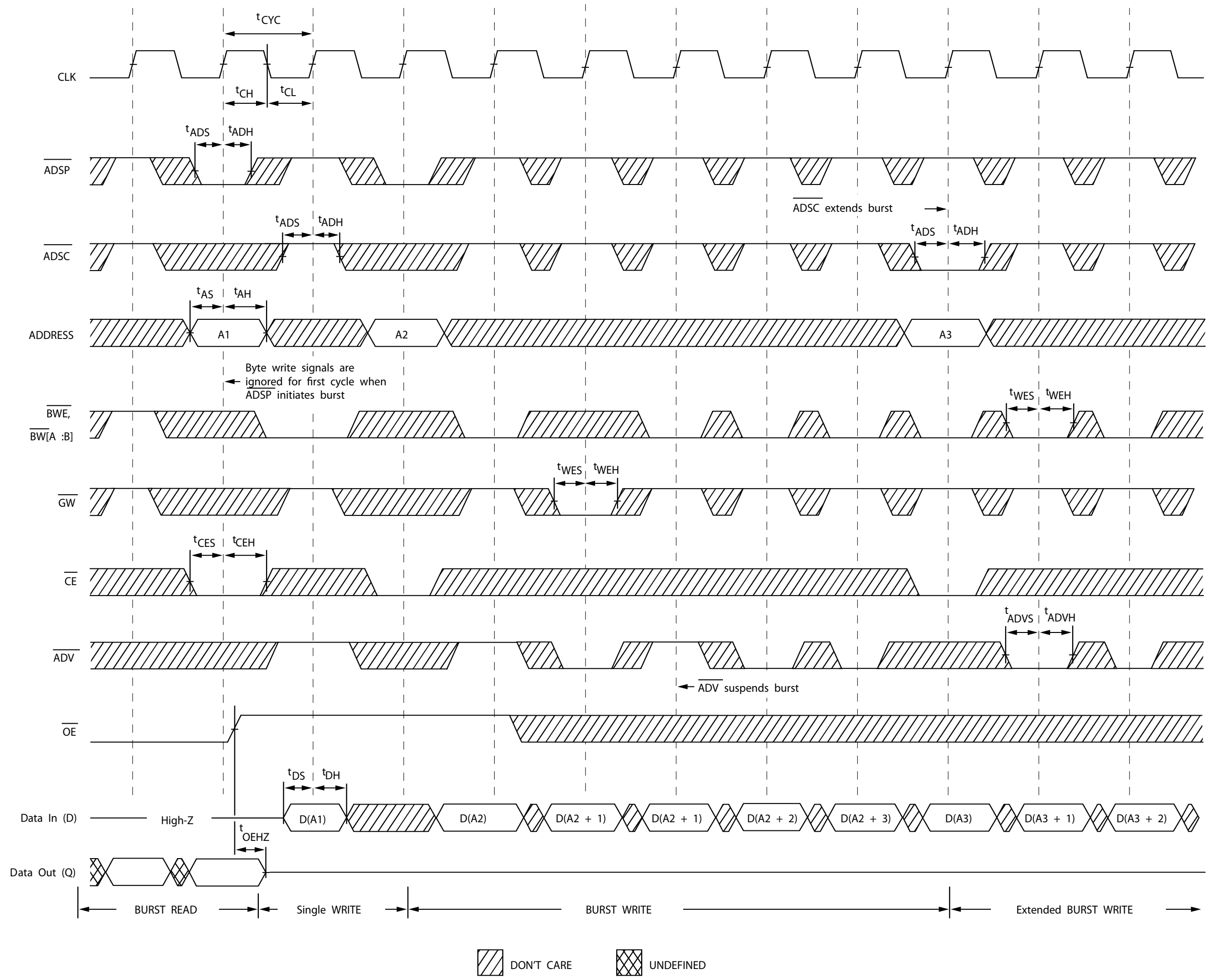


Note

17. In this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle Timing[18, 19]

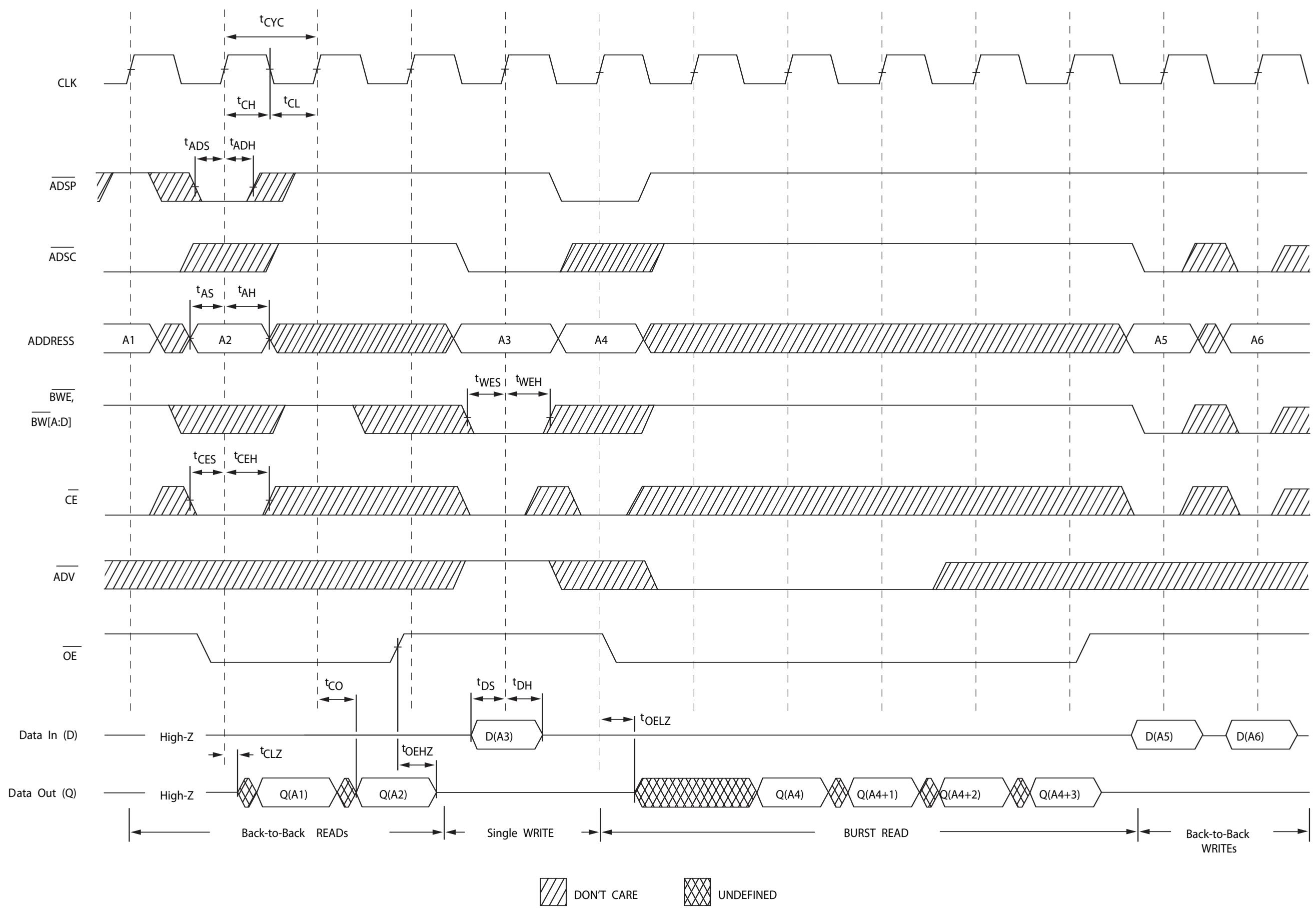


Notes

18. In this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.
19. Full width write can be initiated by either $\overline{GW}$ LOW, or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and BW_x LOW.

Switching Waveforms (continued)

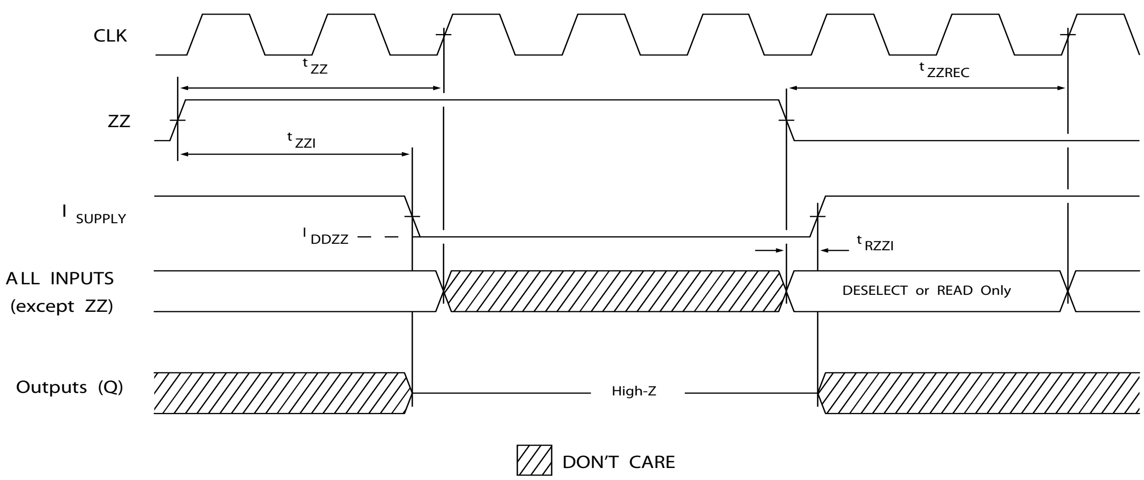
Figure 7. Read/Write Cycle Timing[20, 21, 22]



Notes
20. In this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.
21. The data bus (Q) remains in High Z following a write cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
22. $\overline{GW}$ is HIGH.

Switching Waveforms (continued)

Figure 8. ZZ Mode Timing[23, 24]



Notes

23. Device must be deselected when entering ZZ mode. See Truth Table on page 8 for all possible signal conditions to deselect the device.
24. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C1347G-133AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1347G-133BGXC	51-85115	119-ball Ball Grid Array (14 × 22 × 2.4 mm) Pb-free	
166	CY7C1347G-166AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial
200	CY7C1347G-200AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial
250	CY7C1347G-250AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial

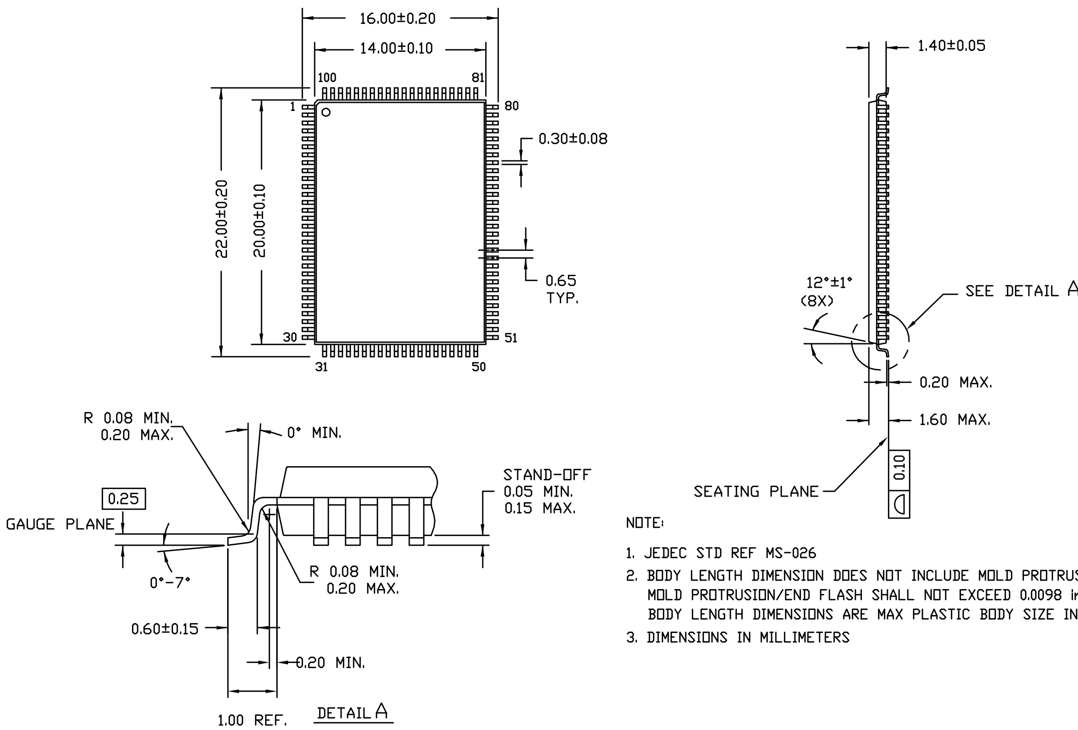
Ordering Code Definitions

CY 7C 1347 G - XXX XXX C

- Temperature range:
  C = Commercial
- Package Type:
  AX = 100-pin TQFP (Pb-free)
  BGX = 119-ball BGA (Pb-free)
- Speed Grade: XXX = 133 MHz or 166 MHz or 200 MHz or 250 MHz
- Process Technology ≥ 90 nm
- 1347 = SCD, 128 K × 36 (4 Mb)
- Marketing Code: 7C = SRAMs
- Company ID: CY = Cypress

Package Diagrams

Figure 9. 100-pin TQFP (14 × 20 × 1.4 mm)



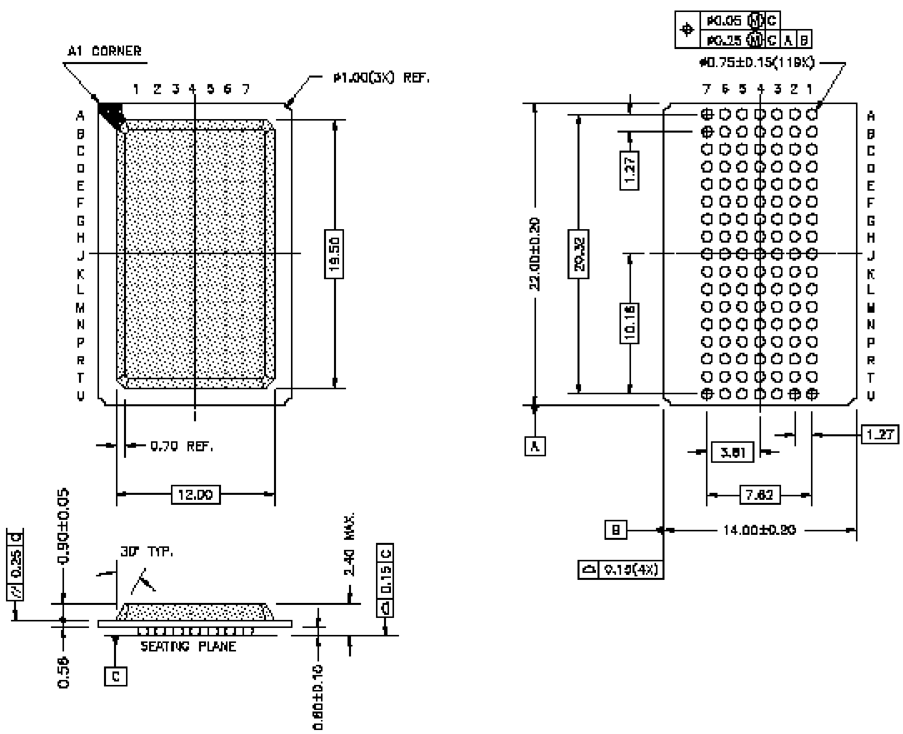
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *D

Package Diagrams (continued)

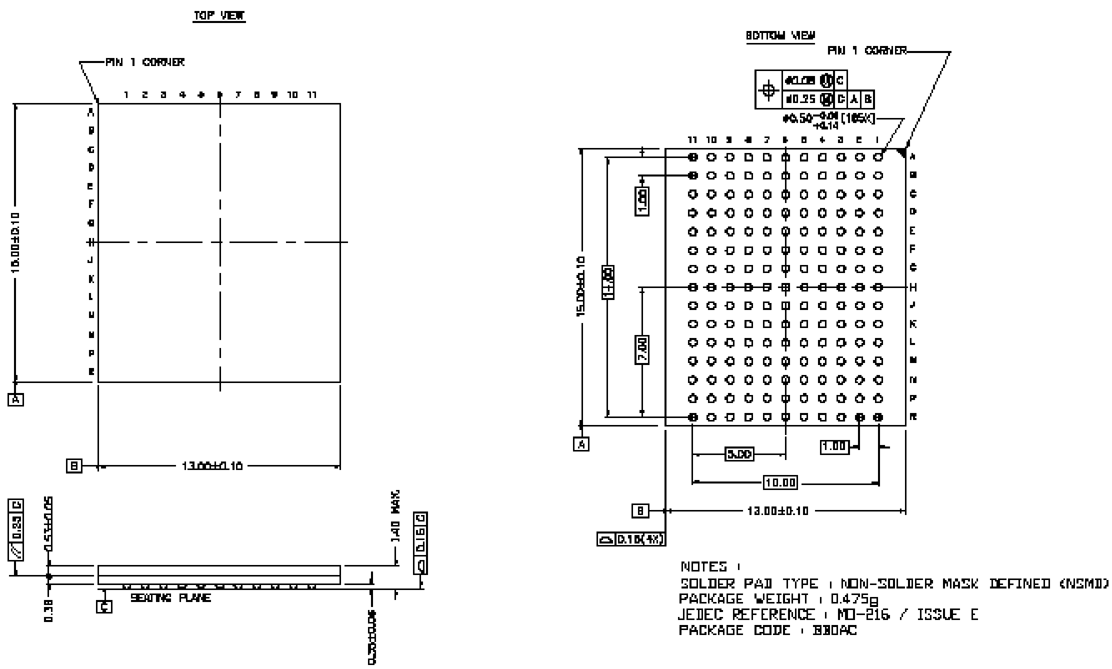
Figure 10. 119-ball BGA (14 × 22 × 2.4 mm)



51-85115 *C

Package Diagrams (continued)

Figure 11. 165-ball FBGA (13 × 15 × 1.4 mm)



51-85180 *C

Acronyms

Acronym	Description
DDR	double data rate
FBGA	fine-pitch ball grid array
HSTL	high-speed transceiver logic
JEDEC	joint electron device engineering council
JTAG	joint test action group
ODT	on-die termination
PLL	phase-locked loop
QDR	quad data rate
TAP	test access port
TCK	test clock
TDO	test data out
TDI	test data in
TMS	test mode select

Document History Page

Document Title: CY7C1347G 4-Mbit (128 K × 36) Pipelined Sync SRAM Document Number: 38-05516				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	224364	RKF	See ECN	New datasheet
*A	276690	VBL	See ECN	Changed TQFP package in Ordering Information section to Pb-Free TQFP Added comment of BG and BZ Pb-Free package availability
*B	333625	SYT	See ECN	Removed 225 MHz and 100 MHz speed grades Modified Address Expansion balls in the pinouts for 100 TQFP Package as per JEDEC standards and updated the Pin Definitions accordingly Modified $V_{OL,}$ V_{OH} test conditions Replaced TBDs for Θ_{JA} and Θ_{JC} to their respective values on the Thermal Resistance table Changed the package name for 100 TQFP from A100RA to A101 Removed comment on the availability of BG Pb-Free package Updated the Ordering Information by shading and unshading MPNs as per availability
*C	419256	RXU	See ECN	Converted from Preliminary to Final. Changed address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Swapped typo CE_2 and $\overline{CE}_3$ in the Truth Table column heading on Page #6 Modified test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD.}$ Modified test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$ Modified “Input Load” to “Input Leakage Current except ZZ and MODE” in the Electrical Characteristics Table. Replaced Package Name column with Package Diagram in the Ordering Information table. Replaced Package Diagram of 51-85050 from *A to *B Replaced Package Diagram of 51-85180 from ** to *A Updated the Ordering Information.
*D	480124	VKN	See ECN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND. Updated the Ordering Information table.
*E	1078184	VKN	See ECN	Corrected write timing diagram on page 12
*F	2633279	NXR/AESA	01/15/09	Updated Ordering Information and data sheet template.
*G	2756998	VKN	08/28/09	Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information. Updated Package Diagram for spec 51-85180.
*H	2998771	NJY	08/02/10	Template update. Updated package diagrams to latest revision. 51-85050 – *B to *C 51-85115 – *B to *C 51-85180 – *B to *C
*I	3208774	NJY	03/29/2011	Updated Ordering Information and added Ordering Code Definitions. Updated Package Diagrams.

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