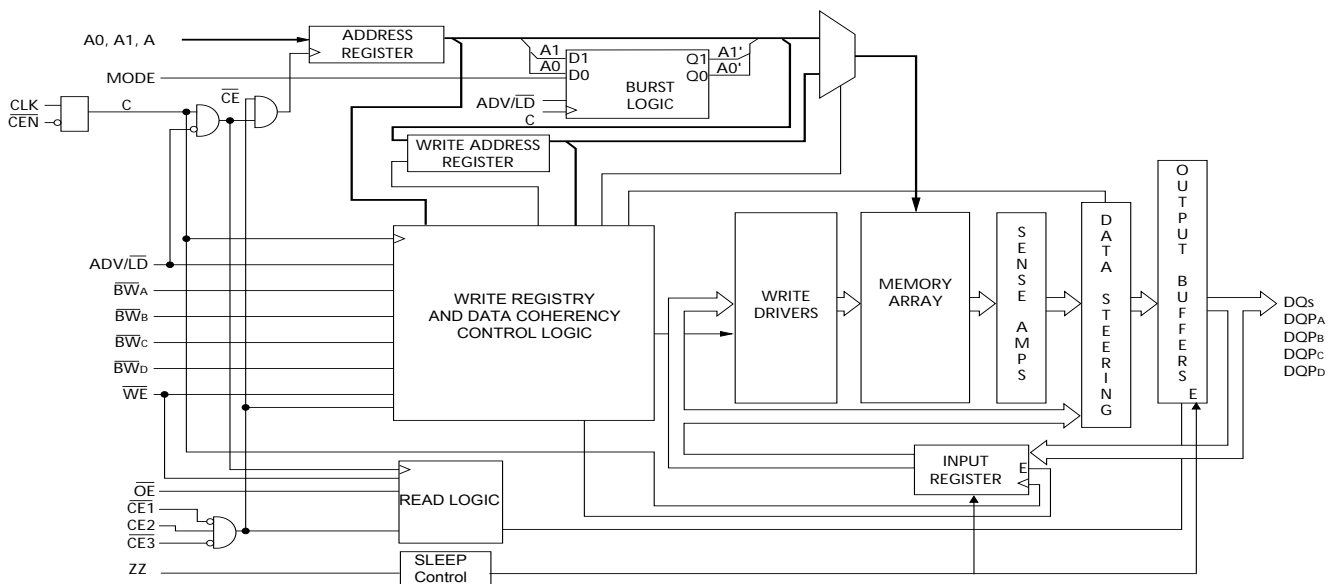# 4-Mbit (128 K × 36) Flow-through SRAM with NoBL™ Architecture

Features

- Can support up to 133-MHz bus operations with zero wait states
  - Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self-timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow-through operation
- Byte write capability
- 128 K × 36 common I/O architecture
- 2.5 V/3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock enable ($\overline{CEN}$) pin to suspend operation
- Synchronous self-timed writes
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package, Pb-free and non Pb-free 119-ball BGA package
- Burst capability—linear or interleaved burst order
- Low standby power

Functional Description

The CY7C1351G[1] is a 3.3 V, 128 K × 36 synchronous flow-through burst SRAM designed specifically to support unlimited true back-to-back read/write operations without the insertion of wait states. The CY7C1351G is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable (CEN) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

Write operations are controlled by the four byte write select ($\overline{BW}_{[A:D]}$) and a write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. In order to avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

Logic Block Diagram

Note

1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.
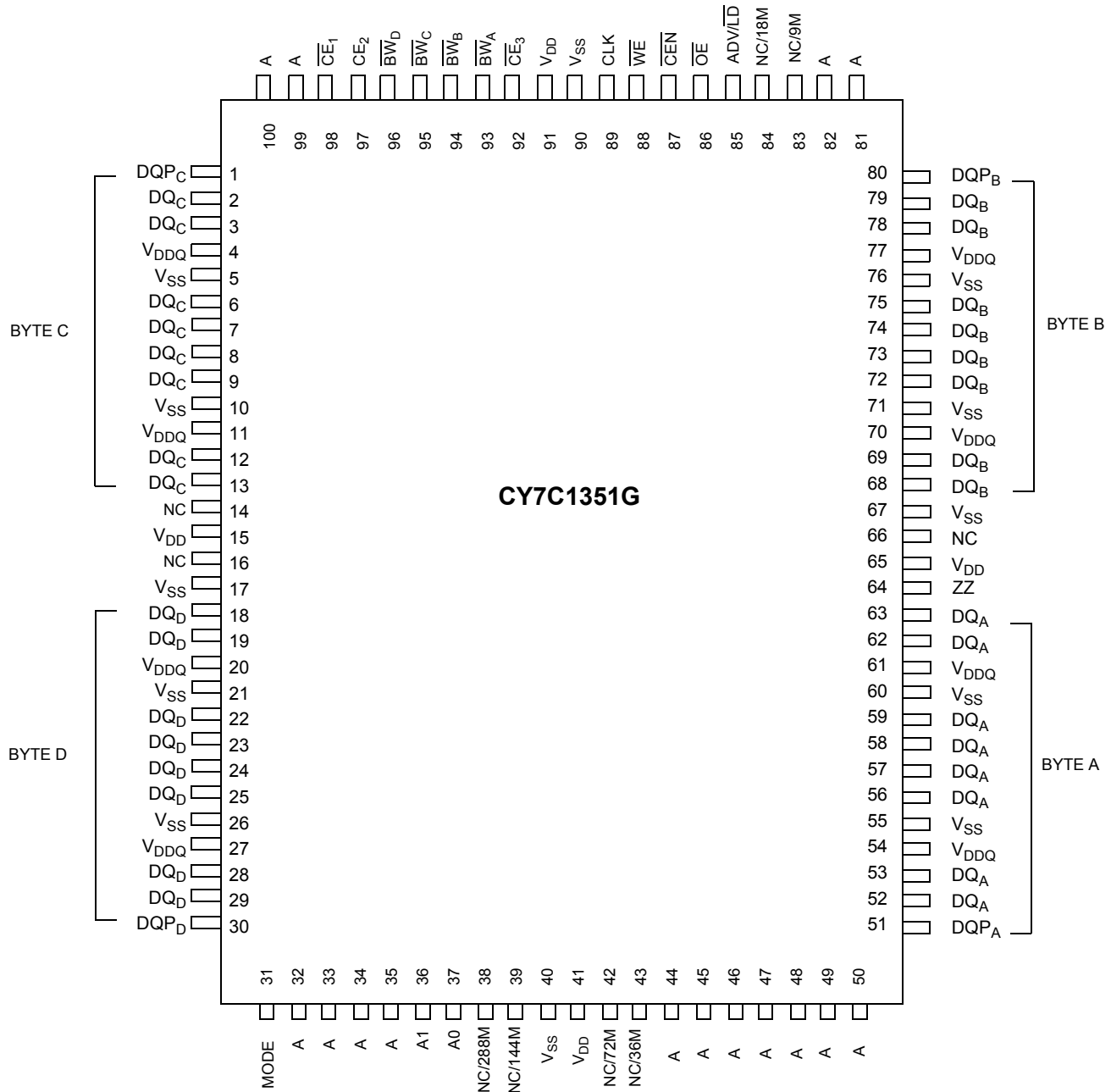
[+] Feedback

Contents

Selection Guide

	133 MHz	100 MHz	Unit
Maximum access time	6.5	8.0	ns
Maximum operating current	225	205	mA
Maximum CMOS standby current	40	40	mA

Pin Configurations

100-pin TQFP Pinout

[+] Feedback

Pin Configurations *(continued)*

119-ball BGA Pinout

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC/18M	A	A	V_{DDQ}
B	NC/576M	CE_2	A	$ADV/\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE_1}$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW}_C$	NC/9M	$\overline{BW}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{WE}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW}_D$	NC	$\overline{BW}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{CEN}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the 128 K address locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_{[A:D]}$	Input-synchronous	**Byte write inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-synchronous	**Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
$ADV/\overline{LD}$	Input-synchronous	**Advance/load input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, $ADV/\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE_1}$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2, and $\overline{CE_3}$ to select/deselect the device.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device.
$\overline{CE_3}$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-asynchronous	**Output enable, asynchronous input, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.

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Pin Definitions *(continued)*

Name	I/O	Description
$\overline{CEN}$	Input-synchronous	**Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
ZZ	Input-asynchronous	**ZZ "sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin has to be low or left floating. ZZ pin has an internal pull-down.
DQ_s	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by address during the clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_s and $DQP_{[A:D]}$ are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
$DQP_{[A:D]}$	I/O-synchronous	**Bidirectional data parity I/O lines**. Functionally, these signals are identical to DQ_s. During write sequences, $DQP_{[A:D]}$ is controlled by $\overline{BW}_{[A:D]}$ correspondingly.
MODE	Input strap pin	**Mode input. Selects the burst order of the device**. When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**.
NC	–	**No connects**. Not Internally connected to the die.
NC/9M, NC/18M NC/36M NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**No connects**. Not internally connected to the die. NC/9M,NC/18M,NC/36M,NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins are not internally connected to the die.

Functional Overview

The CY7C1351G is a synchronous flow-through burst SRAM designed specifically to eliminate wait states during write-read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If clock enable (CEN) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the write enable (WE). $BW_{[A:D]}$ can be used to conduct byte write operations.

Write operations are qualified by the write enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$

should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, (3) the write enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (read/write/deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output will be tri-stated immediately.

Burst Read Accesses

The CY7C1351G has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four

reads without reasserting the address inputs. ADV/$\overline{\text{LD}}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Accesses section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap around when incremented sufficiently. A HIGH input on ADV/LD will increment the internal burst counter regardless of the state of chip enable inputs or $\overline{\text{WE}}$. $\overline{\text{WE}}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{\text{CEN}}$ is asserted LOW, (2) $\overline{\text{CE}_1}$, CE_2, and $\overline{\text{CE}_3}$ are all asserted active, and (3) the write signal $\overline{\text{WE}}$ is asserted LOW. The address presented to the address bus is loaded into the address register. The write signals are latched into the control logic block. The data lines are automatically tri-stated regardless of the state of the $\overline{\text{OE}}$ input signal. This allows the external logic to present the data on DQs and $\text{DQP}_{[A:D]}$.

On the next clock rise the data presented to DQs and $\text{DQP}_{[A:D]}$ (or a subset for byte write operations, see truth table for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by $\text{BW}_{[A:D]}$ signals. The CY7C1351G provides byte write capability that is described in the truth table. Asserting the write enable input ($\overline{\text{WE}}$) with the selected byte write select input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1351G is a common I/O device, data should not be driven into the device while the outputs are active. The output enable ($\overline{\text{OE}}$) can be deasserted HIGH before presenting data to the DQs and $\text{DQP}_{[A:D]}$ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs and $\text{DQP}_{[A:D]}$ are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{\text{OE}}$.

Burst Write Accesses

The CY7C1351G has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/LD must be driven LOW in order to load the initial address, as described in the Single Write Accesses section above. When ADV/$\overline{\text{LD}}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{\text{CE}_1}$, CE_2, and $\overline{\text{CE}_3}$) and $\overline{\text{WE}}$ inputs are ignored and the burst counter is incremented. The correct $\overline{\text{BW}}_{[A:D]}$ inputs must be driven in each cycle of the burst write, in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{\text{CE}_1}$, CE_2, and $\overline{\text{CE}_3}$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Linear Burst Address Table (MODE = GND)

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD}$ – 0.2 V	–	40	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD}$ – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

[+] Feedback

Truth Table [2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$ADV/\overline{LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-state
Deselect cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-state
Deselect cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-state
Continue deselect cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-state
READ cycle (begin burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data out (Q)
READ cycle (continue burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data out (Q)
NOP/DUMMY READ (begin burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-state
DUMMY READ (continue burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-state
WRITE cycle (begin burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data in (D)
WRITE cycle (continue burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data in (D)
NOP/WRITE ABORT (begin burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-state
WRITE ABORT (continue burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-state
IGNORE CLOCK EDGE (stall)	Current	X	X	X	L	X	X	X	X	H	L->H	–
SLEEP MODE	None	X	X	X	H	X	X	X	X	X	X	Tri-state

Partial Truth Table for Read/Write [2, 3, 9]

Function	$\overline{WE}$	$\overline{BW_A}$	$\overline{BW_B}$	$\overline{BW_C}$	$\overline{BW_D}$
Read	H	X	X	X	X
Read	H	X	X	X	X
Write – no bytes written	L	H	H	H	H
Write byte A – (DQ_A and DQP_A)	L	L	H	H	H
Write byte B – (DQ_B and DQP_B)	L	H	L	H	H
Write byte C – (DQ_C and DQP_C)	L	H	H	L	H
Write byte D – (DQ_D and DQP_D)	L	H	H	H	L
Write all bytes	L	L	L	L	L

Notes
2. X = Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{BW}$x = L signifies at least one byte write select is active, $\overline{BW}$x = valid signifies that the desired byte write selects are asserted, see truth table for details.
3. Write is defined by $\overline{BW_X}$, and $\overline{WE}$. See truth table for read/write.
4. When a write cycle is detected, all I/Os are tri-stated, even during byte writes.
5. The DQs and $DQP_{[A:D]}$ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. $\overline{CEN}$ = H, inserts wait states.
7. Device will power-up deselected and the I/Os in a tri-state condition, regardless of $\overline{OE}$.
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and $DQP_{[A:D]}$ = tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and $DQP_{[A:D]}$ = data when $\overline{OE}$ is active.
9. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write will be done based on which byte write is active.

[+] Feedback

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with
power applied .... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND ....–0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND .... –0.5 V to +V_{DD}

DC voltage applied to outputs
in tri-state ....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage .... –0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage.. > 2001 V
(per MIL-STD-883, method 3015)

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range [10,11]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL}= 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL}= 1.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
	Input HIGH voltage	for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[10]	for 3.3 V I/O		–0.3	0.8	V
	Input LOW voltage[10]	for 2.5 V I/O		–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled		–5	5	µA
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz	–	225	mA
			10-ns cycle, 100 MHz	–	205	mA
I_{SB1}	Automatic CE power-down current—TTL inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	7.5-ns cycle, 133 MHz	–	90	mA
			10-ns cycle, 100 MHz	–	80	mA
I_{SB2}	Automatic CE power-down current—CMOS inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{DD} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0, inputs static	All speeds	–	40	mA
I_{SB3}	Automatic CE power-down current—CMOS inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{DDQ} – 0.3 V or V_{IN} ≤ 0.3 V, f = f_{MAX}, inputs switching	7.5-ns cycle, 133 MHz	–	75	mA
			10-ns cycle, 100 MHz	–	65	mA
I_{SB4}	Automatic CE power-down current—TTL inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0, inputs static	All speeds	–	45	mA

Notes
10. Overshoot: V_{IH}(AC) < V_{DD} +1.5 V (Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC) > –2 V (Pulse width less than t_{CYC}/2).
11. $T_{Power-up}$: Assumes a linear ramp from 0 V to V_{DD} (min.) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance[12]

Parameter	Description	Test Conditions	100 TQFP Max	119 BGA Max	Unit
C_{IN}	Input capacitance	$T_A = 25 \ °C$, f = 1 MHz, $V_{DD} = 3.3 \ V$ $V_{DDQ} = 3.3 \ V$	5	5	pF
C_{CLOCK}	Clock input capacitance		5	5	pF
$C_{I/O}$	I/O capacitance		5	7	pF

Thermal Resistance[12]

Parameters	Description	Test Conditions	100 TQFP Package	119 BGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	30.32	34.1	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.85	14.0	°C/W

AC Test Loads and Waveforms

3.3 V I/O Test Load

(a)

(b)

(c)

2.5 V I/O Test Load

(a)

(b)

(c)
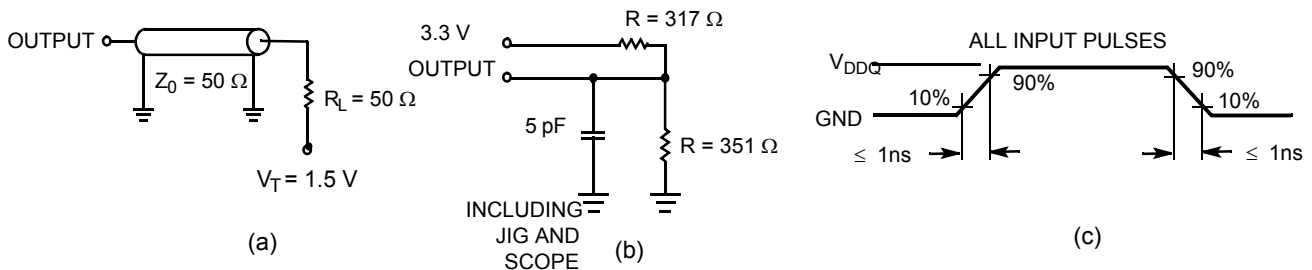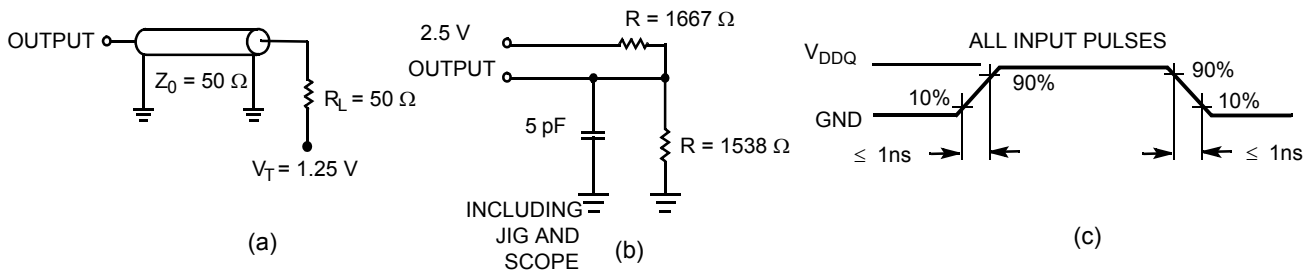
Note
12. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics

Over the Operating Range[13, 14]

Parameter	Description	−133		−100		Unit
		Min	**Max**	**Min**	**Max**	
t_{POWER}	V_{DD}(typical) to the first access[15]	1	–	1	–	ms
Clock						
t_{CYC}	Clock cycle time	7.5	–	10	–	ns
t_{CH}	Clock HIGH	2.5	–	4.0	–	ns
t_{CL}	Clock LOW	2.5	–	4.0	–	ns
Output Times						
t_{CDV}	Data output valid after CLK rise	–	6.5	–	8.0	ns
t_{DOH}	Data output hold after CLK rise	2.0	–	2.0	–	ns
t_{CLZ}	Clock to low Z[16, 17, 18]	0	–	0	–	ns
t_{CHZ}	Clock to high Z[16, 17, 18]	–	3.5	–	3.5	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.5	–	3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z[16, 17, 18]	0	–	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z[16, 17, 18]	–	3.5	–	3.5	ns
Set-up Times						
t_{AS}	Address set-up before CLK rise	1.5	–	2.0	–	ns
t_{ALS}	ADV/$\overline{LD}$ set-up before CLK rise	1.5	–	2.0	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ set-up before CLK rise	1.5	–	2.0	–	ns
t_{CENS}	$\overline{CEN}$ set-up before CLK rise	1.5	–	2.0	–	ns
t_{DS}	Data input set-up before CLK rise	1.5	–	2.0	–	ns
t_{CES}	Chip enable set-up before CLK rise	1.5	–	2.0	–	ns
Hold Times						
t_{AH}	Address hold after CLK rise	0.5	–	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ hold after CLK rise	0.5	–	0.5	–	ns
t_{CENH}	$\overline{CEN}$ hold after CLK rise	0.5	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	0.5	–	ns

Notes
13. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
14. Test conditions shown in (a) of AC Test Loads, unless otherwise noted.
15. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
16. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
17. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve tri-state prior to low Z under the same system conditions.
18. This parameter is sampled and not 100% tested.

Switching Waveforms
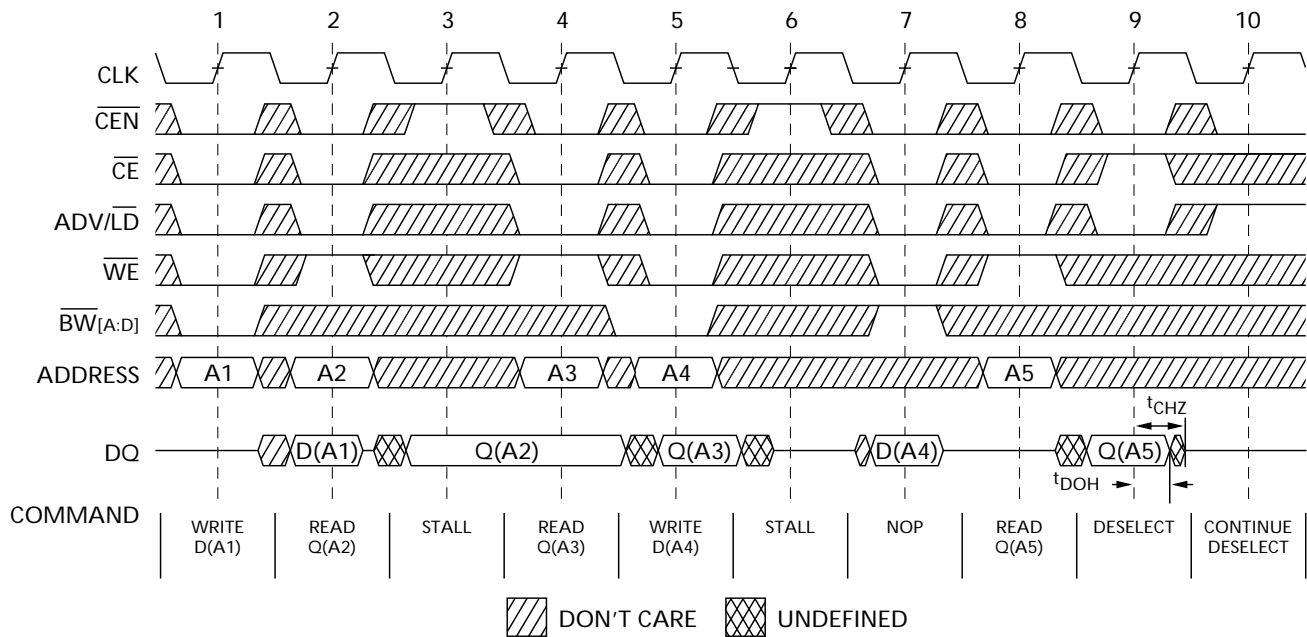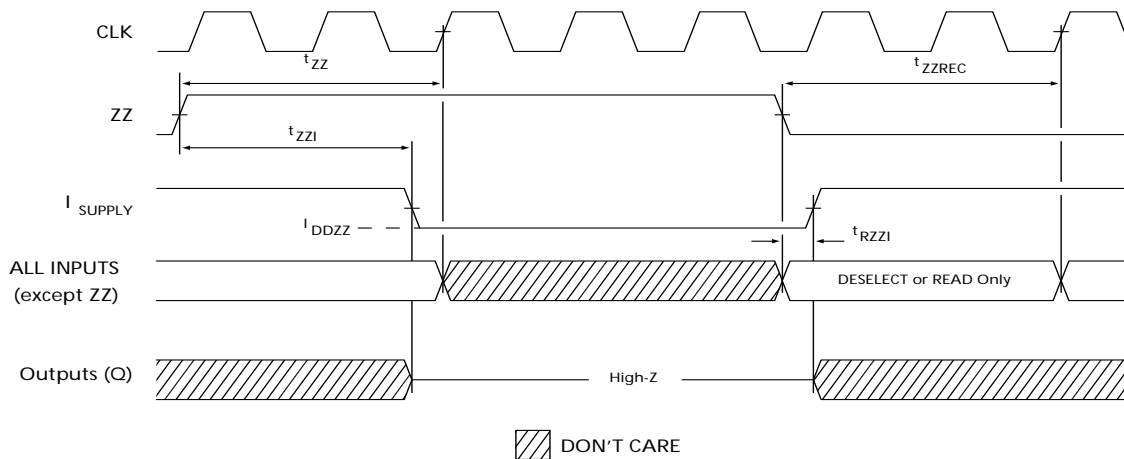
Read/Write Waveforms[19, 20, 21]
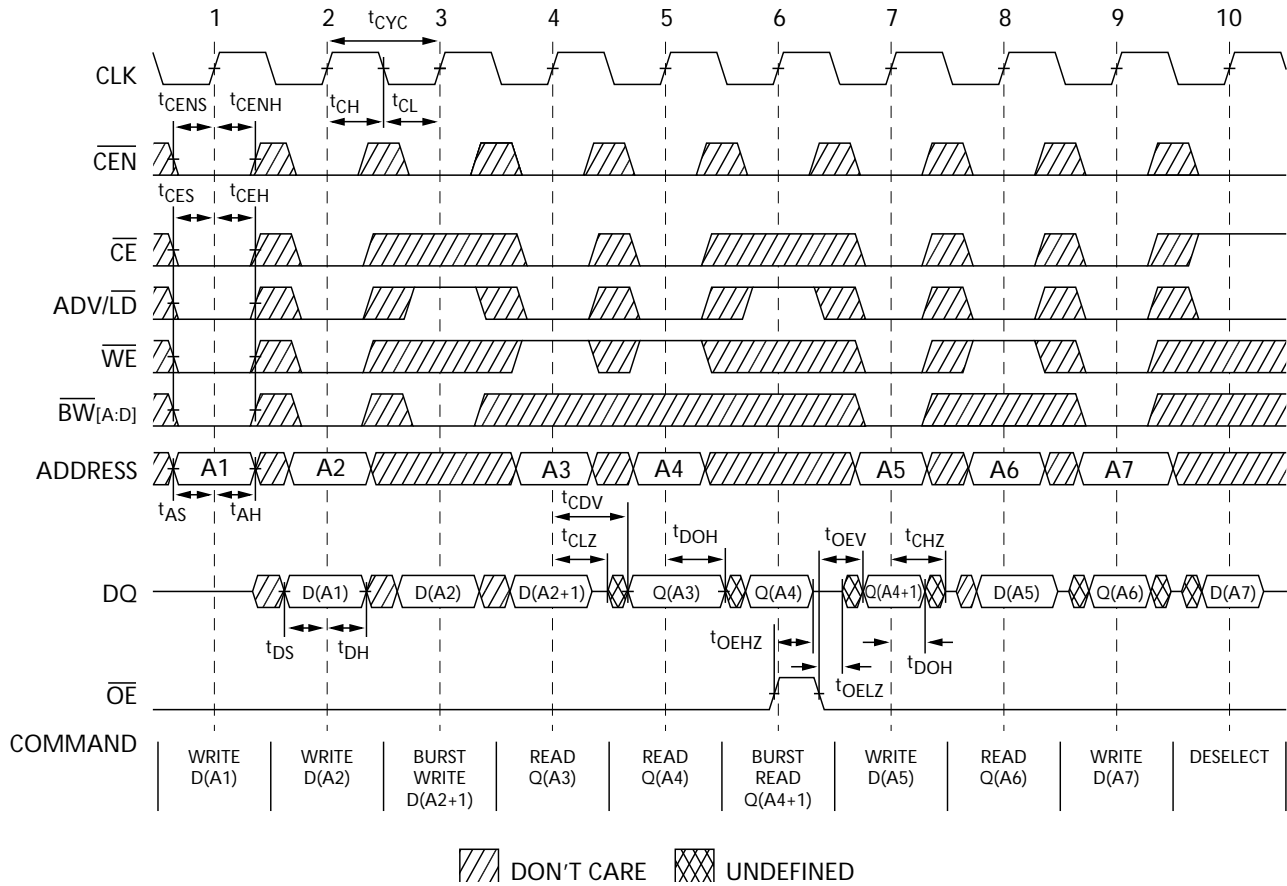
Notes
19. For this waveform ZZ is tied LOW.
20. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
21. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

[+] Feedback

Switching Waveforms *(continued)*

NOP, STALL and DESELECT Cycles[22, 23, 24]

WRITE D(A1)	READ Q(A2)	STALL	READ Q(A3)	WRITE D(A4)	STALL	NOP	READ Q(A5)	DESELECT	CONTINUE DESELECT

DON'T CARE   UNDEFINED

ZZ Mode Timing[25, 26]

DON'T CARE

Notes
22. For this waveform ZZ is tied LOW.
23. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
24. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.
25. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
26. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
100	CY7C1351G-100AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial
133	CY7C1351G-133AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	

Ordering Code Definitions

CY 7C 1351 G - XXX A X C

Temperature Range:
C = Commercial = 0 °C to 70 °C

X = Pb-free; X Absent = Leaded

Package Type:
A = 100-pin TQFP

Speed Grade: XXX = 100 MHz / 133 MHz

Process Technology ≥ 90 nm

1351 = FT, 128 Kb × 18 (2 Mb)

Marketing Code: 7C = SRAMs

Company ID: CY = Cypress
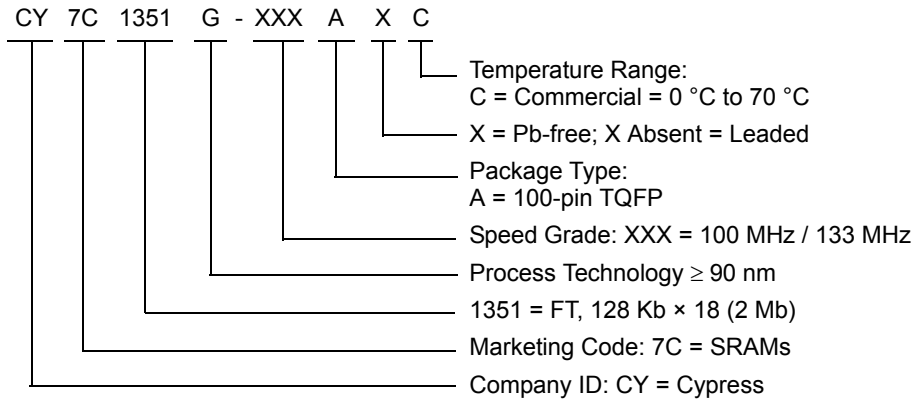
Package Diagrams

100-pin TQFP (14 × 20 × 1.4 mm), 51-85050
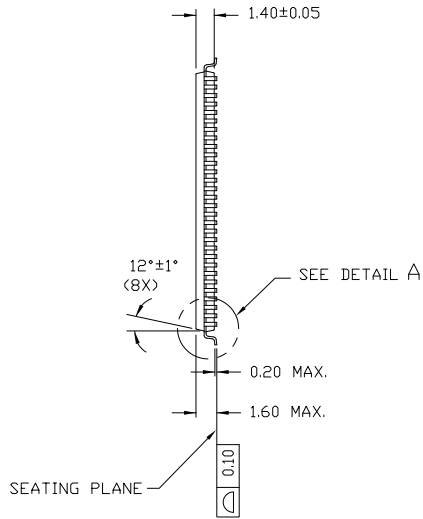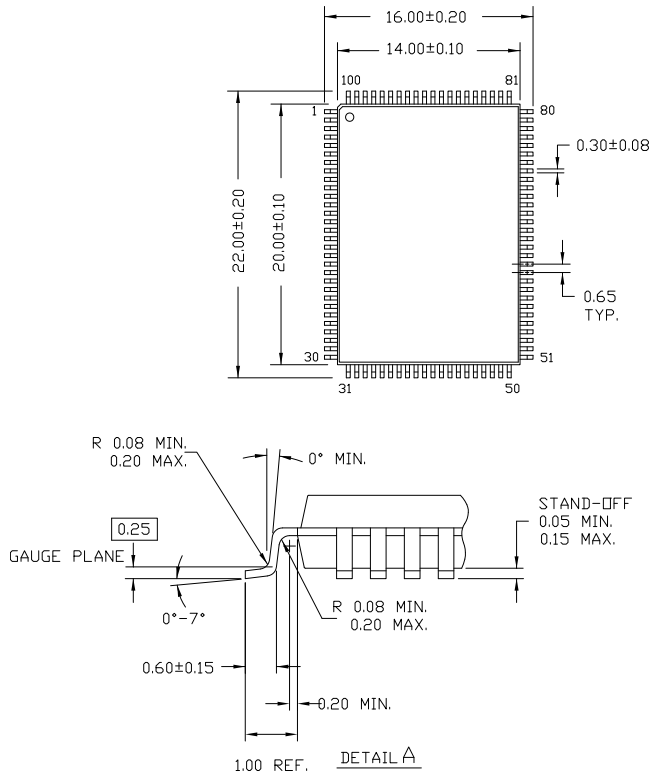
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *C

Package Diagrams *(continued)*

119-ball BGA (14 × 22 × 2.4 mm), 51-85115
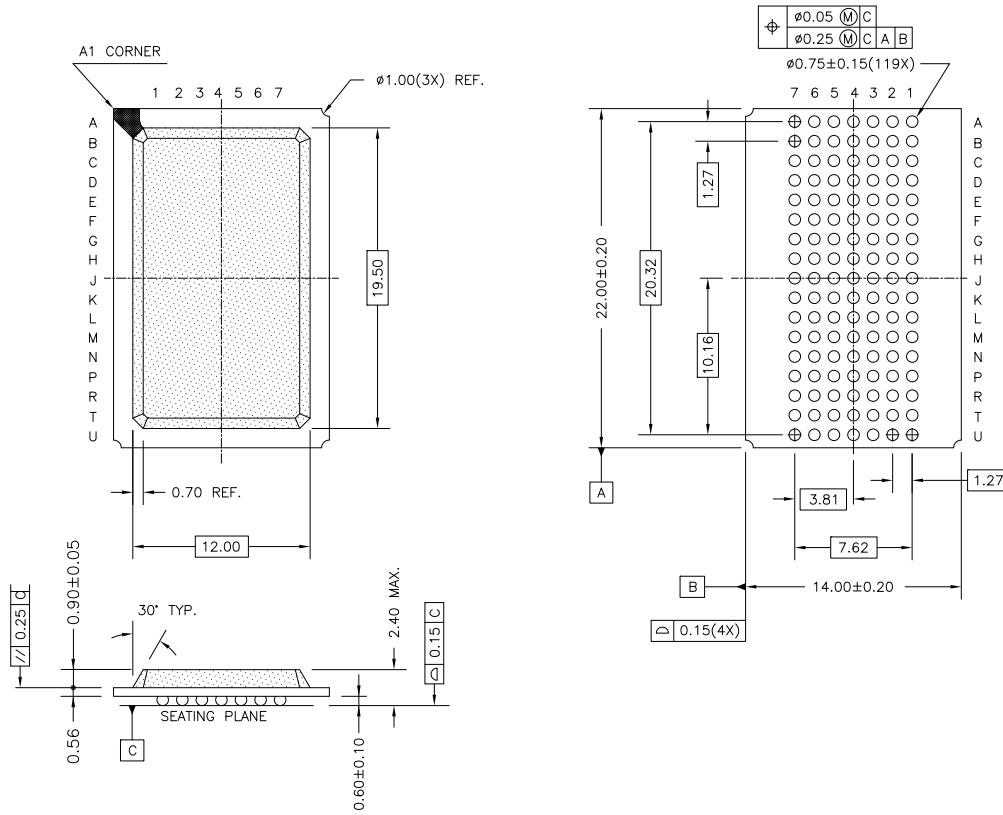
51-85115 *C

Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
CE	chip enable
CEN	clock enable
I/O	input/output
NoBL	No Bus Latency
OE	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius
%	percent

Document History Page

Document Title: CY7C1351G 4-Mbit (128 K × 36) Flow-through SRAM with NoBL™ Architecture Document Number: 38-05513				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224360	See ECN	RKF	New data sheet
*A	276690	See ECN	VBL	Deleted 66 MHz Changed TQFP package in Ordering Information section to lead-free TQFP Added comment of availability of BG lead-free package
*B	333626	See ECN	SYT	Removed 117-MHz speed bin Modified Address Expansion balls in the pinouts for 100 TQFP and 119 BGA Packages as per JEDEC standards and updated the Pin Definitions accordingly Modified V_{OL}, V_{OH} test conditions Replaced 'Snooze' with 'Sleep' Replaced TBD's for Θ_{JA} and Θ_{JC} to their respective values on the Thermal Resistance table Changed the package name for 100 TQFP from A100RA to A101 Updated the Ordering Information by shading and unshading MPNs as per availability
*C	418633	See ECN	RXU	Converted from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Modified Typo in V_{OH} test condition from "for 3.3V I/O" to "for 3.3V I/O, I_{OH} = –4.0 mA" and from "for 2.5V I/O" to "for 2.5V I/O, I_{OH} = –1.0 mA" in the Electrical Characteristics Table Modified Typo in V_{OL} test condition for 3.3V I/O from "I_{OH} = –4.0 mA" to "I_{OH} = 8.0 mA" and for 2.5V I/O from "I_{OH} = –1.0 mA" to "I_{OH} = 1.0 mA" in the Electrical Characteristics Table Modified Typo in the test condition for V_{IH} from "for 3.3V I/O, I_{OH} = 8.0 mA" to "for 3.3V I/O" and from "for 2.5V I/O, I_{OH} =1.0 mA" to "for 2.5V I/O" in the Electrical Characteristics Table Modified Typo in I_X Input Load Current test condition from "for 3.3V" to "GND $\le V_I \le V_{DDQ}$" and I_X Input Current of Mode test condition from "for 2.5V I/O and "GND $\le V_I \le V_{DDQ}$" to Input = V_{SS} and Input = V_{DD} respectively in the Electrical Characteristics Table Modified Typo in I_{SB4} from "$V_{IN} \ge V_{DDQ}$ – 0.3V or $V_{IN} \le$ 0.3V" to "$V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$" in the Electrical Characteristics Table Added V$_{DDQ}$ for 3.3V I/O in the Electrical Characteristics Table Modified test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \le V_{DD}$ Modified "Input Load" to "Input Leakage Current except ZZ and MODE" in the Electrical Characteristics Table Replaced Package Name column with Package Diagram in the Ordering Information table Replaced Package Diagram of 51-85050 from *A to *B Updated the Ordering Information
*D	480124	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V$_{DDQ}$ Relative to GND. Updated the Ordering Information table.
*E	2896584	03/20/2010	NJY	Removed obsolete part numbers from Ordering Information table and updated package diagrams.
*F	3033272	09/19/2010	NJY	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits and updated in new template.
*G	3067198	10/20/2010	NJY	Updated Ordering Information.
*H	3096309	11/28/2010	NJY	Minor edits and updated Functional Description.

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