

4-Mbit (256K x 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 7 μ A
- Ultra low active power
 - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP II package)

Functional Description

The CY62146E is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable

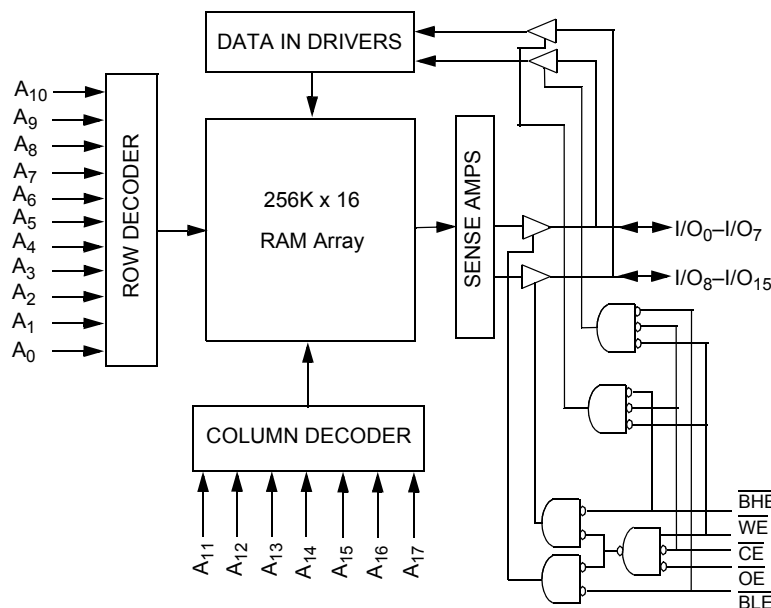
applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (\overline{CE} HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See Table for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram

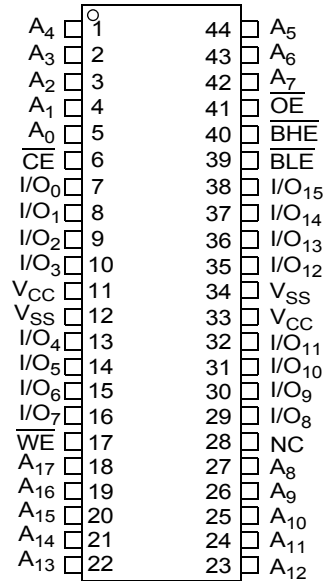


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Pin Configuration

Figure 1. 44-Pin TSOP II (Top View) ^[1]



Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby, I _{SB2} (μA)	
		f = 1 MHz		f = f _{max}							
		Min	Typ ^[2]	Max		Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max
CY62146ELL	Ind/I/Auto-A	4.5	5.0	5.5	45	2	2.5	15	20	1	7

Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential	-0.5 V to 6.0 V
DC voltage applied to outputs in high Z state ^[3, 4]	-0.5 V to 6.0 V
DC input voltage ^[3, 4]	-0.5 V to 6.0 V

Output current into outputs (LOW)	20 mA
Static discharge voltage.....	>2001 V (MIL-STD-883, Method 3015)
Latch-up current	>200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[5]
CY62146ELL	Industrial/ Auto-A	-40 °C to +85 °C	4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Ind'I/Auto-A)			Unit
			Min	Typ ^[6]	Max	
V _{OH}	Output high voltage	I _{OH} = -1.0 mA	2.4	-	-	V
V _{OL}	Output low voltage	I _{OL} = 2.1 mA	-	-	0.4	V
V _{IH}	Input high voltage	4.5 ≤ V _{CC} ≤ 5.5	2.2	-	V _{CC} + 0.5	V
V _{IL}	Input low voltage	4.5 ≤ V _{CC} ≤ 5.5	-0.5	-	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled	-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{max} = 1/t _{RC}	-	15	20	mA
		f = 1 MHz	-	2	2.5	
I _{SB2} ^[7]	Automatic CE power down current — CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = V _{CC(max)}	-	1	7	μA

Capacitance

Parameter ^[8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

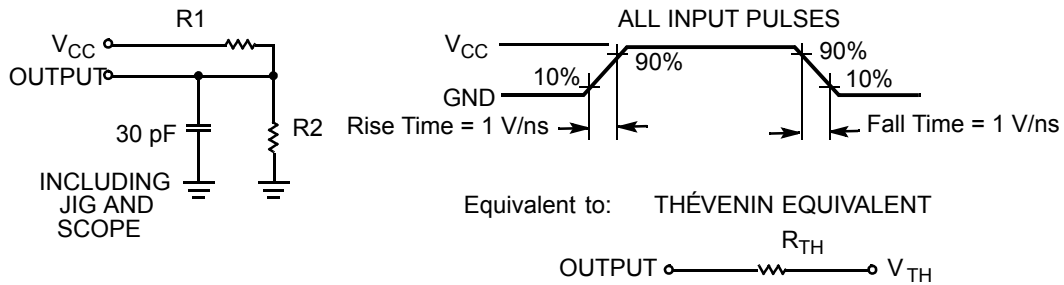
Thermal Resistance

Parameter ^[8]	Description	Test Conditions	TSOP II	Unit
θ _{JA}	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two layer printed circuit board	77	°C/W
θ _{JC}	Thermal resistance (Junction to case)		13	°C/W

Notes

- V_{IL}(min) = -2.0 V for pulse durations less than 20 ns for I < 30 mA.
- V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full Device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs are left floating.
- Tested initially after any design or process changes that may affect these parameters.

Figure 2. AC Test Loads and Waveforms



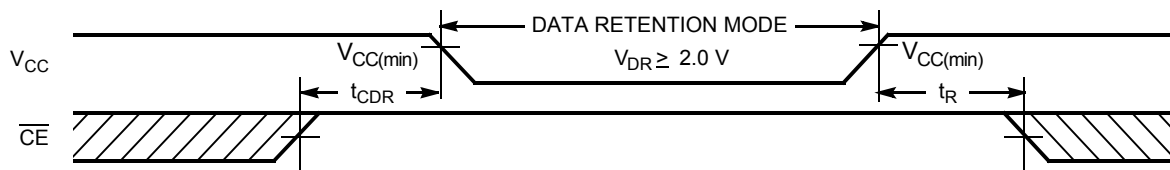
Parameters	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R _{TH}	639	Ω
V _{TH}	1.77	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[9]	Max	Unit
V _{DR}	V _{CC} for data retention		2	–	–	V
I _{CCDR} ^[10]	Data retention current	V _{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} $\geq V_{CC} - 0.2$ V or V _{IN} ≤ 0.2 V	–	1	7	μ A
t _{CDR} ^[11]	Chip deselect to data retention time		0	–	–	ns
t _R ^[12]	Operation recovery time		45	–	–	ns

Figure 3. Data Retention Waveform



Notes

- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- 10. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs are left floating.
- 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μ s or stable at V_{CC(min)} ≥ 100 μ s.

Switching Characteristics

Over the Operating Range

Parameter ^[13, 14]	Description	45 ns (Ind'l/Auto-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to LOW Z ^[15]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[15, 16]	–	18	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[15]	10	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[15, 16]	–	18	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down	–	45	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[15]	5	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z ^[15, 16]	–	18	ns
Write Cycle^[17]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE} LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[15, 16]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[15]	10	–	ns

Notes

13. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in [AC Test Loads and Waveforms on page 5](#).
14. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See [application note AN13842](#) for further clarification.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
17. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No.1: Address Transition Controlled^[18, 19]

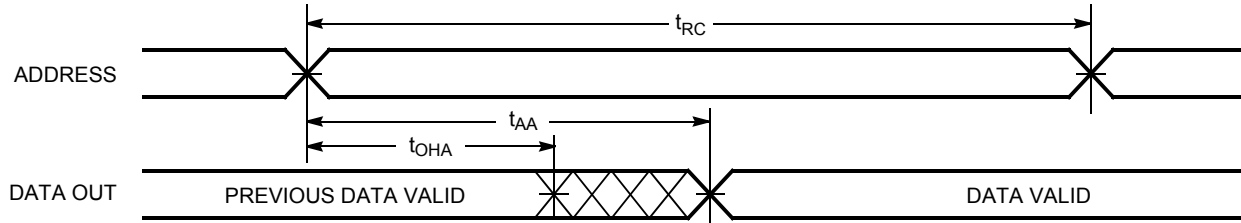
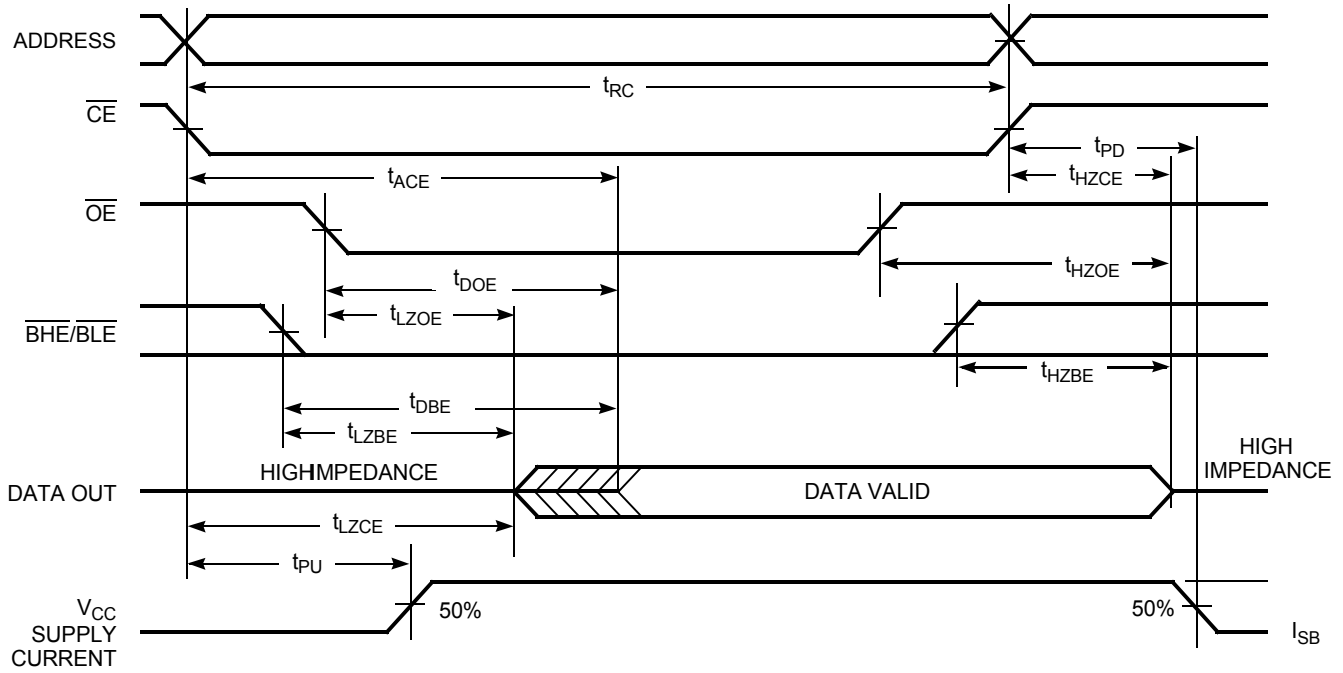


Figure 5. Read Cycle No. 2: \overline{OE} Controlled^[19, 20]



Notes

18. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} .
19. \overline{WE} is HIGH for read cycle.
20. Address valid before or similar to \overline{CE} , \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No 1: \overline{WE} Controlled [21, 22, 23]

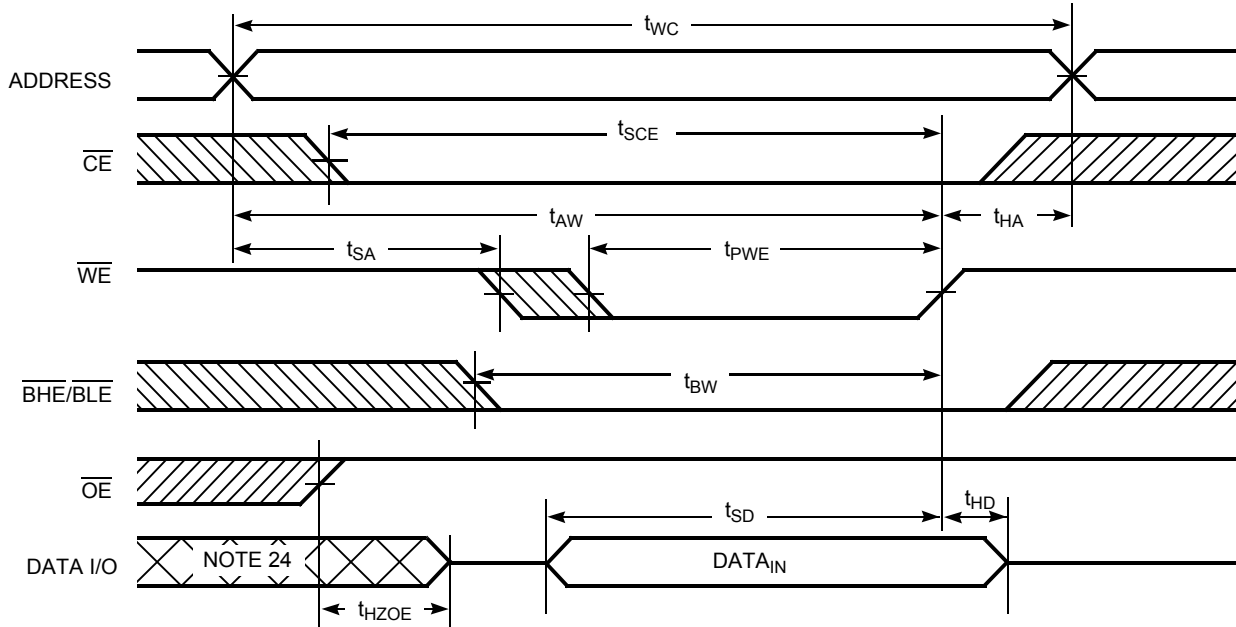
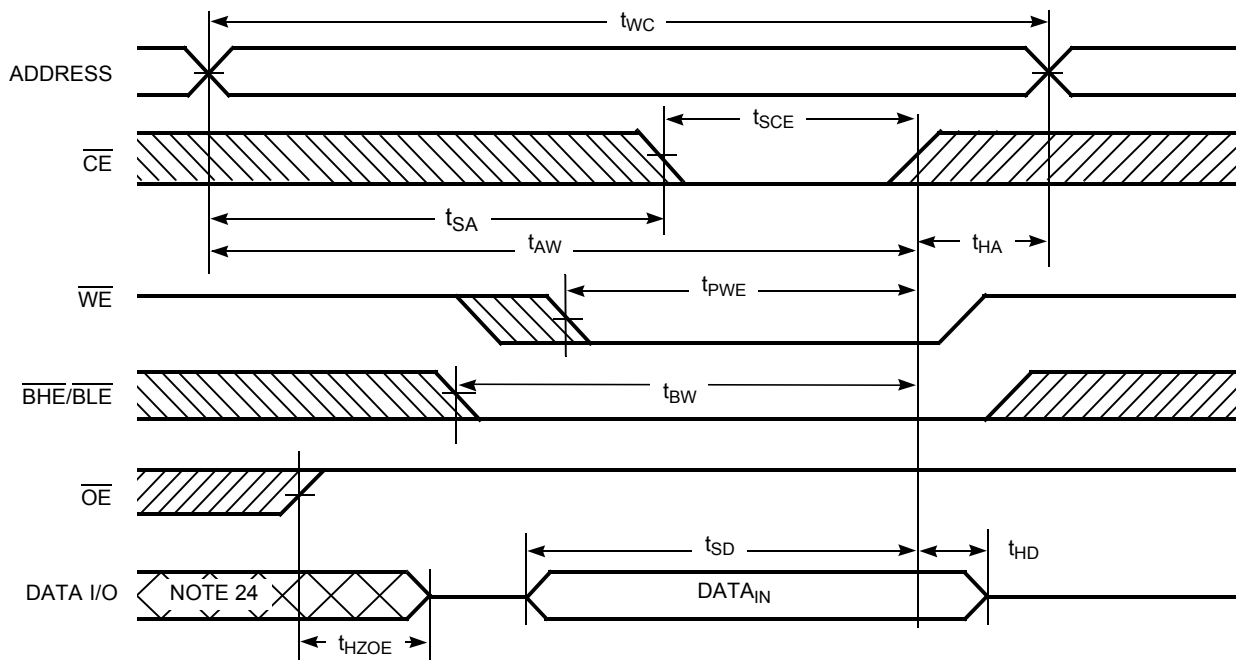


Figure 7. Write Cycle 2: \overline{CE} Controlled [21, 22, 23]



Notes

- 21. \overline{WE} is HIGH for read cycle.
- 22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 23. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 24. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle 3: \overline{WE} controlled, \overline{OE} LOW ^[25]

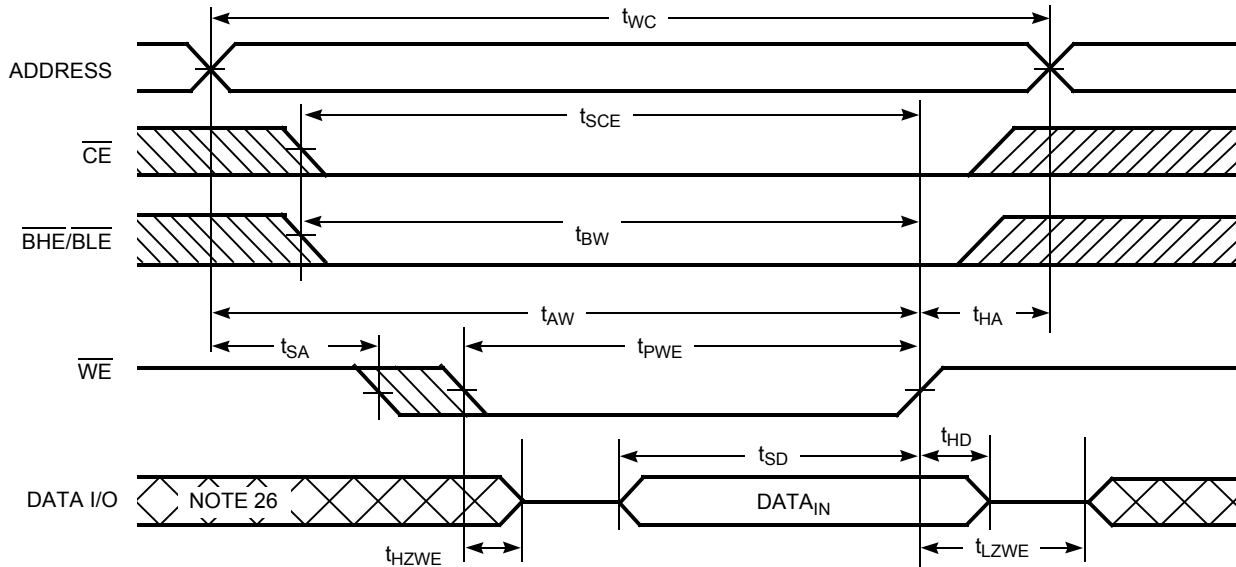
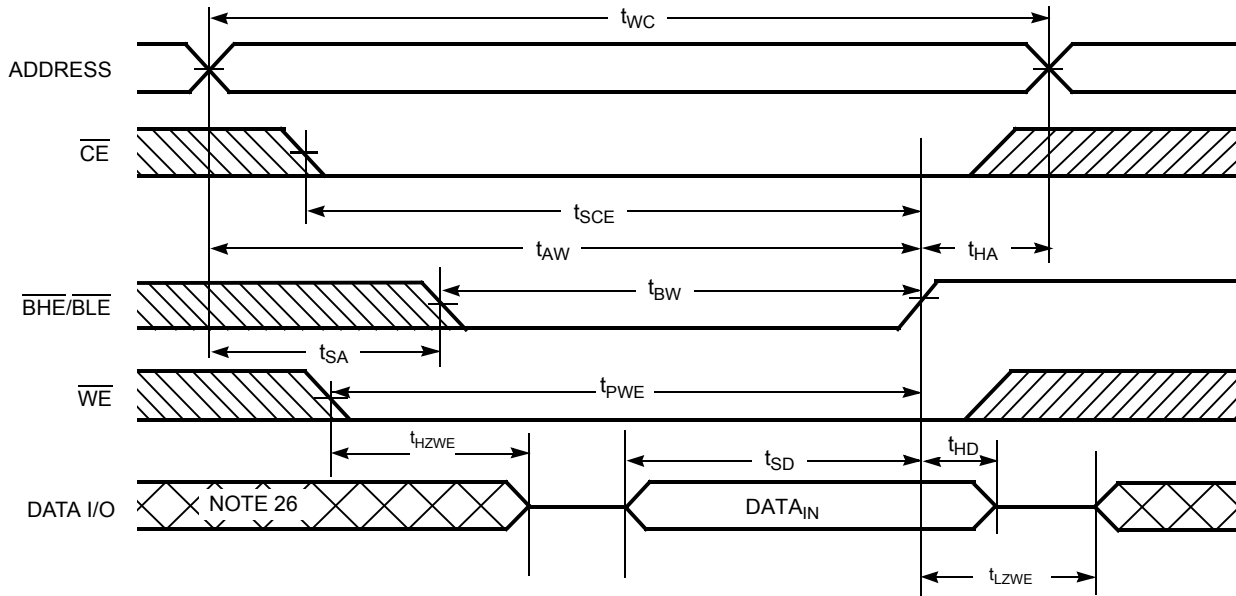


Figure 9. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW ^[25]



Notes

- 25. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 26. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{\text{CE}}^{[27]}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X ^[27]	X ^[27]	High Z	Deselect/power down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O ₀ –I/O ₁₅)	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O ₀ –I/O ₁₅)	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I_{CC})

Note

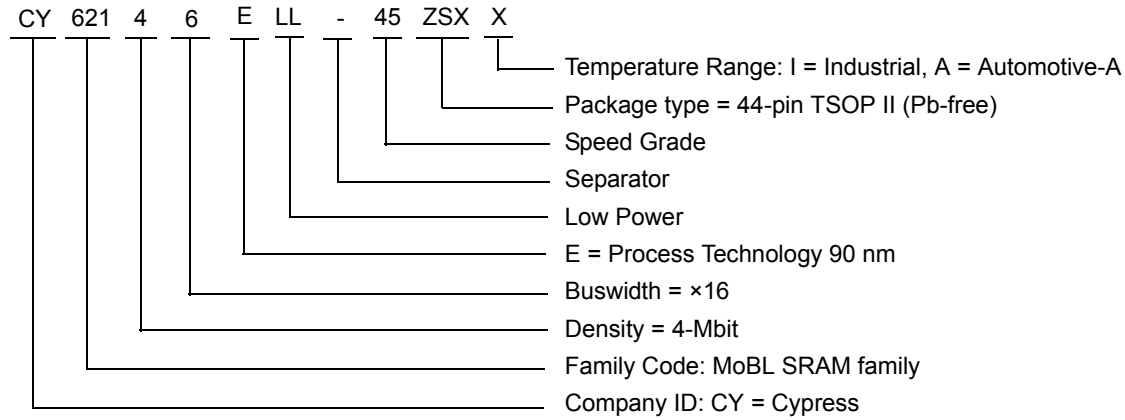
27. Chip enable ($\overline{\text{CE}}$) and byte enables ($\overline{\text{BHE}}$ and $\overline{\text{BLE}}$) must be at CMOS levels (not floating) to meet the $I_{\text{SB}2}$ / I_{CCDR} spec. Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146ELL-45ZSXI	51-85087	44-pin thin small outline package II (Pb-free)	Industrial
	CY62146ELL-45ZSXA	51-85087	44-pin thin small outline package II (Pb-free)	Automotive-A

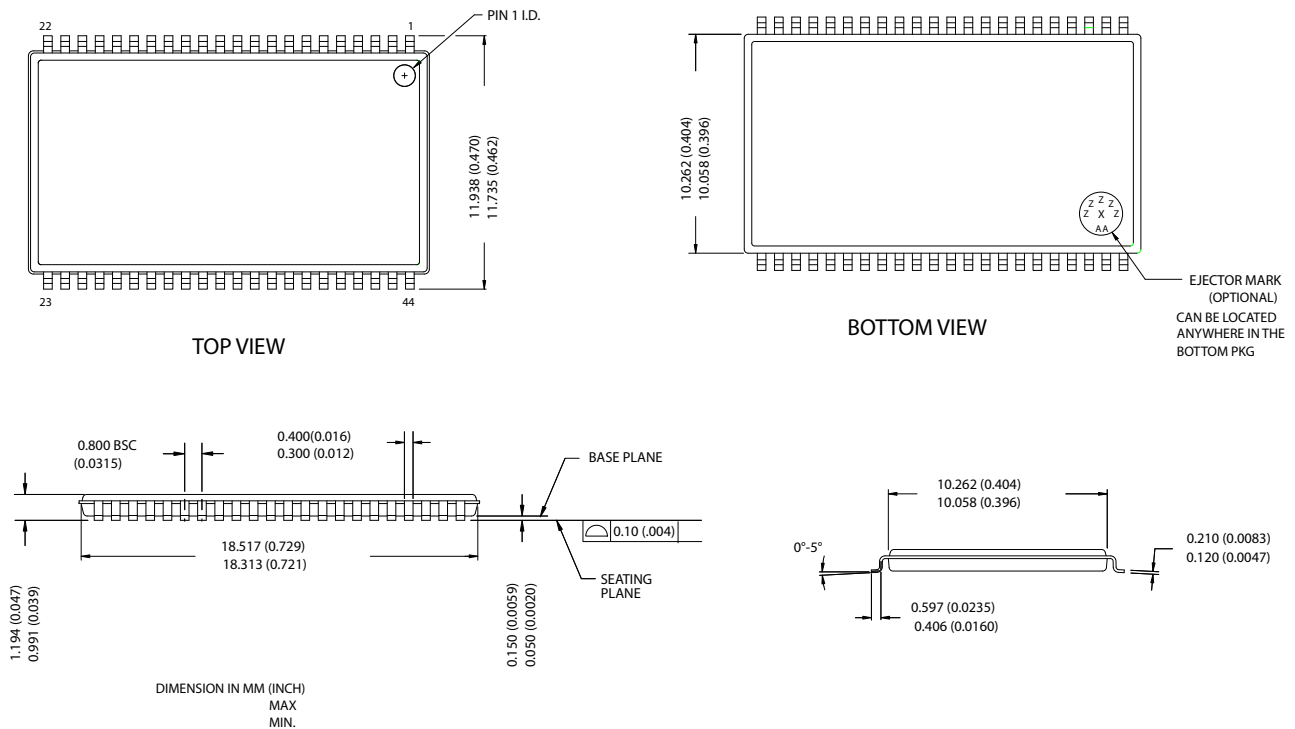
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 10. 44-Pin TSOP II, 51-85087



51-85087-1C

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	volts
μ A	micro amperes
mA	milli amperes
pF	pico Farad
$^{\circ}$ C	degree Celsius
W	watts

Document History Page

Document Title: CY62146E MoBL [®] 4-Mbit (256K x 16) Static RAM Document Number: 001-07970				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	463213	See ECN	NXR	New Data Sheet
*A	684343	See ECN	VKN	Added Preliminary Automotive-A Information Updated Ordering Information Table
*B	925501	See ECN	VKN	Added footnote #8 related to I _{SB2} and I _{CCDR} Added footnote #13 related AC timing parameters
*C	1045260	See ECN	VKN	Converted Automotive-A specs from preliminary to final
*D	2073548	See ECN	VKN/AESA	Corrected typo in the Data Retention Waveform and removed its irrelevant footnote
*E	2943752	06/03/2010	VKN	Added Contents Added footnote related to chip enable in Truth Table Updated Package Diagram Added Sales, Solutions, and Legal Information
*F	3109050	12/13/2010	PRAS	Changed Table Footnotes to Footnotes. Added Ordering Code Definitions.
*G	3149059	01/20/2011	RAME	Updated as per latest template Corrected Errors in Ordering Code Definitions Added Acronyms and Units of Measure table

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