CY62136EV30 MoBL®

2-Mbit (128K x 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62136CV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Offered in a Pb-free 48-ball very fine ball grid array (VFBGA) and 44-pin thin small outline package (TSOP II) packages

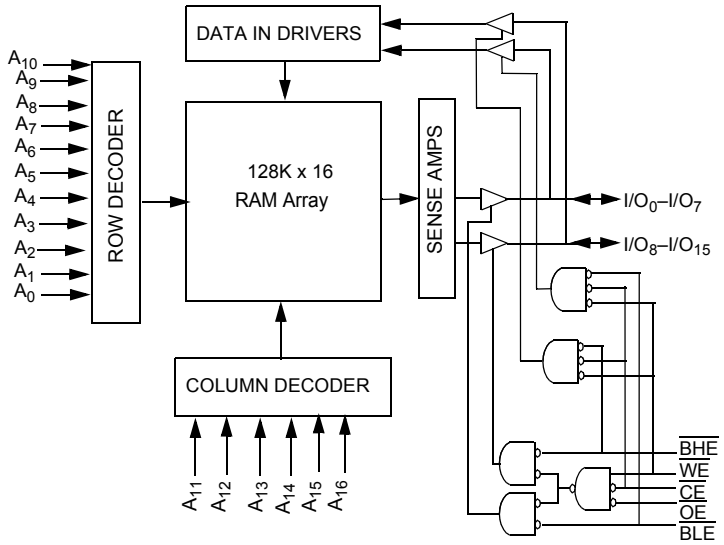
Functional Description

The CY62136EV30[1] is a high performance CMOS static RAM organized as 128 K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appear on I/O_8 to I/O_{15}. See the Truth Table on page 10 for a complete description of read and write modes.

Logic Block Diagram

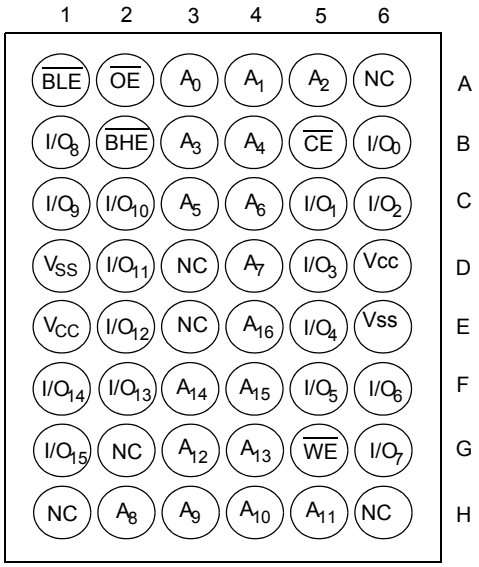


Note
1. For best practice recommendations, refer to the Cypress application note “SRAM System Design Guidelines” on http://www.cypress.com.

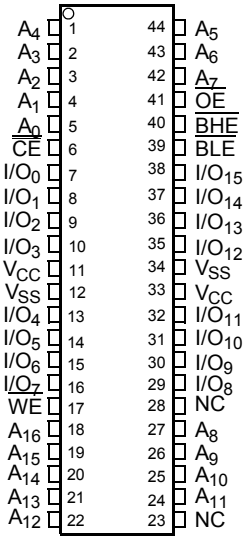
Contents

Pin Configuration[2, 3]

VFBGA (Top View)



44 TSOP II (Top View)



Product Portfolio[4]

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating ICC (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[4]	Max		Typ[4]	Max	Typ[4]	Max	Typ[4]	Max
CY62136EV30LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Notes
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, H6 and H3 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.3 V to 3.9 V ($V_{CC\ MAX}$ + 0.3 V)

DC voltage applied to outputs in High-Z state[5,6] ..... –0.3 V to 3.9 V ($V_{CC\ MAX}$ + 0.3 V)

DC input voltage[5,6] ..... –0.3 V to 3.9 V ($V_{CC\ MAX}$ + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V (per MIL-STD-883, Method 3015)

Latch up current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[7]
CY62136EV30LL	Industrial	–40 °C to +85 °C	2.2 V - 3.6 V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ[8]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20 V	2.0	–	–	V
		I_{OH} = –1.0 mA	V_{CC} = 2.70 V	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20 V	–	–	0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70 V	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2V to 2.7 V		1.8	–	V_{CC} + 0.3	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels	–	15	20	mA
		f = 1 MHz		–	2	2.5	
I_{SB1}[9]	Automatic CE power-down current — CMOS inputs	$\overline{CE}$ ≥ V_{CC}–0.2 V, V_{IN}≥V_{CC}–0.2 V, V_{IN}≤0.2 V) f = f_{max} (address and data only), f = 0 (OE, and WE), V_{CC} = 3.60 V		–	1	7	µA
I_{SB2} [9]	Automatic CE power-down current — CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60 V		–	1	7	µA

Capacitance

Parameter[10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

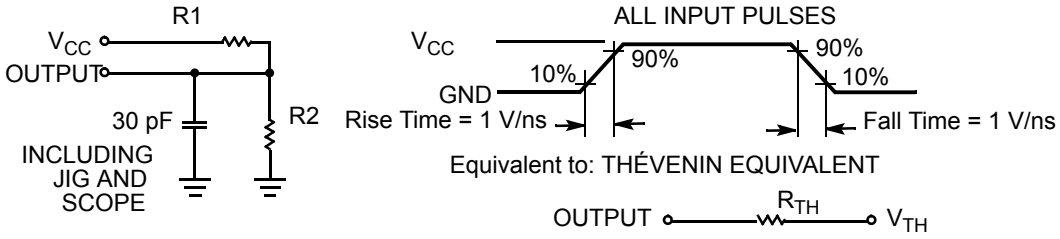
Notes

5. $V_{IL(min.)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$=V_{CC}+0.75 V for pulse durations less than 20 ns.
7. Full Device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C
9. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter[11]	Description	Test Conditions	VFBGA Package	TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C / W
Θ_{JC}	Thermal resistance (junction to case)		10	13	°C / W

Figure 1. AC Test Loads and Waveforms



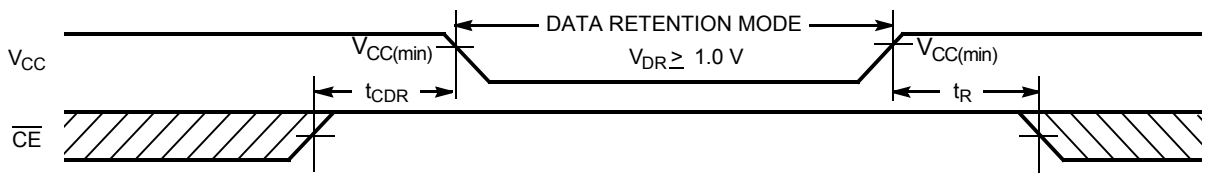
Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics

(Over the Operating Range)

Parameter	Description	Conditions	Min	Typ[12]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} [13]	Data retention current	V_{CC}= 1.0 V $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	0.8	3	µA
t_{CDR}[11]	Chip deselect to data retention time		0	–	–	ns
t_R[14]	Operation recovery time		45		–	ns

Data Retention Waveform[15]



Notes
11. Tested initially and after any design or process changes that may affect these parameters.
12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, T_A = 25 °C
13. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.
15. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. The chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics Over the Operating Range

Parameter[16, 17]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[18]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[18, 19]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[18]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[18, 19]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[18]	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH Z[18, 19]	–	18	ns
Write Cycle[20]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[18, 19]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[18]	10	–	ns

Notes

16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in AC Test Loads and Waveforms.
17. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. Refer application note AN13842 for more information.
18. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
19. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
20. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 2. Read Cycle 1: Address Transition Controlled [21, 22]

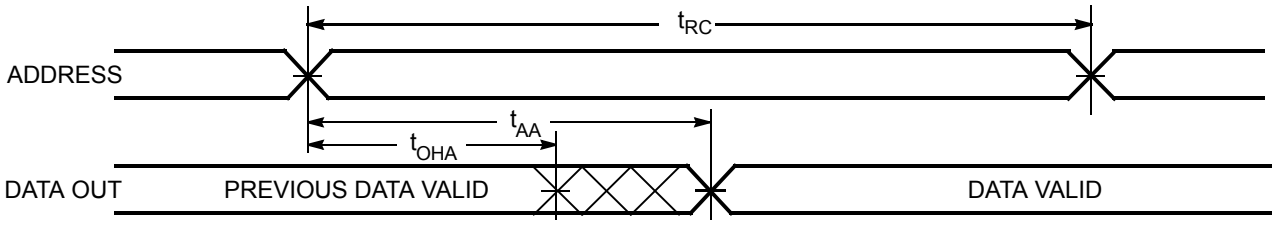
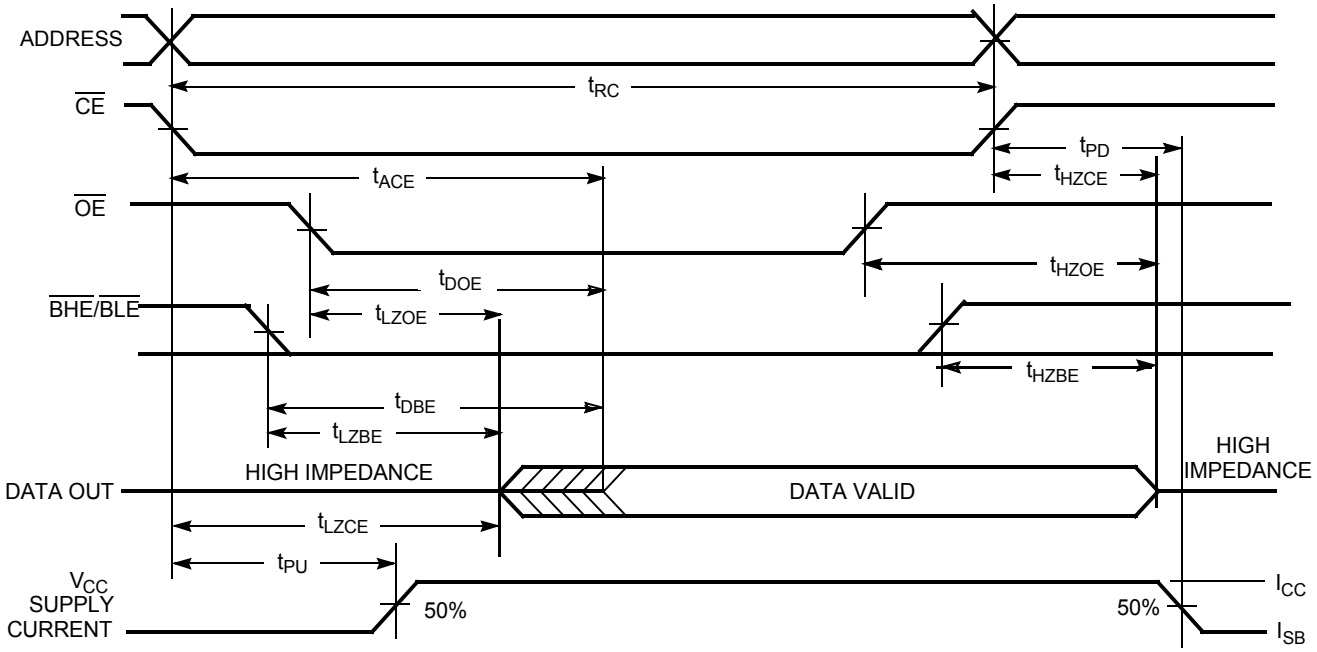


Figure 3. Read Cycle No. 2 : $\overline{OE}$ Controlled[22, 23]



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Notes
21. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
22. $\overline{WE}$ is HIGH for read cycle.
23. Address valid prior to or coincident with $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 4. Write Cycle No. 1: $\overline{WE}$ Controlled [24, 25, 26]

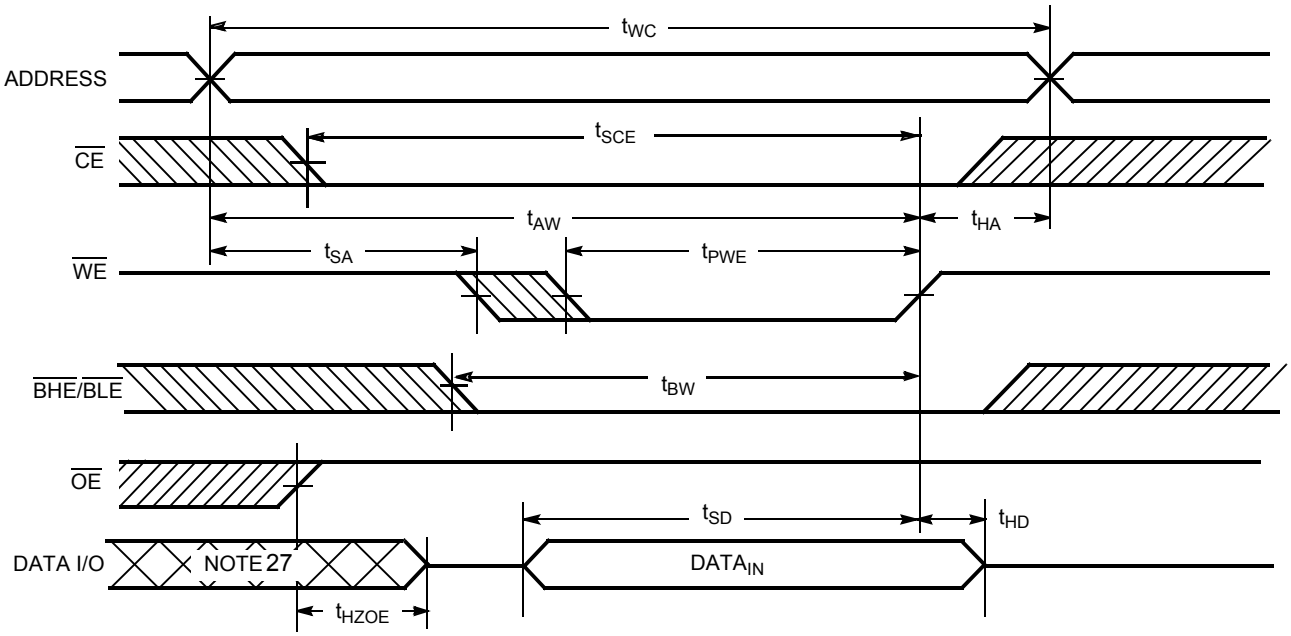
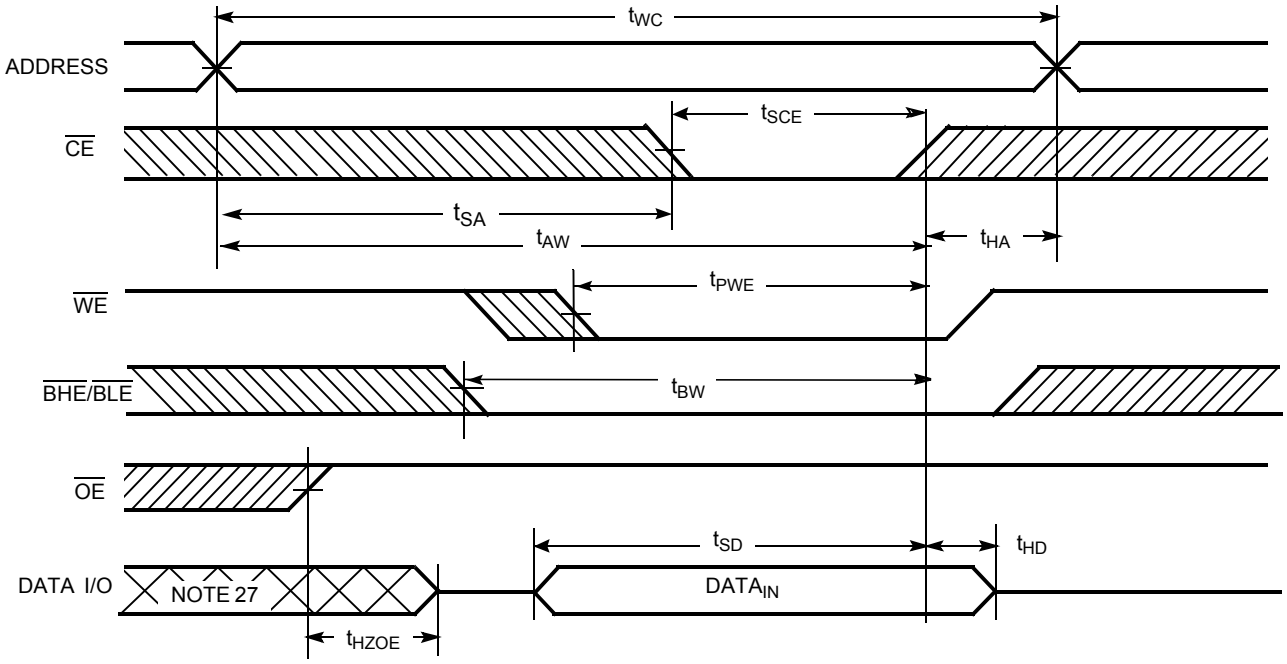


Figure 5. Write Cycle No. 2: $\overline{CE}$ Controlled [24, 25, 26]



Notes

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
27. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [28]

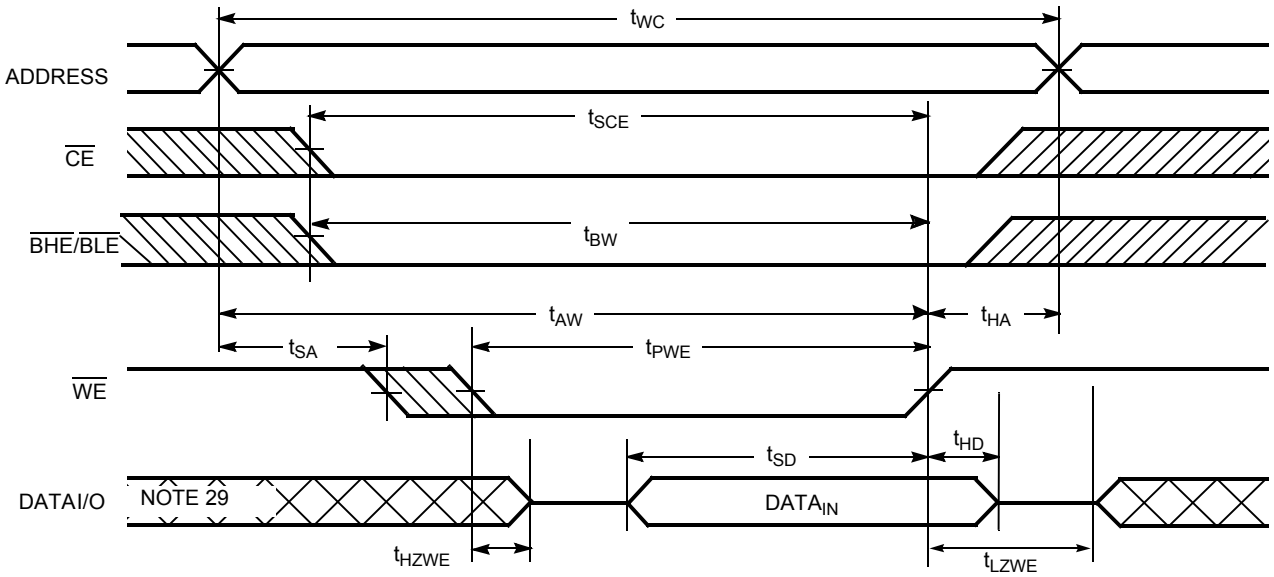
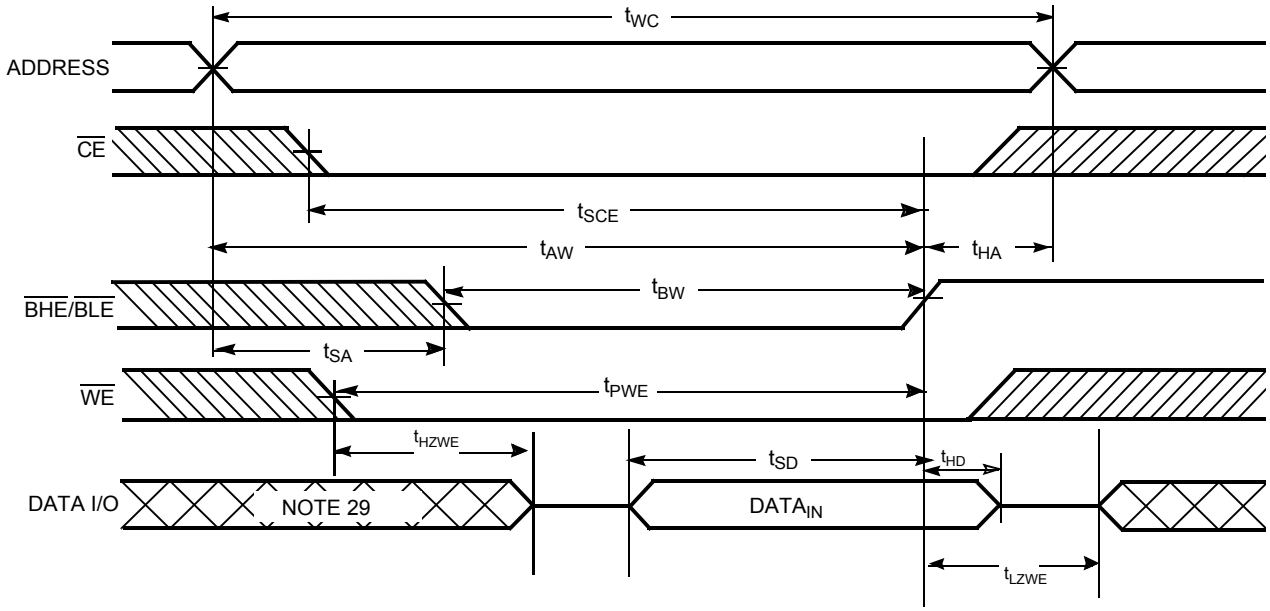


Figure 7. Write Cycle No. 4: $\overline{BHE/BLE}$ Controlled, $\overline{OE}$ LOW [28]



Notes
28. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state
29. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H[30]	X	X	X[30]	X[30]	High Z	Deselect/power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

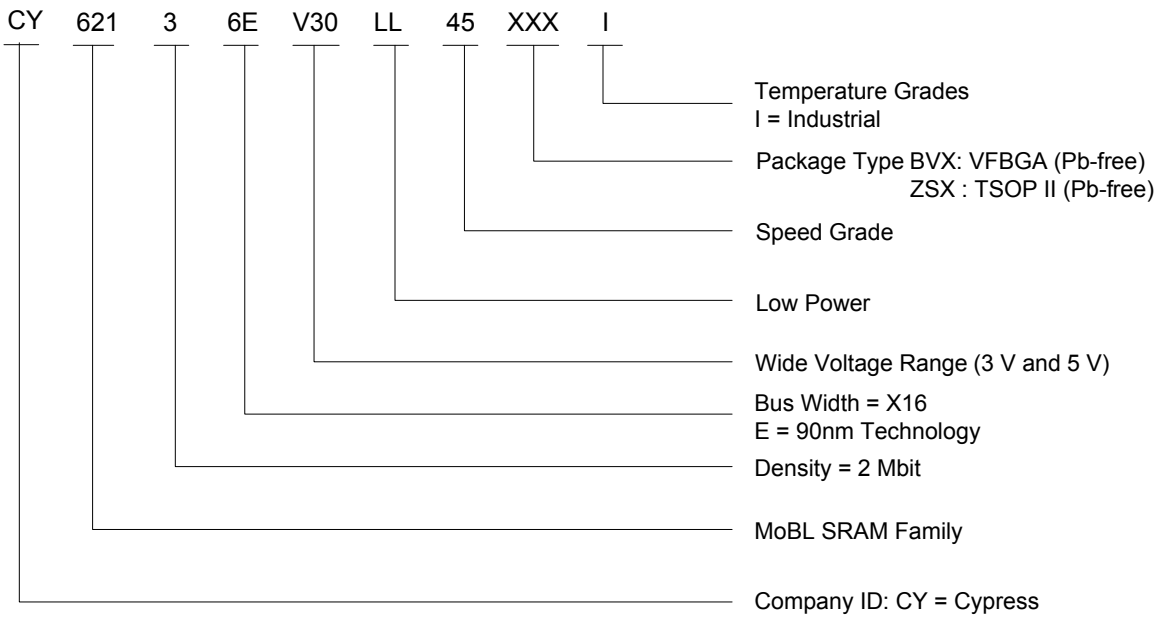
Note
30. Chip enable ($\overline{CE}$) and Byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be at fixed CMOS levels (not floating). Intermediate voltage levels on these pins is not permitted

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136EV30LL-45BVXI	51-85150	48-Ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62136EV30LL-45ZSXI	51-85087	44-Pin Thin Small Outline Package II (Pb-free)	

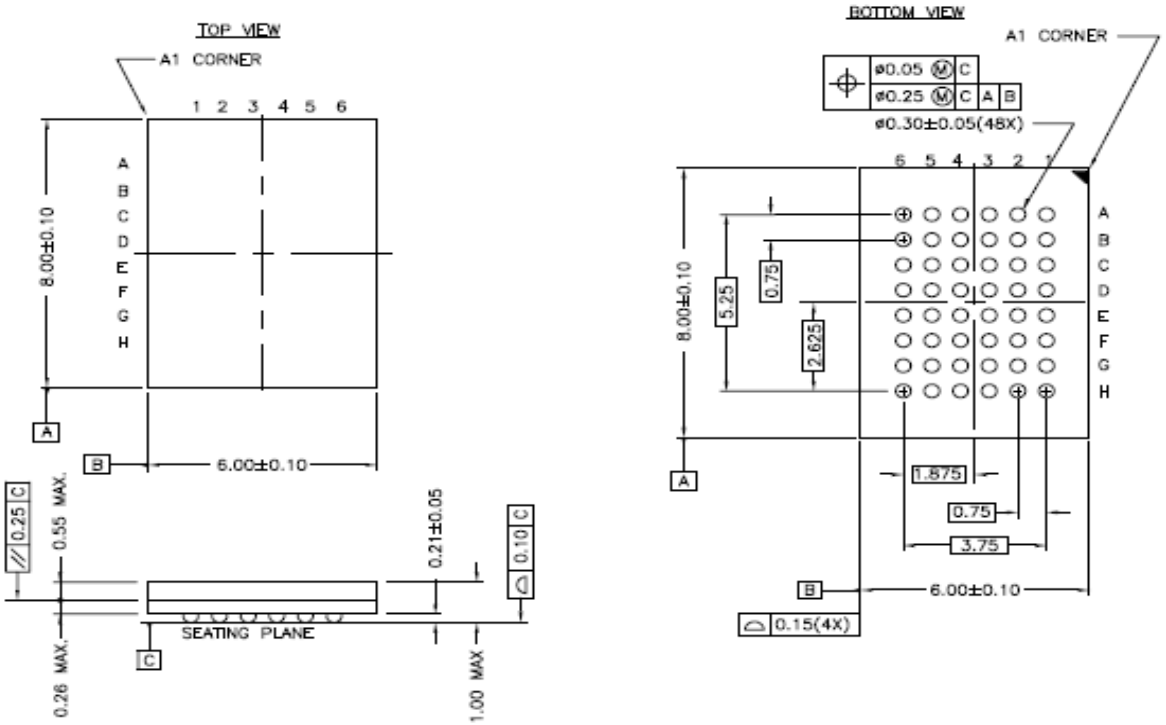
Contact your local Cypress sales representative for availability of other parts

Ordering Code Definition



Package Diagrams

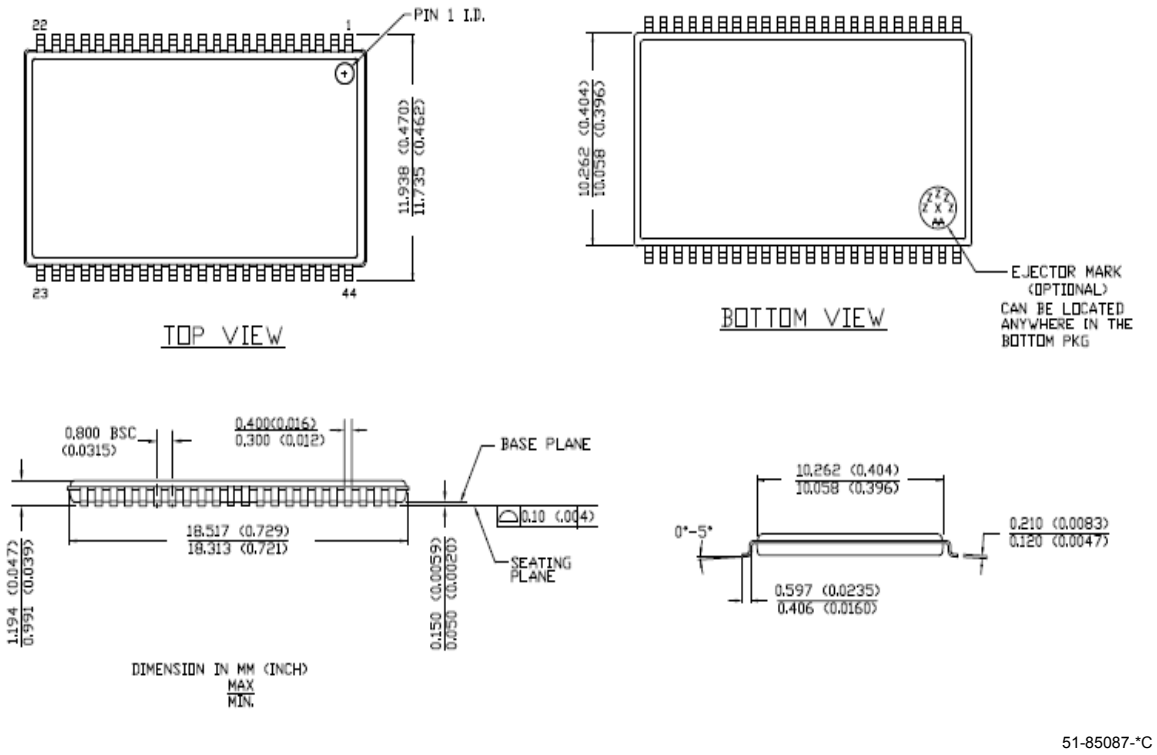
Figure 8. 48-Pin VFBGA (6 x 8 x 1 mm) (51-85150)



51-85150-*F

Package Diagrams (continued)

Figure 9. 44-Pin TSOP II (51-85087)



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball gird array
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62136EV30 MoBL® 2-Mbit (128K x 16) Static RAM Document Number: 38-05569				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	237432	AJU	See ECN	New Data Sheet
*A	419988	RXU	See ECN	Converted from Advanced Information to Final. Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Removed 35ns Speed Bin Removed “L” version of CY62136EV30 Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max} Changed I_{SB1} and I_{SB2} Typ. values from 0.7 µA to 1 µA and Max. values from 2.5 µA to 7 µA. Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed V_{DR} from 1.5V to 1V on Page# 4. Changed I_{CCDR} from 2.5 µA to 3 µA. Added I_{CCDR} typical value. Changed t_{OHA}, t_{LZCE} and t_{LZWE} from 6 ns to 10 ns Changed t_{LZBE} from 6 ns to 5 ns Changed t_{LZOE} from 3 ns to 5 ns Changed t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} from 15 ns to 18 ns Changed t_{SCE}, t_{AW} and t_{BW} from 40 ns to 35 ns Changed t_{PWE} from 30 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Corrected typo in the Truth Table on Page# 9 Updated the package diagram 48-pin VFBGA from *B to *D Updated the ordering Information table and replaced the Package Name column with Package Diagram.
*B	427817	NXR	See ECN	Minor change: Moved datasheet to external web
*C	2604685	VKN/PYRS	11/12/08	Added footnote 8 related to I_{SB2} and I_{CCDR} Added footnote 12 related to AC timing parameters
*D	3144174	RAME	01/17/2011	Added Acronyms and Units of Measure table Added Ordering Code Definition Update Package Diagrams 51-85150 from *D to *F Converted all tablenotes into footnotes Added TOC Updated datasheet as per new template.

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