

# 1-Mbit (128K x 8) Static RAM

#### **Features**

■ Very high speed: 45 ns

■ Temperature ranges

☐ Industrial: -40°C to +85°C ☐ Automotive-A: -40°C to +85°C ☐ Automotive-E: -40°C to +125°C

■ Voltage range: 4.5V to 5.5V

■ Pin compatible with CY62128B

■ Ultra low standby power

Typical standby current: 1 μA

Maximum standby current: 4 μA (Industrial)

■ Ultra low active power

□ Typical active current: 1.3 mA at f = 1 MHz

■ Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features

■ Automatic power down when deselected

■ CMOS for optimum speed and power

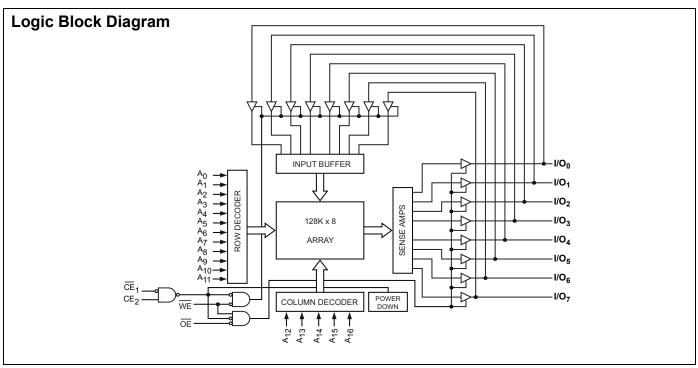
 Offered in standard Pb-free 32-pin STSOP, 32-pin SOIC, and 32-pin TSOP I packages

### **Functional Description**

The CY62128E<sup>[1]</sup> is a high performance CMOS static RAM organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life  $^{\rm TM}$  (MoBL  $^{\rm ®}$ ) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (CE $_1$  HIGH or CE $_2$  LOW). The eight input and output pins (I/O $_0$  through I/O $_7$ ) are placed in a high impedance state when the device is deselected (CE $_1$  HIGH or CE $_2$  LOW), the outputs are disabled (OE HIGH), or a write operation is in progress (CE $_1$ LOW and CE $_2$  HIGH and WE LOW)

To write to the device, take Chip Enable ( $\overline{\text{CE}}_1$  LOW and CE<sub>2</sub> HIGH) and Write Enable (WE) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

To read from the device, take Chip Enable  $(\overline{CE}_1 LOW)$  and  $CE_2 \underline{HIGH}$ ) and Output Enable  $(\overline{OE})$  LOW while forcing Write Enable  $(\overline{WE})$  HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.



Note

1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at http://www.cypress.com.

# CY62128E MoBL®



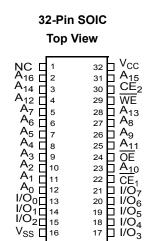
# **Contents**

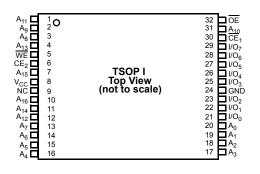
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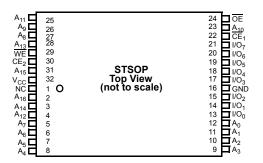
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# Pin Configuration<sup>[2]</sup>







#### **Product Portfolio**

								Power D	Dissipati	on	
Product	Range V <sub>CC</sub> Range (V)		Range V <sub>CC</sub> Range (V) Speed (ns)	V <sub>CC</sub> Range (V)		Operating I <sub>CC</sub> (mA)				Standby L (uA)	
						f = 1MHz		f = f <sub>max</sub>		Standby I <sub>SB2</sub> (μA)	
		Min	<b>Typ</b> <sup>[3]</sup>	Max		<b>Typ</b> [3]	Max	<b>Typ</b> <sup>[3]</sup>	Max	<b>Typ</b> <sup>[3]</sup>	Max
CY62128ELL	Ind'I/Auto-A	4.5	5.0	5.5	45 <sup>[4]</sup>	1.3	2	11	16	1	4
CY62128ELL	Auto-E	4.5	5.0	5.5	55	1.3	4	11	35	1	30

#### Notes

- 2. NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25^{\circ}C$ . When used with a 100 pF capacitive load and resistive loads as shown on page 4, access times of 55 ns  $(t_{AA}, t_{ACE})$  and 25 ns  $(t_{DOE})$  are guaranteed.



### **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ......-65°C to +150°C

Ambient Temperature with

Power Applied .......55°C to +125°C

Supply Voltage to Ground

Potential......-0.5V to 6.0V (V<sub>CC(max)</sub> + 0.5V)

DC Voltage Applied to Outputs in High-Z State  $^{[5,\ 6]}$  ......-0.5V to 6.0V (V  $_{CC(max)}$  + 0.5V)

DC Input Voltage<sup>[5, 6]</sup>.....-0.5V to 6.0V ( $V_{CC(max)} + 0.5V$ )

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage(MIL-STD-883, Method 3015)	> 2001V
Latch up Current	> 200 mA

## **Operating Range**

Device	Device Range Ambient Temperatu		<b>V</b> cc <sup>[7]</sup>
CY62128ELL	Ind'l/Auto-A	–40°C to +85°C	4.5V to 5.5V
	Auto-E	-40°C to +125°C	

#### Electrical Characteristics (Over the Operating Range)

Dawamataw	Description	Test Conditions		45	ns (Ind'I	/Auto-A)	5	11:4		
Parameter	Description			Min	<b>Typ</b> [3]	Max	Min	<b>Typ</b> <sup>[3]</sup>	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1 mA		2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA				0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 4.5V to 5.5V		2.2		V <sub>CC</sub> + 0.5	2.2		V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW voltage	V <sub>CC</sub> = 4.5V to 5.5V		-0.5		0.8	-0.5		0.8	V
I <sub>IX</sub>	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		<b>–1</b>		+1	-4		+4	μА
I <sub>OZ</sub>	Output Leakage Current	$GND \le V_O \le V_{CC}$ , Output Disabled		<b>–1</b>		+1	-4		+4	μА
I <sub>CC</sub>	V <sub>CC</sub> Operating	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$ $I_{OUT} = 0 \text{ mA}$		11	16		11	35	mA
	Supply Current	f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS levels		1.3	2		1.3	4	
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE Power down Current—CMOS Inputs		2V or $CE_2 \le 0.2V$ , 2V or $V_{IN} \le 0.2V$ , C(max)		1	4		1	30	μА

## Capacitance (For all Packages) [9]

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	10	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = V_{CC(typ)}$	10	pF

- Notes

  5. V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.

  6. V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.

  7. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub>(min) and 200 μs wait time after V<sub>CC</sub> stabilization.

  8. Only chip enables (CE<sub>1</sub> and CE<sub>2</sub>) must be at CMOS level to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

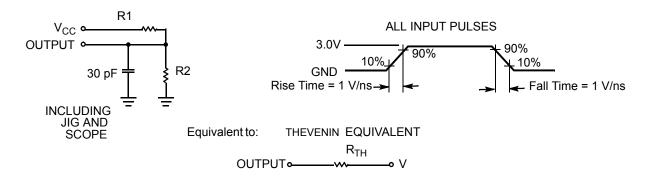
  9. Tested initially and after any design or process changes that may affect these parameters.



#### Thermal Resistance<sup>[9]</sup>

Parameter	Description	Test Conditions	SOIC Package	STSOP Package	TSOP Package	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	48.67	32.56	33.01	°C/W
$\Theta_{\sf JC}$	Thermal Resistance (Junction to Case)		25.86	3.59	3.42	°C/W

#### **AC Test Loads and Waveform**

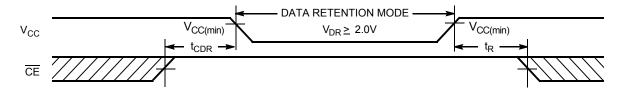


Parameters	Value	Unit
R1	1800	Ω
R2	990	Ω
R <sub>TH</sub>	639	Ω
V <sub>TH</sub>	1.77	V

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions			<b>Typ</b> <sup>[3]</sup>	Max	Unit
$V_{DR}$	V <sub>CC</sub> for Data Retention			2			V
I <sub>CCDR</sub> [8]	Data Retention Current	$V_{CC} = V_{DR}, \overline{CE}_1 \ge V_{CC} - 0.2V \text{ or } CE_2 \le 0.2V, \ V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$	Ind'I/Auto-A			4	μΑ
		$V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$	Auto-E			30	μΑ
t <sub>CDR</sub> <sup>[9]</sup>	Chip Deselect to Data Retention Time			0			ns
t <sub>R</sub> <sup>[10]</sup>	Operation Recovery Time			t <sub>RC</sub>			ns

#### Data Retention Waveform[11]



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<sup>10.</sup> Full device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

11. CE is the logical combination of CE₁ and CE₂. When CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH.



# Switching Characteristics (Over the Operating Range)[12]

D	December 1	45 ns (Inc	d'I/Auto-A)	55 ns (	Auto-E)	11
Parameter	Description	Min	Max	Min	Max	Unit
Read Cycle			•		•	•
t <sub>RC</sub>	Read Cycle Time	45		55		ns
t <sub>AA</sub>	Address to Data Valid		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Data Valid		45		55	ns
t <sub>DOE</sub>	OE LOW to Data Valid		22		25	ns
t <sub>LZOE</sub>	OE LOW to Low-Z <sup>[13]</sup>	5		5		ns
t <sub>HZOE</sub>	OE HIGH to High-Z <sup>[13, 14]</sup>		18		20	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}_1$ LOW and $\text{CE}_2$ HIGH to Low-Z <sup>[13]</sup>	10		10		ns
t <sub>HZCE</sub>	CE <sub>1</sub> HIGH or CE <sub>2</sub> LOW to High-Z <sup>[13, 14]</sup>		18		20	ns
t <sub>PU</sub>	CE₁ LOW and CE₂ HIGH to Power Up	0		0		ns
t <sub>PD</sub>	CE₁ HIGH or CE₂ LOW to Power Down		45		55	ns
Write Cycle <sup>[15]</sup>	<u>'</u>		<u>'</u>		•	
t <sub>WC</sub>	Write Cycle Time	45		55		ns
t <sub>SCE</sub>	CE₁ LOW and CE₂ HIGH to Write End	35		40		ns
t <sub>AW</sub>	Address Setup to Write End	35		40		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	WE Pulse Width	35		40		ns
t <sub>SD</sub>	Data Setup to Write End	25		25		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	WE LOW to High-Z <sup>[13, 14]</sup>		18		20	ns
t <sub>LZWE</sub>	WE HIGH to Low-Z <sup>[13]</sup>	10		10		ns

 <sup>12.</sup> Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns (1V/ns) or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in the "" on page 5.
 13. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZCE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
 14. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
 15. The internal Write time of the memory is defined by the overlap of WE, CE = V<sub>IL</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.



## **Switching Waveforms**

Figure 1. Read Cycle 1 (Address Transition Controlled) [16, 17]

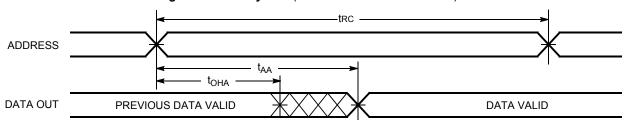


Figure 2. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [17, 18, 19]

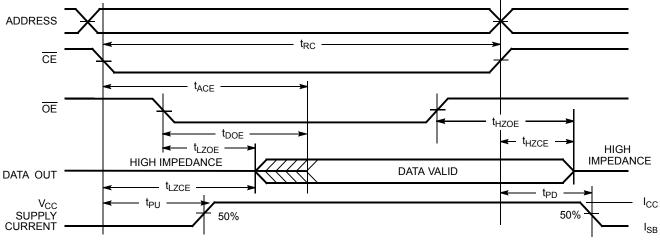
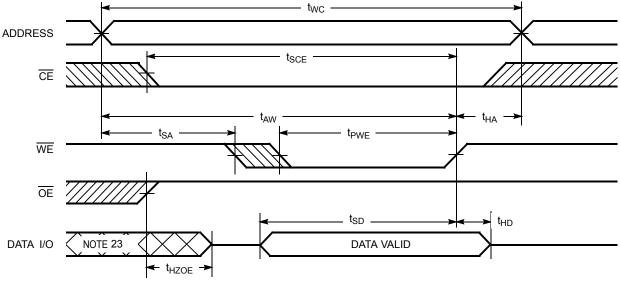


Figure 3. Write Cycle No. 1 (WE Controlled) [19, 20, 21, 22]



#### Notes:

- 16. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{CE}_2 = V_{IH}$ .

  17.  $\overline{WE}$  is HIGH for read cycle.

- 11. WE is Filled to lead cycle.
   18. Address valid before or similar to \(\overline{CE}\_1\) transition LOW and CE<sub>2</sub> transition HIGH.
   19. CE is the logical combination of CE<sub>1</sub> and CE<sub>2</sub>. When CE<sub>1</sub> is LOW and CE<sub>2</sub> is HIGH, \(\overline{CE}\) is LOW; when \(\overline{CE}\_1\) is HIGH or CE<sub>2</sub> is LOW, \(\overline{CE}\) is HIGH.
   20. The internal Write time of the memory is defined by the overlap of \(\overline{WE}\), \(\overline{CE} = V\_{IL}\). All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 21. Data I/O is high impedance if  $\overline{OE}$  =  $V_{IH}$ .

  22. If  $\overline{CE}_1$  goes HIGH or  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 23. During this period, the I/Os are in output state and input signals must not be applied.



## Switching Waveforms (continued)

Figure 4. Write Cycle No. 2 (CE1 or CE2 Controlled) [24, 25, 26, 27]

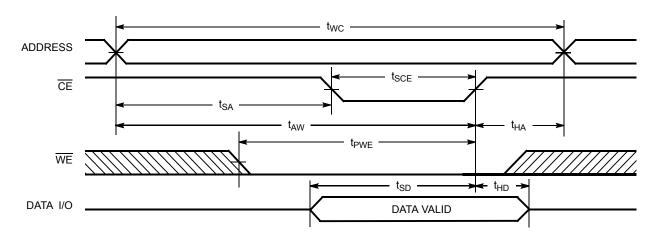
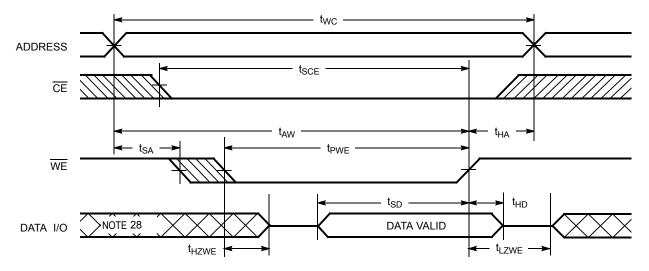


Figure 5. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [24, 27]



#### Notes

<sup>24.</sup> CE is the logical combination of  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\overline{\text{CE}}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\overline{\text{CE}}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

25. The internal Write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}$  =  $V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

<sup>26.</sup> Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

27. If  $\overline{CE}_1$  goes HIGH or  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.

28. During this period, the I/Os are in output state and input signals must not be applied.



#### **Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	Inputs/Outputs	Inputs/Outputs Mode	
Н	X <sup>[29]</sup>	X	Х	High-Z Deselect/Power down S		Standby (I <sub>SB</sub> )
X <sup>[29]</sup>	L	Х	Х	High-Z	igh-Z Deselect/Power down S	
L	Н	Н	L	Data Out	Out Read Ad	
L	Н	L	Х	Data In	In Write Active	
L	Н	Н	Н	High-Z	ligh-Z Selected, Outputs Disabled Active (I <sub>C</sub>	

Note
29. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

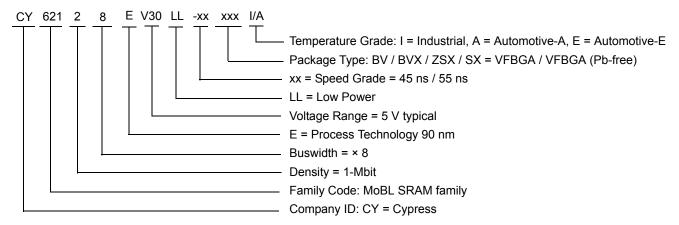


# **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128ELL-45SXI	51-85081	32-pin 450-Mil SOIC (Pb-free)	Industrial
	CY62128ELL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	
	CY62128ELL-45ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
45	CY62128ELL-45SXA	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-A
	CY62128ELL-45ZXA	51-85056	32-pin TSOP Type I (Pb-free)	
55	CY62128ELL-55SXE	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-E
	CY62128ELL-55ZAXE	51-85094	32-pin STSOP (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

## **Ordering Code Definitions**



[+] Feedback



# **Package Diagrams**

Figure 6. 32-pin (450 Mil) Molded SOIC (51-85081)

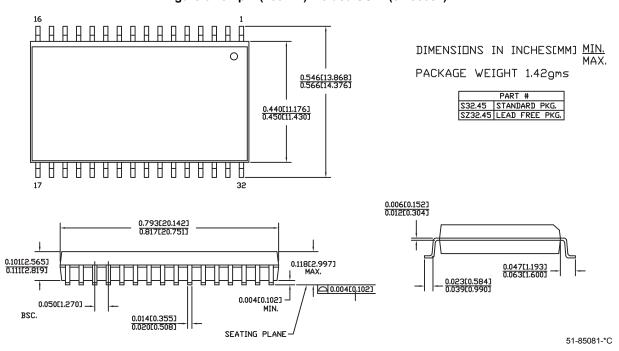




Figure 7. 32-pin Shrunk Thin Small Outline Package (8 x 13.4 mm) (51-85094)

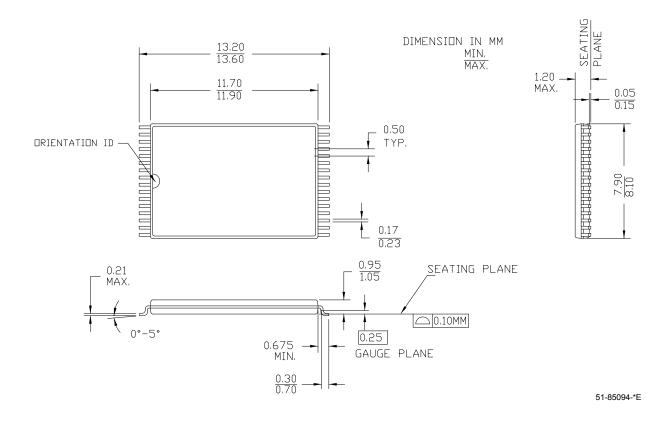
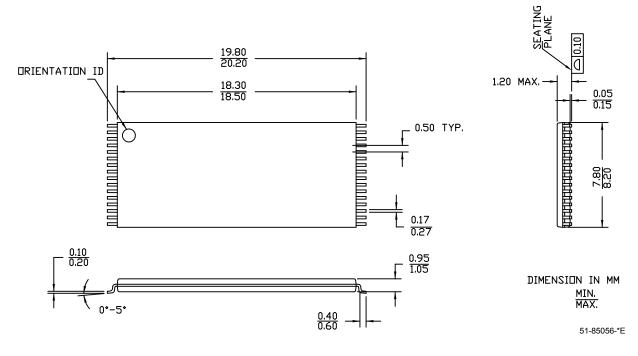


Figure 8. 32-pin Thin Small Outline Package Type I (8 x 20 mm) (51-85056)



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# **Document History Page**

Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	203120	See ECN	AJU	New data sheet
*A	299472	See ECN	SYT	Converted from Advance Information to Preliminary Changed $t_{OHA}$ from 6 ns to 10 ns for both 35 ns and 45 ns, respectively Changed $t_{DOE}$ from 15 ns to 18 ns for 35 ns speed bin Changed $t_{HZOE}$ , $t_{HZWE}$ from 12 and 15 ns to 15 and 18 ns for the 35 and 45 ns speed bins, respectively Changed $t_{HZCE}$ from 12 and 15 ns to 18 and 22 ns for the 35 and 45 ns speed bins, respectively Changed $t_{SCE}$ from 25 and 40 ns to 30 and 35 ns for the 35 and 45 ns speed bins, respectively Changed $t_{SCE}$ from 15 and 20 ns to 18 and 22 ns for the 35 and 45 ns speed bins, respectively Changed $t_{SD}$ from 15 and 20 ns to 18 and 22 ns for the 35 and 45 ns speed bin respectively Added Pb-free package information Added footnote #9 Changed operating range for SOIC package from Commercial to Industrial Modified signal transition time from 5 ns to 3 ns in footnote #11 Changed max of $t_{SB1}$ , $t_{SB2}$ and $t_{CCDR}$ from 1.0 $t_{CDR}$ from 1.0 $t_{CDR}$
*B	461631	See ECN	NXR	Converted from Preliminary to Final Included Automotive Range and 55 ns speed bin Removed 35 ns speed bin Removed "L" version of CY62128E Removed Reverse TSOP I package from Product offering Changed I <sub>CC (Typ)</sub> from 8 mA to 11 mA and I <sub>CC (max)</sub> from 12 mA to 16 mA for $=f_{max}$ Changed I <sub>CC (max)</sub> from 1.5 mA to 2.0 mA for f = 1 MHz Removed I <sub>SB1</sub> DC Specs from Electrical characteristics table Changed I <sub>SB2 (max)</sub> from 1.5 $\mu$ A to 4 $\mu$ A Changed I <sub>SB2 (max)</sub> from 0.5 $\mu$ A to 1 $\mu$ A Changed I <sub>CCDR (max)</sub> from 1.5 $\mu$ A to 4 $\mu$ A Changed the AC Test load Capacitance value from 100 pF to 30 pF Changed t $_{LZOE}$ from 3 to 5 ns Changed t $_{LZCE}$ from 6 to 10 ns Changed t $_{LZCE}$ from 22 to 18 ns Changed t $_{LZWE}$ from 30 to 35 ns Changed t $_{LZWE}$ from 6 to 10 ns Updated the Ordering Information Table
*C	464721	See ECN	NXR	Updated the Block Diagram on page # 1
*D	563144	See ECN	AJU	Added footnote 4 on page 2
*E	1024520	See ECN	VKN	Added Automotive-A information Converted Automotive-E specs to final Added footnote #9 related to I <sub>SB2</sub> and I <sub>CCDR</sub> Updated Ordering Information table
*F	2548575	08/05/08	NXR	Corrected typo error in Ordering Information table
*G	2934396	06/03/10	VKN	Added footnote #22 related to chip enable Updated package diagrams Updated template
*H	3113780	12/17/2010	PRAS	Updated Logic Block Diagram. Added Ordering Code Definitions.



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