FAIRCHILD SEMICONDUCTOR™

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74VCX16835
Low Voltage 18-Bit Universal Bus Driver with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16835 low voltage 18-bit universal bus driver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow is controlled by output-enable ($\overline{OE}$), latch-enable (LE), and clock (CLK) inputs. The device operates in Transparent Mode when LE is held HIGH. The device operates in clocked mode when LE is LOW and CLK is toggled. Data transfers from the Inputs (I_n) to Ouputs (O_n) on a Positive Edge Transition of the Clock. When $\overline{OE}$ is LOW, the output data is enabled. When $\overline{OE}$ is HIGH the output port is in a high impedance state.

The 74VCX16835 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74VCX16835 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- Compatible with PC100 DIMM module specifications
- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (CLK to O_n)
  - 4.2ns max for 3.0V to 3.6V V_{CC}
  - 5.2ns max for 2.3V to 2.7V V_{CC}
  - 9.2ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
  - ±24mA @ 3.0V
  - ±18mA @ 2.3V
  - ±6mA @ 1.65V
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} (OE to GND) through a pulldown resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver.

Ordering Code:

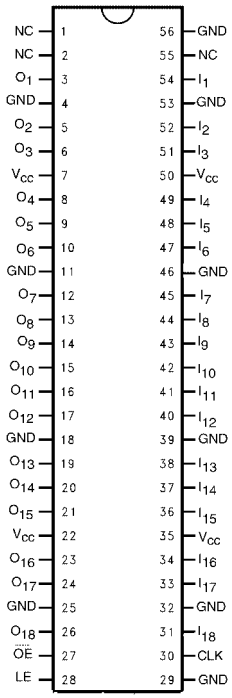
Order Number	Package Number	Package Description
74VCX16835GX (Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74VCX16835MTD (Note 3)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: BGA package available in Tape and Reel only.

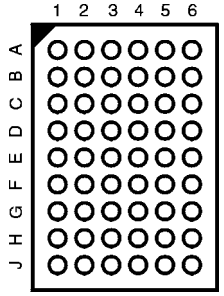
Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable Input
CLK	Clock Input
I_1 - I_{18}	Data Inputs
O_1 - O_{18}	3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_2	O_1	NC	GND	I_1	I_2
B	O_4	O_3	NC	NC	I_3	I_4
C	O_6	O_5	V_{CC}	V_{CC}	I_5	I_6
D	O_8	O_7	GND	GND	I_7	I_8
E	O_{10}	O_9	GND	GND	I_9	I_{10}
F	O_{12}	O_{11}	GND	GND	I_{11}	I_{12}
G	O_{14}	O_{13}	V_{CC}	V_{CC}	I_{13}	I_{14}
H	O_{16}	O_{15}	$\overline{OE}$	CLK	I_{15}	I_{16}
J	O_{17}	O_{18}	LE	GND	I_{18}	I_{17}

Truth Table

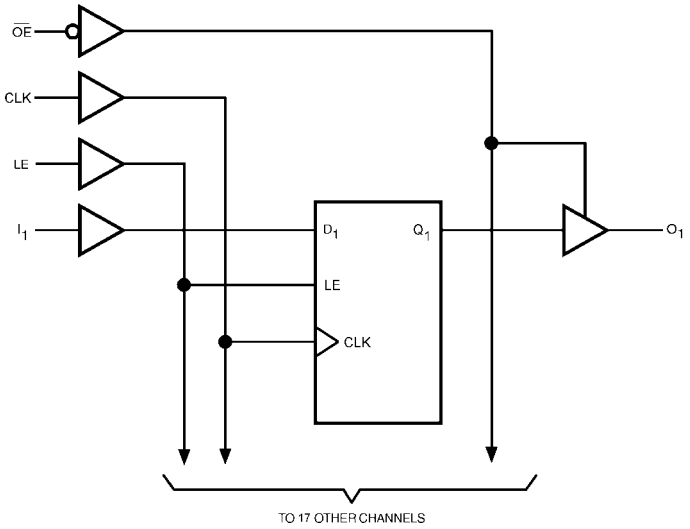
Inputs				Outputs
$\overline{OE}$	LE	CLK	I_n	O_n
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	O_0 (Note 4)
L	L	L	X	O_0 (Note 5)

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Clock Transition

Note 4: Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

Note 5: Output level before the indicated steady-state input conditions were established.

Logic Diagram



Absolute Maximum Ratings (Note 6)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 7)	−0.5 to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or Ground)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 8)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.3V to 2.7V	±18 mA
V_{CC} = 1.65V to 2.3V	±6 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 6: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 7: I_O Absolute Maximum Rating must be observed.

Note 8: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics ($2.7V < V_{CC} \leq 3.6V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0V ≤ V_I ≤ 3.6V	2.7–3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0V ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}	2.7–3.6		±10	µA
I_{OFF}	Power Off Leakage Current	0V ≤ (V_I, V_O) ≤ 3.6V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	µA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 9)			±20	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		750	µA

Note 9: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($2.3V \le V_{CC} \le 2.7V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.6		V
V_{IL}	LOW Level Input Voltage		2.3 - 2.7		0.7	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100\ \mu A$	2.3 -2.7	$V_{CC} - 0.2$		V
		$I_{OH} = -6$ mA	2.3	2.0		
		$I_{OH} = -12$ mA	2.3	1.8		
		$I_{OH} = -18$ mA	2.3	1.7		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\ \mu A$	2.3 - 2.7		0.2	V
		$I_{OL} = 12$mA	2.3		0.4	
		$I_{OL} = 18$ mA	2.3		0.6	
I_I	Input Leakage Current	$0V \le V_I \le 3.6V$	2.3 - 2.7		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0V \le V_O \le 3.6V$	2.3 - 2.7		±10	µA
		$V_I = V_{IH}$ or V_{IL}				
I_{OFF}	Power Off Leakage Current	$0V \le (V_I, V_O) \le 3.6V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 - 2.7		20	µA
		$V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 10)	2.3 - 2.7		±20	

Note 10: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($1.65V \le V_{CC} < 2.3V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 2.3	$0.65 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage		1.65 - 2.3		$0.35 \times V_{CC}$	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100\ \mu A$	1.65 - 2.3	$V_{CC} - 0.2$		V
		$I_{OH} = -6$ mA	1.65	1.25		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\ \mu A$	1.65 - 2.3		0.2	V
		$I_{OL} = 6$mA	1.65		0.3	
I_I	Input Leakage Current	$0V \le V_I \le 3.6V$	1.65 - 2.3		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0V \le V_O \le 3.6V$	1.65 - 2.3		±10	µA
		$V_I = V_{IH}$ or V_{IL}				
I_{OFF}	Power Off Leakage Current	$0V \le (V_I, V_O) \le 3.6V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.65 - 2.3		20	µA
		$V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 11)			±20	

Note 11: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 12)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 30$ pF, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5 \pm 0.2V$		$V_{CC} = 1.8 \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	250		200		100		MHz
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus	0.6	3.3	0.8	4.2	1.5	8.4	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Bus	1.4	4.2	1.5	5.2	2.0	9.2	ns
t_{PHL}, t_{PLH}	Propagation Delay LE to Bus	0.6	3.8	0.8	4.9	1.5	9.8	ns
t_{PZL}, t_{PZH}	Output Enable Time	0.6	3.8	0.8	4.9	1.5	9.8	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	0.6	3.9	0.8	4.5	1.5	7.6	ns
t_S	Setup Time	1.5		1.5		2.5		ns
t_H	Hold Time	0.7		0.7		1.0		ns
t_W	Pulse Width	1.5		1.5		4.0		ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 13)		0.5		0.5		0.75	ns

Note 12: For CL=50pF, add approximately 300ps to the AC maximum specification.

Note 13: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

AC Electrical Characteristics Over Load (Note 14)

Symbol	Parameter	$T_A = -0°C$ to $+85°C$, $R_L = 500\Omega$ $V_{CC} = 3.3V \pm 0.15V$				Units
		$C_L = 0$ pF		$C_L = 50$ pF		
		Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus	0.7	2.1	1.0	3.6	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Bus	1.5	3.0	1.7	4.5	ns
t_{PHL}, t_{PLH}	Propagation Delay LE to Bus	0.7	2.6	1.0	4.1	ns
t_{PZL}, t_{PZH}	Output Enable Time	0.7	2.6	1.0	4.1	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	0.7	2.7	1.0	4.2	ns
t_{PHL}, t_{PLH}	SSO Prop Delay Clock to Bus (Note 15)	1.5	3.3			ns
t_S	Setup Time	1.5		1.5		ns
t_H	Hold Time	0.7		0.7		ns

Note 14: This parameter is guaranteed by characterization but not tested.

Note 15: SSO = Simultaneous Switching Output. Any output combination of LOW-to-HIGH and/or HIGH-to-LOW transition.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	0.35	V
			2.5	0.7	
			3.3	0.9	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	–0.35	V
			2.5	–0.7	
			3.3	–0.9	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	1.3	V
			2.5	1.7	
			3.3	2.0	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance	$V_I = 0V$ or V_{CC}, $V_{CC} = 1.8V$, 2.5V, or 3.3V,	3.5	pF
$C_{I/O}$	Input/Output Capacitance	$V_I = 0V$, or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	5.5	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, f = 10 MHz, $V_{CC} = 1.8V$, 2.5V or 3.3V	13	pF

I_{OUT} - V_{OUT} Characteristics

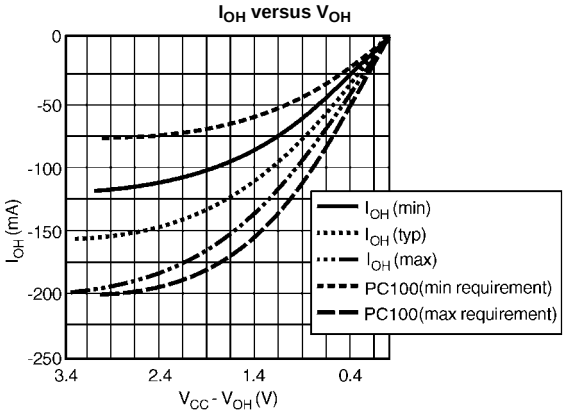


FIGURE 1. Characteristics for Output - Pull Up Driver

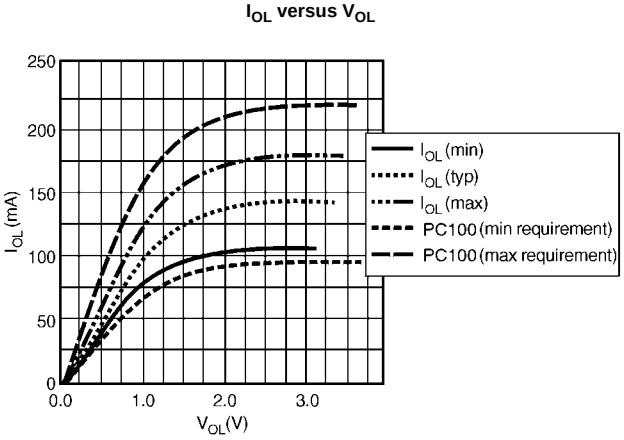


FIGURE 2. Characteristics for Output - Pull Down Driver

AC Loading and Waveforms

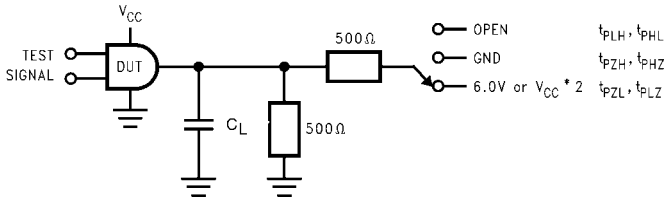


FIGURE 3. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V; 1.8V to ± 0.15V
t_{PZH}, t_{PHZ}	GND

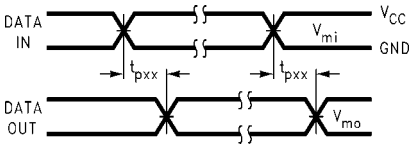


FIGURE 4. Waveform for Inverting and Non-inverting Functions
$t_r = t_f \leq$ 2.0ns, 10% to 90%

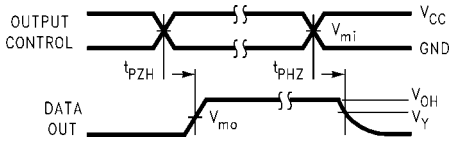


FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic
$t_r = t_f \leq$ 2.0ns, 10% to 90%

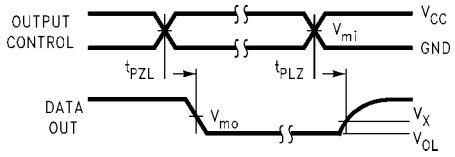
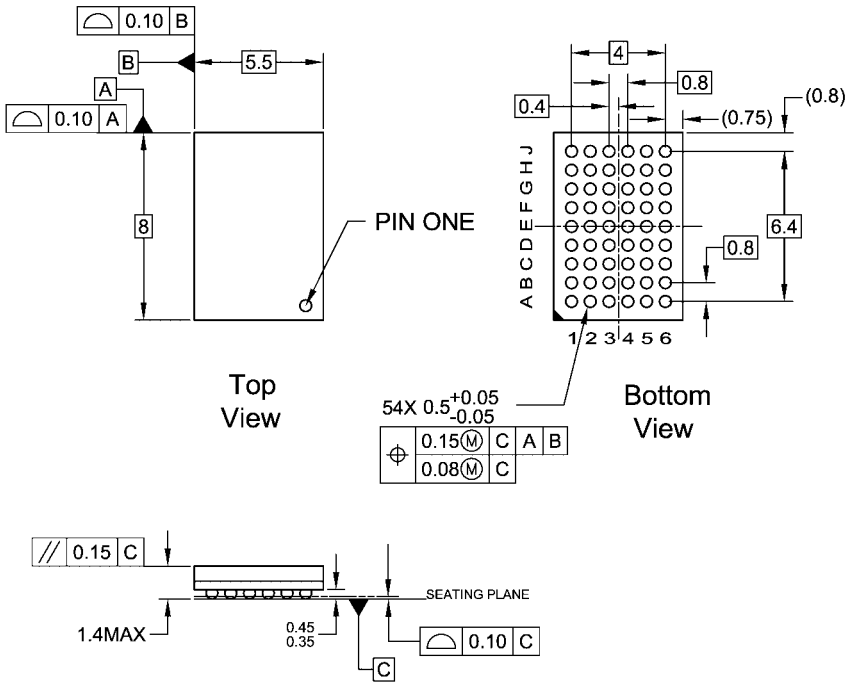


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic
$t_r = t_f \leq$ 2.0ns, 10% to 90%

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8 ± 0.15V**
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

Physical Dimensions inches (millimeters) unless otherwise noted



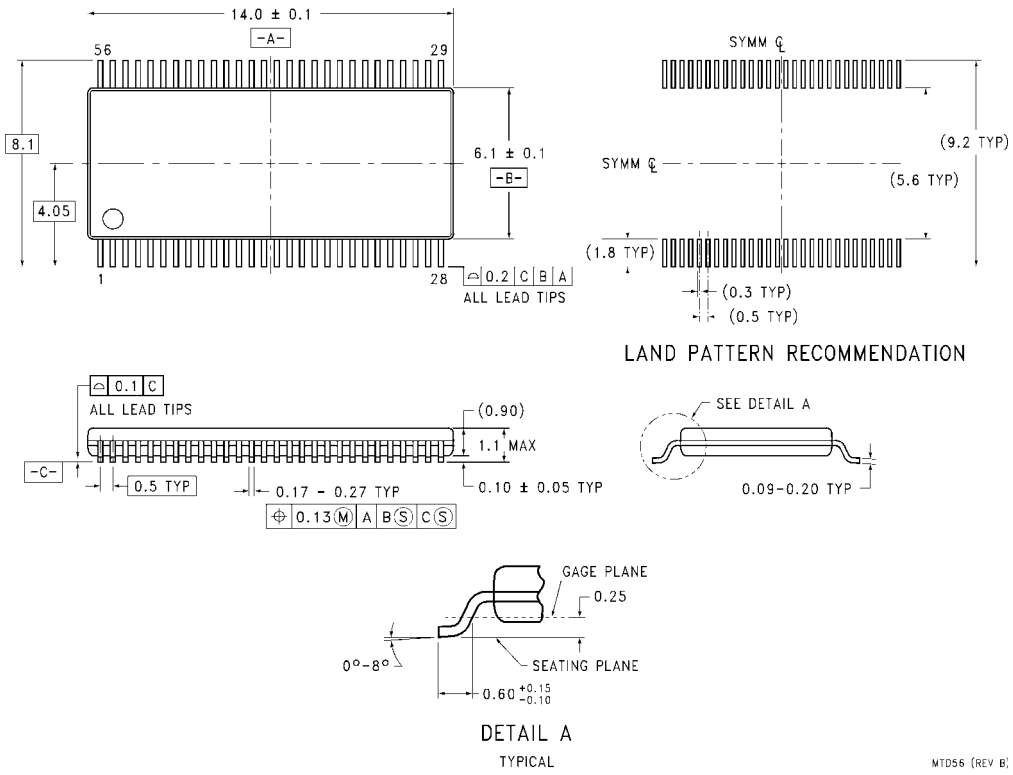
NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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