Low Power Level Shifter

ON Semiconductor™

http://onsemi.com

The NCN6011 is a level shifter analog circuit designed to translate the voltages between a SIM Card and an external microcontroller. The device handles all the signals needed to control the data transaction between the external Card and the MPU.

Features

- 2.7 to 6.0 V Input and/or Output Voltage Range
- 500 nA Quiescent Supply Current
- All Pins are Fully ESD Protected
- Supports 10 MHz Clock
- Provides a Logic I/O Enable Function
- Rx/Tx Communication Capability

Typical Applications

- SIM/GSM/SMARTCARD Interface

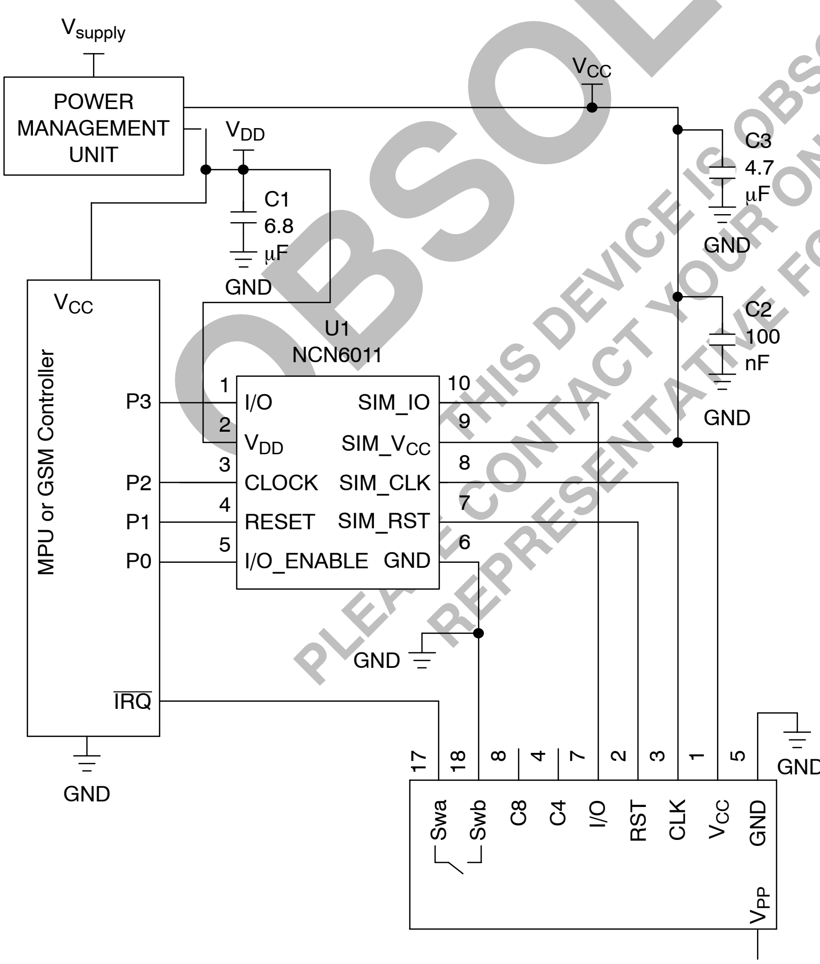
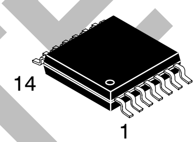
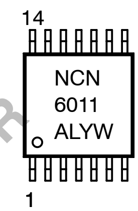


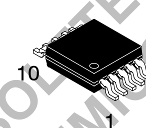
Figure 1. Typical Interface Application

MARKING DIAGRAMS

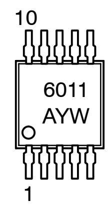


TSSOP−14
DTB SUFFIX
CASE 948G





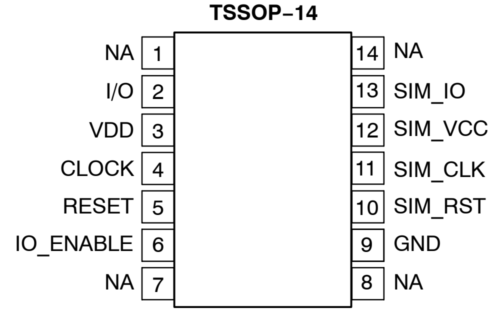
Micro−10
DM SUFFIX
CASE 846B



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week

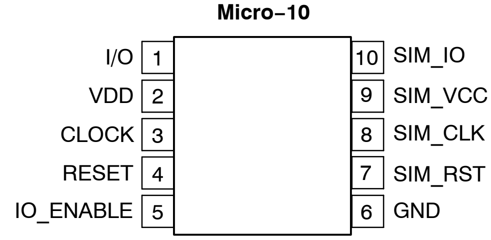
PIN CONNECTIONS

TSSOP−14



(Top View)

Micro−10



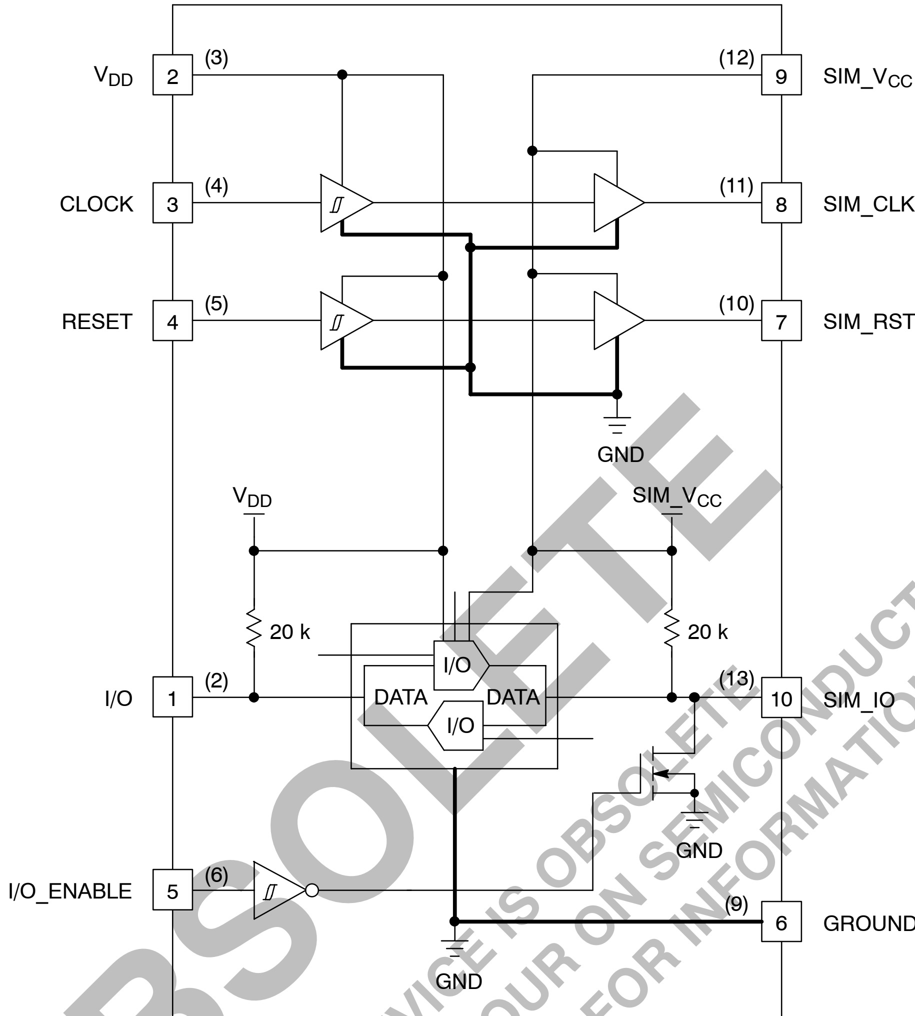
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

July, 2006 − Rev. 4

Publication Order Number:
NCN6011/D



NOTES:
1. Numbers in parenthesis adjacent to the pins are related to the TSSOP−14 package.
2. TSSOP−14 package Pins 1, 7, 8 and 14 are not connected.

Figure 2. Block Diagram

ABBREVIATIONS

CLOCK	Input Logic Clock
RESET	Input Logic Reset
VDD	Interface Power Supply Input
SIM_VCC	Interface IC Card Power Supply Output
SIM_CLK	Interface IC Card Clock Output
SIM_RST	Interface IC Card Reset Output
SIM_IO	Interface IC Card I/O Signal Line
Class A	5.0 V Smart Card
Class B	3.0 V Smart Card

PIN DESCRIPTIONS **(Pin numbers in parenthesis are related to the TSSOP−14 package)** **(Pin numbers in bold are related to the MIcro−10 package)**

Pin	Name	Type	Description
(1)	–	NA	No Connection. (TSSOP−14 Only)
1 (2)	I/O	INPUT	This pin is connected to an external microcontroller. A bidirectional level translator adapts the serial I/O signal between the smart card and the external controller. A built−in constant 20 kΩ typical resistor provides a high impedance state when not activated.
2 (3)	V_{DD}	POWER	This pin is connected to the system controller power supply and the input voltage can range from 2.7 to 6.0 V.
3 (4)	CLOCK	INPUT	The clock signal, coming from the external controller, must have a Duty Cycle within the Min/Max limits defined by the specification (typically 50%). The built−in level shifter translates the input signal to the external SIM card voltage supply.
4 (5)	RESET	INPUT	The RESET signal present at this pin is provided by the MPU. The internal level shifter translates the level according to the voltages applied to pin 3 and pin 12.
5 (6)	IO_ENABLE	INPUT	This logic input pin forces SIM_IO pin to Low when IO_ENABLE = Low, leaving this signal High when IO_ENABLE = High. The signal is not latched and the SIM_IO pin is released to a logic High when IO_ENABLE = High. When this condition is met, the SIM_IO logic status depends upon the signal presence pin I/O. When the MPU uses two different channels to exchange data with the SIM card, the IO_ENABLE pin can be used to as a Write line to the external card, the I/O pin being used to Read data from the SIM card.
(7)	–	NA	No Connection. (TSSOP−14 Only)
(8)	–	NA	No Connection. (TSSOP−14 Only)
6 (9)	GND	GROUND	This pin is the GROUND reference for the integrated circuit and associated signals. High frequency layout techniques are requested to connect the GND pin to the external functions.
7 (10)	SIM_RST	OUTPUT	This pin is connected to the RST pin of the card connector. A voltage level translator adapts the external RESET signal (coming from the MPU) to the smart card.
8 (11)	SIM_CLK	OUTPUT	This pin is connected to the CLK pin of the card connector. The CLOCK signal comes from the external clock generator. The internal voltage level shifter adapts the clock signal flowing through this link. Care must be observed to prevent AC coupling with adjacent lines and signals PCB tracks.
9 (12)	SIM_VCC	POWER	This pin is connected to the smart card VCC power supply pin. The voltage, provided by an external power supply, can range from 2.7 V to 6.0 V. The NCN6011 does not regulate or protect the voltage supply applied to the external card.
10 (13)	SIM_I/O	OUTPUT	This pin handles the connection to the serial I/O of the card connector. A bidirectional voltage level translator adapts the serial I/O signal between the card and the microcontroller. A 20 kΩ typical pull up resistor provides a High impedance state for the SIM card I/O link.
(14)	–	NA	No Connection. (TSSOP−14 Only)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply	V_{DD}	7.0 V	V
External Card and Level Shifter Power Supply	SIM_VCC	7.0 V	V
Digital Input Voltage Digital Input Current	RESET, IO_ENABLE	$-0.3 \le V \le V_{DD}$ 1.0	V mA
Digital Input Voltage Digital Input Current	CLOCK	$-0.3 \le V \le V_{DD}$ 1.0	V mA
Digital Input Voltage Digital Input Current	I/O	$-0.3 \le V \le V_{DD}$ 1.0	V mA
Digital Output Voltage Digital Output Current	SIM_RST	$-0.3 \le V \le$ SIM_VCC 25	V mA
Digital Output/Input Voltage Digital Output/Input Current	SIM_I/O	$-0.3 \le V \le$ SIM_VCC 25	V mA
Digital Output Voltage Digital Output Current	SIM_CLK	$-0.3 \le V \le$ SIM_VCC 50	V mA
Human Body Model: R = 1500 Ω, C = 100 pF SIM card side, pins **7, 8, 9, 10** (10, 11, 12, 13) All other pins	ESD	 4.0 2.0	 kV kV
Micro−10 Package Power Dissipation @ T_A = +85°C Thermal Resistance Junction to Air	 P_D R_{THhja}	 200 200	 mW °C/W
TSSOP−14 Package Power Dissipation @ T_A = +85°C Thermal Resistance Junction to Air	 P_D R_{THhja}	 320 125	 mW °C/W
Operating Ambient Temperature Range	T_A	−25 to +85	°C
Operating Junction Temperature Range	T_J	−25 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

POWER SUPPLY SECTION (–25°C to +85°C ambient temperature, unless otherwise noted)
(Pin numbers in parenthesis are related to the TSSOP–14 package)
(Pin numbers in bold are related to the MIcro–10 package)

Rating	Symbol	Pin	Min	Typ	Max	Unit
Power Supply	V_{DD}	**2** (3)	2.7	–	6.0	V
Standby Supply Current, CLOCK = L, I/O = H, SIM_VCC = 3.0 V, No SIM Card Inserted	I_{VDD}	**2** (3)	–	0.5	2.0	μA
Input External Power Supply	SIM_VCC	**9** (12)	2.7	–	6.0	V
Standby Current, SIM_VCC = 3.0 V, I/O = H, No SIM Card Inserted, CLOCK = L	I_{VCC}	**9** (12)	–	0.2	0.5	μA
Power Supply Normal Operating Current @ VDD = +5.0 V, SIM_VCC = +5.0 V, CLOCK = 5.0 MHz, RESET = H, IO_ENABLE = H, I/O Data = 100 kHz	I_{DD}	**2** (3)	–	230	–	μA
Power Supply Normal Operating Current @ VDD = +5.0 V, SIM_VCC = +5.0 V, CLOCK = 5.0 MHz, RESET = H, IO_ENABLE = H, I/O Data = H	I_{DD}	**2** (3)	–	80	–	μA
Card Level Shifter Operating Current @ VDD = +5.0 V, SIM_VCC = +5.0 V, CLOCK = 5.0 MHz, RESET = H, IO_ENABLE = H, I/O Data = 100 kHz	I_{CC}	**9** (12)	–	1.50	–	mA
Card Level Shifter Operating Current @ VDD = +5.0 V, SIM_VCC = +5.0 V, CLOCK = 5.0 MHz, RESET = H, IO_ENABLE = H, I/O Data = H	I_{CC}	**9** (12)	–	1.30	–	mA

DIGITAL INPUT SECTION: CLOCK, RESET, I/O, IO_ENABLE
(–25°C to +85°C ambient temperature, unless otherwise noted) (Note 1)

Rating	Symbol	Pin	Min	Typ	Max	Unit
CLOCK, RESET, IO_ENABLE High Level Input Voltage Low Level Input Voltage Input Rise Time Input Fall Time Input Capacitance	 V_{IH} V_{IL} tr tf Cin	 **1, 3,** **4, 5** (2, 4, 5, 6)	 0.7 * V_{DD}	–	 V_{CC} 0.3 * V_{DD} 50 50 10	 V V ns ns pF
Input @ Duty Cycle = 50% ±1% (Note 2) Clock Rise Time Clock Fall Time Input Clock Capacitance	CLOCK	**3** (4)	–	–	5.0 50 50 10	MHz ns ns pF
Input/Output Data Transfer Frequency I/O Rise Time I/O Fall Time Input I/O Capacitance	I/O	**1** (2)	–	–	160 0.8 0.8 10	kHz μs μs pF

1. Digital inputs undershoot < –0.30 V, Digital inputs overshoot < 0.30 V.
2. The SIM_CLK clock can operate up to 10 MHz, but, in this case, the rise and fall time are not guaranteed to be fully within the GSM specification over the temperature range.

SIM INTERFACE SECTION (Note 3)

Rating	Symbol	Pin	Min	Typ	Max	Unit
SIM_VCC = +5.0 V	SIM_RST	**7**				
Output RESET V_{OH} @ Irst = +200 μA		(10)	SIM_VCC − 0.7 V		SIM_VCC	V
Output RESET V_{OL} @ Irst = −200 μA			0		0.6	V
Output RESET Rise Time @ Cout = 30 pF					100	ns
Output RESET Fall Time @ Cout = 30 pF					100	ns
SIM_VCC = +3.0 V						
Output RESET V_{OH} @ Irst = +200 μA			0.8 * SIM_VCC		SIM_VCC	V
Output RESET V_{OL} @ Irst = −200 μA			0		0.2 * SIM_VCC	V
Output RESET Rise Time @ Cout = 30 pF					100	ns
Output RESET Fall Time @ Cout = 30 pF					100	ns
SIM_VCC = +5.0 V	SIM_CLK	**8**				
Output Duty Cycle @ Fin = 5.0 MHz DC = 50% ± 1%		(11)	40		60	%
Output SIM_CLK Rise Time @ Cout = 30 pF					18	ns
Output SIM_CLK Fall Time @ Cout = 30 pF					18	ns
Output V_{OH} @ Iclk = +20 μA			0.7 * SIM_VCC		SIM_VCC	V
Output V_{OL} @ Iclk = −200 μA			0		+0.5	V
SIM_VCC = +3.0 V						
Output Duty Cycle @ Fin = 5.0 MHz DC = 50% ± 1%			40		60	%
Output SIM_CLK Rise Time @ Cout = 30 pF					18	ns
Output SIM_CLK Fall Time @ Cout = 30 pF					18	ns
Output V_{OH} @ Iclk = +20 μA			0.7 * SIM_VCC		SIM_VCC	V
Output V_{OL} @ Iclk = −20 μA			0		0.2 * SIM_VCC	V
SIM_VCC = +5.0 V @ IO_ENABLE = H	SIM_I/O	**10**				
SIM_I/O Data Transfer Frequency		(13)			160	kHz
SIM_I/O Rise Time @ Cout = 30 pF					0.8	μs
SIM_I/O Fall Time @ Cout = 30 pF					0.8	μs
Output V_{OH} @ ISIM_IO = +20 μA, $V_{IH} = V_{DD}$			0.7 * SIM_VCC		SIM_VCC	V
Output V_{OL} @ ISIM_IO = −1.0 mA, I/O V_{IL} = 0 V			0		0.4	V
SIM_VCC = +3.0 V @ IO_ENABLE = H						
SIM_I/O Data Transfer Frequency					160	kHz
SIM_I/O Rise Time @ Cout = 30 pF					0.8	μs
SIM_I/O Fall Time @ Cout = 30 pF					0.8	μs
Output V_{OH} @ ISIM_IO = +20 μA, $V_{IH} = V_{DD}$			0.7 * SIM_VCC		SIM_VCC	V
Output V_{OL} @ ISIM_IO = −1.0 mA, I/O V_{IL} = 0 V			0		0.4	V
SIM_VCC = +5.0 V @ IO_ENABLE = L						
SIM_I/O Fall Time @ Cout = 30 pF				150	800	ns
Output V_{OL} @ ISIM_IO = −1.0 mA, I/O V_{IL} = 0 V			0		0.4	V
SIM_VCC = +3.0 V @ IO_ENABLE = L						
SIM_I/O Fall Time @ Cout = 30 pF				150	800	ns
Output V_{OL} @ ISIM_IO = −1.0 mA, I/O V_{IL} = 0 V			0		0.4	V
SIM_VCC = +5.0 V @ I/O = H, IO_ENABLE Returns to High						
SIM_I/O Rise Time @ Cout = 30 pF				2.0		μs
SIM_VCC = +3.0 V @ I/O = H, IO_ENABLE Returns to High						
SIM_I/O Rise Time @ Cout = 30 pF				1.5		μs
I/O Pull Up Resistor	I/O_{RPLD}	**1** (2)	13	20		kΩ
Card I/O Pull Up Resistor	SIM_I/O_{RPLD}	**10** (13)	13	20		kΩ

3. SIM logic input undershoot < −0.30 V, SIM logic input overshoot < 0.30 V.

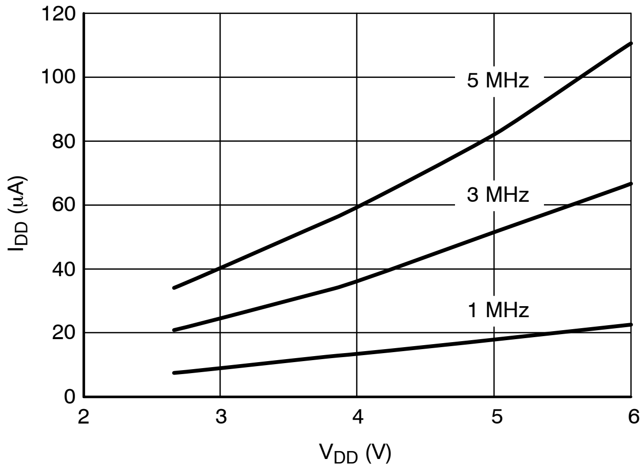


Figure 3. SIM Supply Current as a Function of the V_{DD} Voltage, I/O = High

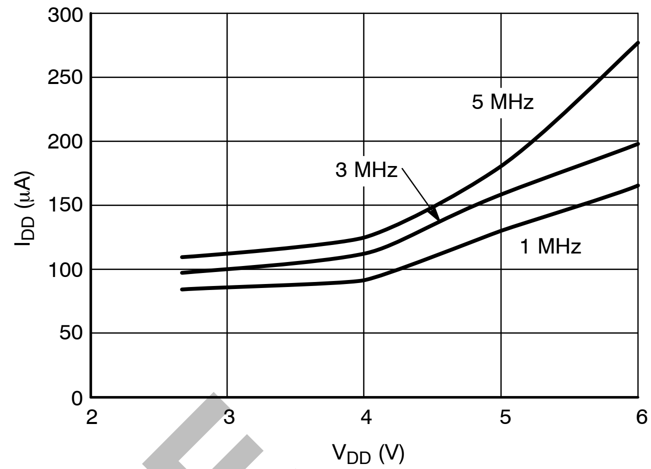


Figure 4. SIM Supply Current as a Function of the V_{DD} Voltage, I/O = 100 kHz Data Transfer

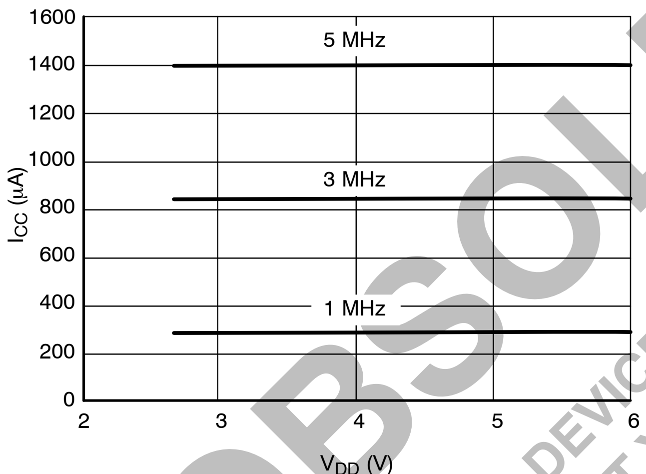


Figure 5. Power Supply Current as Function of the V_{CC} Input Voltage, I/O = High

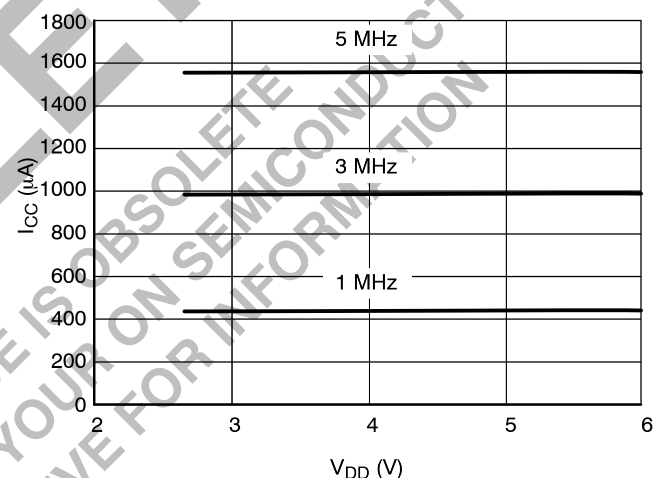


Figure 6. Power Supply Current as Function of the V_{CC} Input Voltage, I/O = 100 kHz Data Transfer

Level Shifters

The built−in level shifters accommodate the differential voltage between the external MPU and the SIM card. Neither the logic nor the functions of the SIM signals are affected by the interface.

The NCN6011 does not regulate the SIM_VCC, nor does it detect the overload current.

Bidirectional Level Shifter

The NCN6011 carries out the voltage difference between the MPU and the Smart Card I/O signals. When the start sequence is completed, and if no failures have been detected, the device becomes essentially transparent for the data transferred on the I/O line. To fulfill the ISO7816−3 specification, both sides of the I/O line have built−in pulsed circuitry to accelerate the signal rise transient. The I/O line is connected on both sides of the interface by a NMOS switch which provide the level shifter and, thanks to its relative high internal impedance, protects the Smart Card in the event of data collision. Such a situation could occur if either the MPU of the smart card forces a signal in the opposite logic level direction.

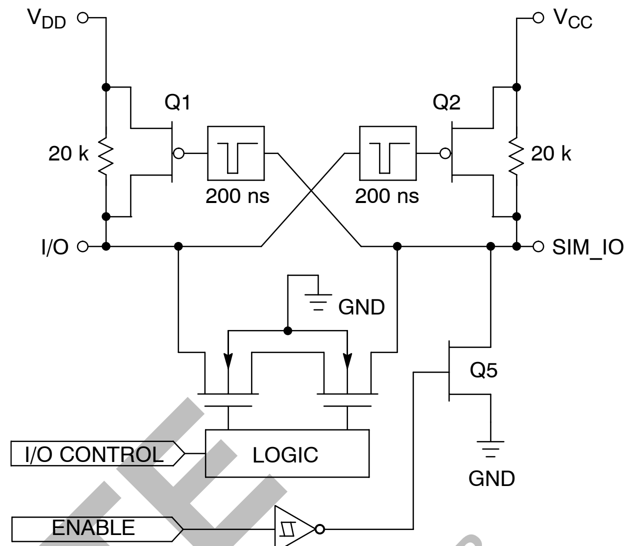


Figure 7. Basic Internal I/O Level Shifter

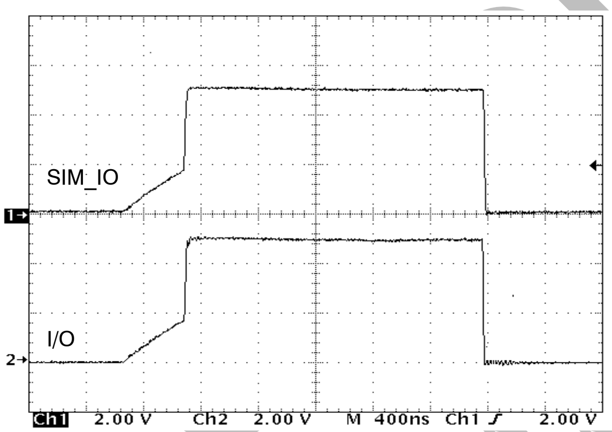


Figure 8. Typical I/O and SIM_IO Waveform, V_{DD} = V_{CC} = 5.0 V, ENABLE = Low

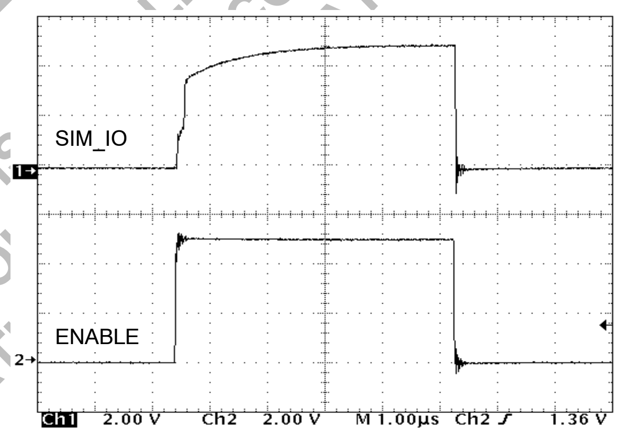


Figure 9. Typical SIM_IO Activated by ENABLE Pin, I/O = High (open drain)

Input Schmitt Triggers

All the Logic Input pins have built−in Schmitt trigger circuits to prevent the NCN6011 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 10.

The output signal is guaranteed to go High when the input voltage is above 0.70*Vbat, and will go Low when the input voltage is below 0.30*Vbat.

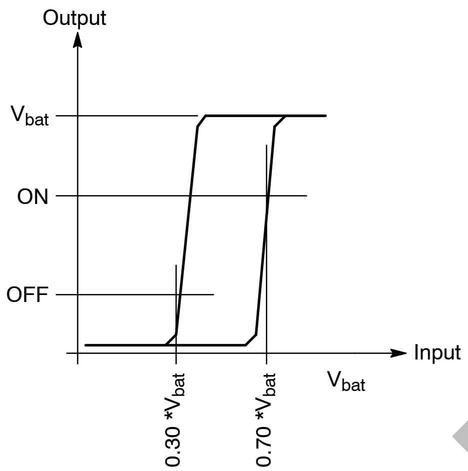


Figure 10. Typical Schmitt Trigger Characteristic

ESD Protection

The NCN6011 includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built−in structures have been designed to handle either 2.0 kV, when related to the microcontroller side, or 4.0 kV when connected with the external contacts. Practically, the SIM_RST, SIMD_CLK and SIM_IO pins can sustain 4.0 kV.

Printed Circuit Board Layout

Since the NCN6011 carries high speed currents together with high frequency clock, the printed circuit board must be carefully designed to avoid the risk of uncontrolled operation of the interface.

Care must be observed to avoid common copper track sharing small signal and high power with a relative high impedance. On top of that, the clock signal (both input and output) shall be properly shielding to minimize the high frequency cross talk between this line and the rest of the circuit. In particular, the SIM_RST signal shall be protected from interference generated by the SIM_CLK line. Such protection can be achieved by surrounding the SIM_CLK track by a copper track connected to ground. Generally speaking, the ground plane shall be as large as possible for a given printed circuit board area.

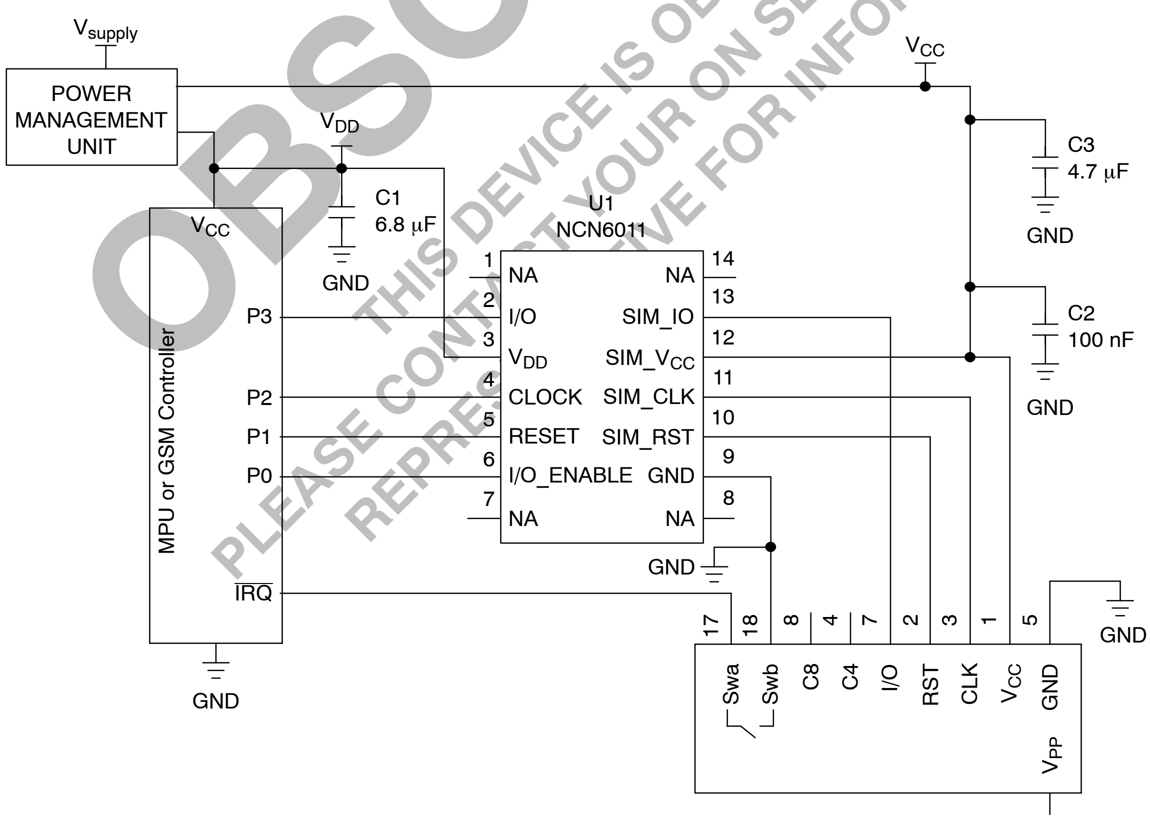


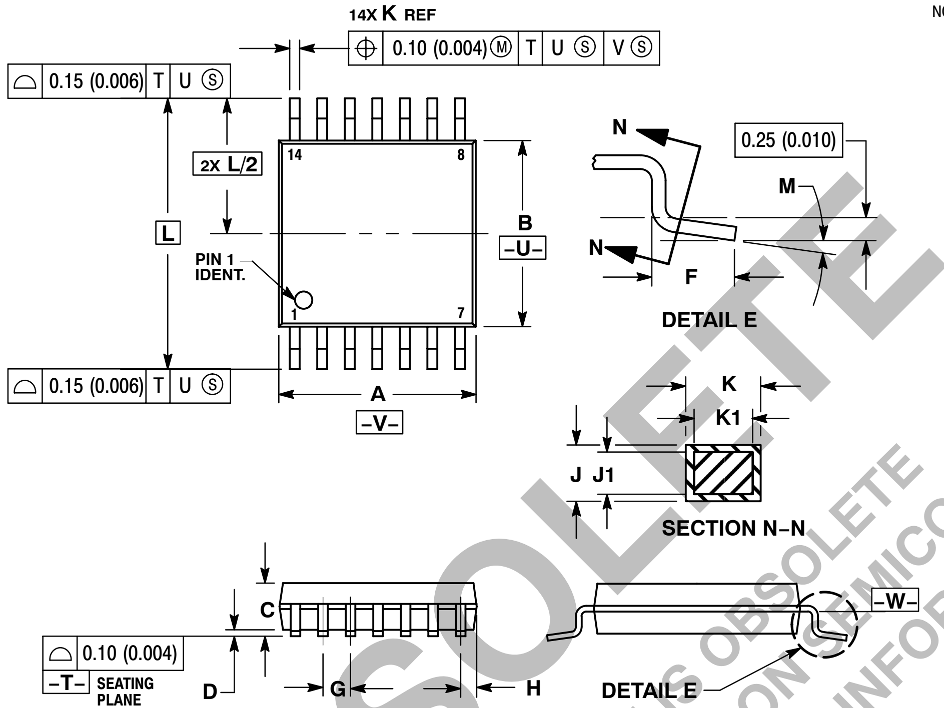
Figure 11. Typical NCN6011/TSSOP−14 Application

ORDERING INFORMATION

Device	Package	Shipping
NCN6011DTB	TSSOP−14	96 Units/Rail
NCN6011DTBR2	TSSOP−14	2500 Tape & Reel
NCN6011DMR2	Micro−10	4000 Tape & Reel

PACKAGE DIMENSIONS

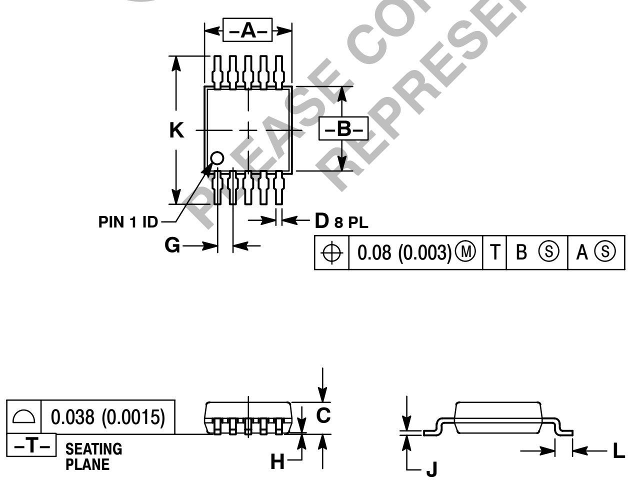
TSSOP−14
DTB SUFFIX
CASE 948G−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Micro−10
DM SUFFIX
CASE 846B−02
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B−01 OBSOLETE. NEW STANDARD 846B−02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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