

# MC10H603, MC100H603

## 9-Bit Latch ECL to TTL Translator

### Description

The MC10H/100H603 is a 9-bit, dual supply ECL to TTL translator. Devices in the ON Semiconductor 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. Latching is controlled by Latch Enable (LEN), and Master Reset (MR) resets the latches. A HIGH on  $\overline{OE/ECL}$  sends the outputs into the high impedance state. All control inputs are ECL level.

The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

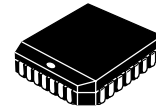
### Features

- 9-Bit Ideal for Byte-Parity Applications
- 3-State TTL Outputs
- Flow-Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- Dual Supply
- 6.0 ns Max Delay into 50 pF, 12 ns into 200 pF (all Outputs Switching)
- PNP TTL Inputs for Low Loading
- Pb-Free Packages are Available\*



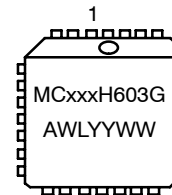
ON Semiconductor®

<http://onsemi.com>



PLCC-28  
FN SUFFIX  
CASE 776

### MARKING DIAGRAM\*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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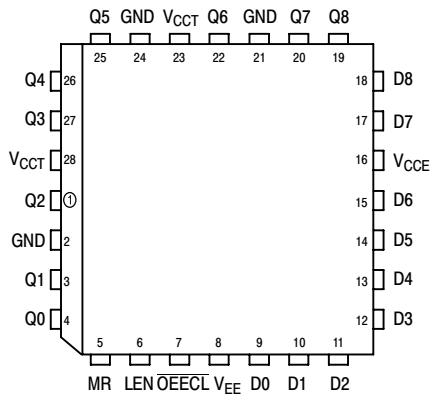


Figure 1. PLCC-28 Pinout (Top View)

Table 1. PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V <sub>CCE</sub>	ECL V <sub>CC</sub> (0 V)
V <sub>CCT</sub>	TTL Supply (+5.0 V)
V <sub>EE</sub>	ECL Supply (-5.2/-4.5 V)
D0 - D8	Data Inputs (ECL)
Q0 - Q8	Data Outputs (TTL)
OE/ECL	3-State Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

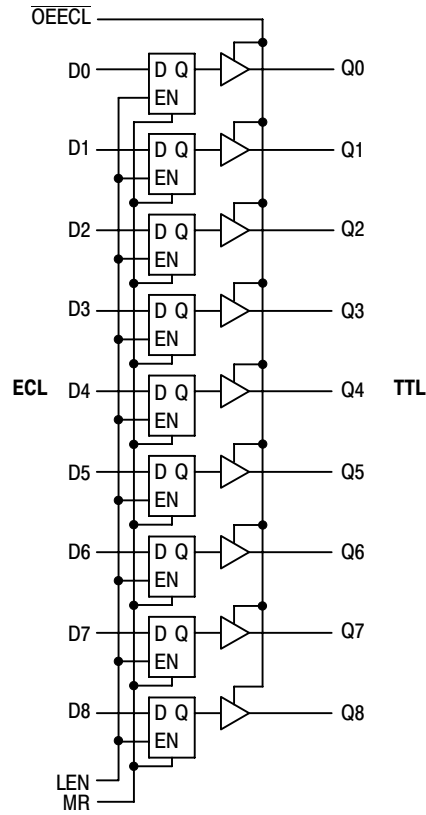


Figure 2. Logic Diagram

Table 2. TRUTH TABLE

D	LEN	MR	OE/ECL	Q
L	L	L	L	L
H	L	L	L	H
X	H	L	L	Q <sub>0</sub>
X	X	H	L	L
X	X	X	H	Z

## MC10H603, MC100H603

**10H ECL DC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -5.2\text{ V} \pm 5\%$

Symbol	Parameter	0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
$I_{EE}$	Power Supply Current		-64		-64		-64	mA
$I_{INH}$ $I_{INL}$	Input HIGH Current Input LOW Current	0.5	255	0.5	175	0.5	175	$\mu\text{A}$ $\mu\text{A}$
$V_{IH}$ $V_{IL}$	Input HIGH Voltage Input LOW Voltage	-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1060 -1950	-720 -1445	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**100H ECL DC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -4.2\text{ V to } -5.5\text{ V}$

Symbol	Parameter	0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
$I_{EE}$	Power Supply Current		-63		-64		-68	mA
$I_{INH}$ $I_{INL}$	Input HIGH Current Input LOW Current	0.5	255	0.5	175	0.5	175	$\mu\text{A}$ $\mu\text{A}$
$V_{IH}$ $V_{IL}$	Input HIGH Voltage Input LOW Voltage	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**TTL DC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -5.2\text{ V} \pm 5\%$  (10H);  $V_{EE} = -4.2\text{ V to } -5.5\text{ V}$  (100H)

Symbol	Parameter	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
$I_{CCH}$	Power Supply Current			110		110		110	mA
$I_{CCL}$				110		110		110	
$I_{CCZ}$				110		110		110	
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0\text{ V}$	-100	-225	-100	-225	-100	-225	mA
$I_{OZH}$ $I_{OZL}$	Output Disable Current HIGH Output Disable Current LOW	$V_{OUT} = 2.7\text{ V}$ $V_{OUT} = 0.5\text{ V}$		50 -50		50 -50		50 -50	$\mu\text{A}$
$V_{OHT}$	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$ $I_{OH} = -15\text{ mA}$	2.5 2.0		2.5 2.0		2.5 2.0		V
$V_{OLT}$	Output LOW Voltage	$I_{OL} = 48\text{ mA}$		0.55		0.55		0.55	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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**AC CHARACTERISTICS:**  $V_{CCT} = 5.0\text{ V} \pm 10\%$ ;  $V_{EE} = -5.2\text{ V} \pm 5\%$  (10H);  $V_{EE} = -4.2\text{ V}$  to  $-5.5\text{ V}$  (100H)

Symbol	Parameter	Condition	0°C		25°C		85°C		Unit	
			Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output	D	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$	3.0 6.4	6.0 12	3.0 6.4	6.0 12	3.0 6.4	6.0 12	ns ns
		LEN	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$	3.5 7.0	6.5 13	3.5 7.0	6.5 13	3.5 7.0	6.5 13	ns ns
		MR	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$	3.0 6.0	6.0 12	3.0 6.0	6.0 12	3.0 6.0	6.0 12	ns ns
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time		$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$	2.5 4.2	6.5 13	2.5 4.2	6.5 13	2.5 4.2	6.5 13	ns ns
				$t_{PZL}$ $t_{PZH}$	Output Enable Time		$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$	2.0 4.0	5.0 10	2.0 4.0
$t_s$	Setup Time	D to LEN		1.5		1.5		1.5		ns
$t_h$	Hold Time	D to LEN		0.8		0.8		0.8		ns
$t_{w(L)}$	LEN Pulse Width, LOW			2.0		2.0		2.0		ns
$t_R$ $t_F$	Output Rise/Fall Time 1.0 V – 2.0 V		$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	ns ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC10H603FN	PLCC-28	37 Units / Rail
MC10H603FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC10H603FNR2	PLCC-28	500 / Tape & Reel
MC10H603FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel
MC100H603FN	PLCC-28	37 Units / Rail
MC100H603FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC100H603FNR2	PLCC-28	500 / Tape & Reel
MC100H603FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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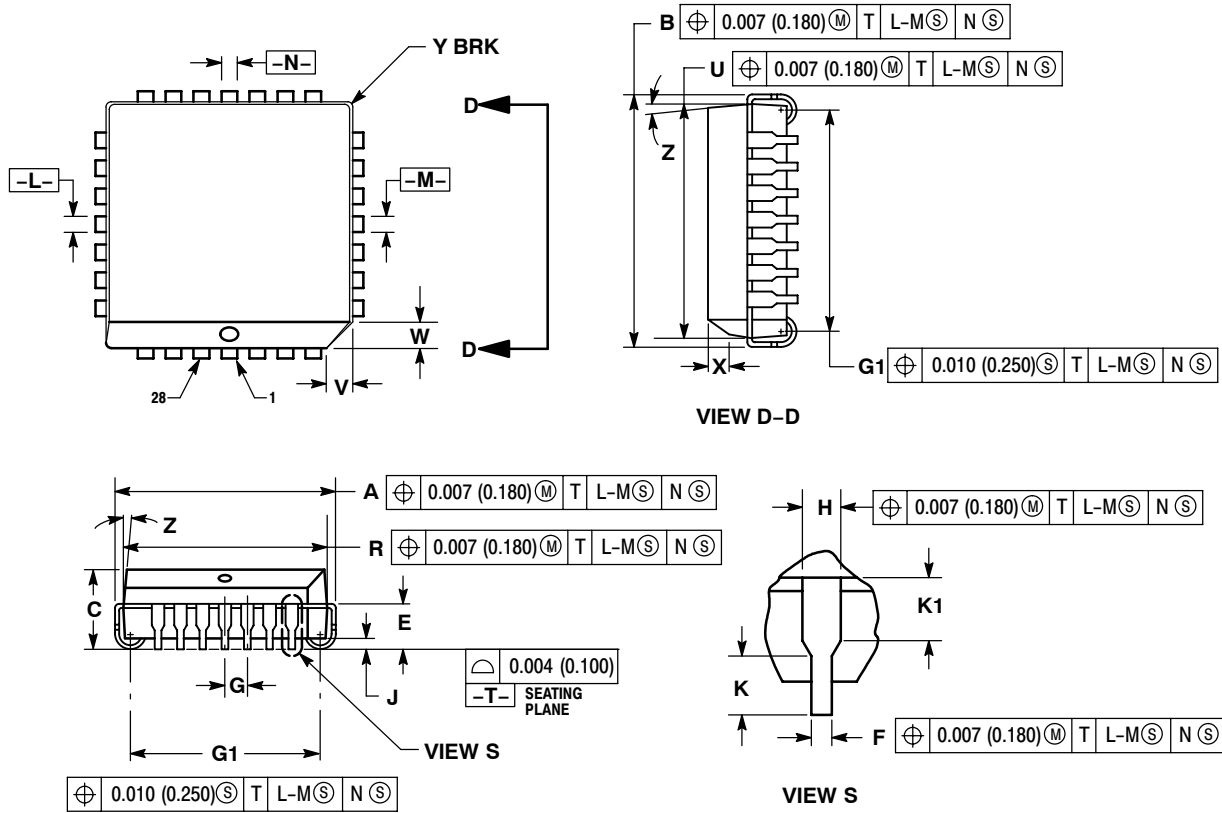
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E



### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE BOTTOM MAY BE SMALLER THAN THE PACKAGE TOP BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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