

# MC74LVXC3245

## Configurable Dual Supply Octal Transceiver

### with 3-State Outputs for 3 V Systems

The 74LVXC3245 is a 24-pin dual-supply, octal configurable voltage interface transceiver especially well suited for PCMCIA and other real time configurable I/O applications. The  $V_{CCA}$  pin accepts a 3.0 V supply level; the A port is a dedicated 3.0 V port. The  $V_{CCB}$  pin accepts a 3.0 V-to-5.0 V supply level. The B port is configured to track the  $V_{CCB}$  supply level. A 5.0 V level on the  $V_{CCB}$  pin will configure the I/O pins at a 5.0 V level and a 3.0 V  $V_{CCB}$  will configure the I/O pins at a 3.0 V level. The A port interfaces with a 3.0 V host system and the B port to the card slots. This device will allow the  $V_{CCB}$  voltage source pin and I/O pins on the B port to float when  $\overline{OE}$  is High. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation. The Transmit/Receive (T/R) input determines the direction of data flow. Transmit (active-High) enables data from the A port to B port. Receive (active-Low) enables data from the B port to the A port.

#### Features

- Bidirectional Interface Between 3.0 V and 3.0 V/5.0 V Buses
- Control Inputs Compatible with TTL Level
- Outputs Source/Sink Up to 24 mA
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Available in SOIC and TSSOP Packages
- Flexible  $V_{CCB}$  Operating Range
- Allows B Port and  $V_{CCB}$  to Float Simultaneously When  $\overline{OE}$  is High
- Functionally Compatible With the 74 Series 245
- Pb-Free Packages are Available\*

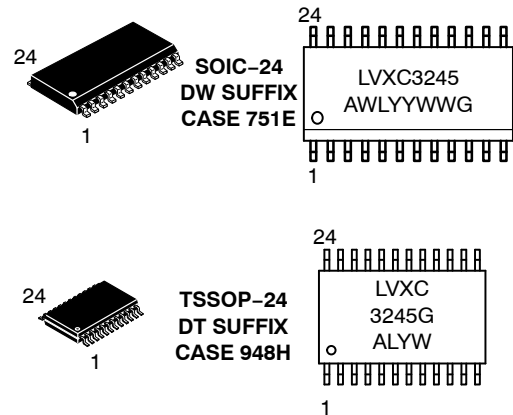
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

<http://onsemi.com>

#### MARKING DIAGRAMS



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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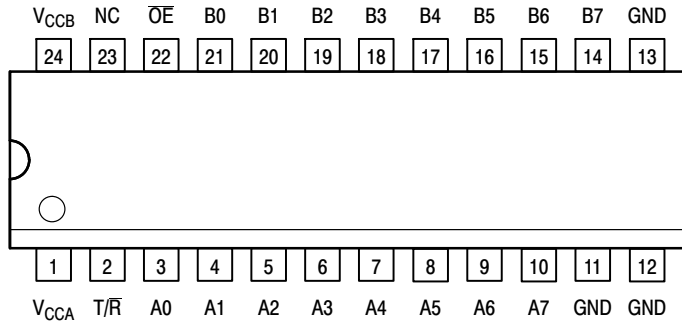


Figure 1. 24-Lead Pinout (Top View)

## PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
T/R	Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State Outputs
B0–B7	Side B 3–State Inputs or 3–State Outputs

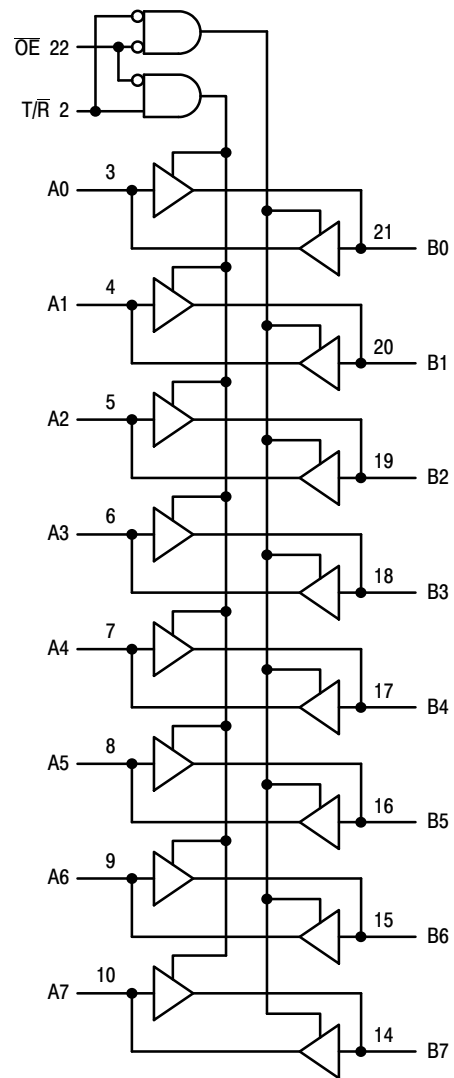


Figure 2. Logic Diagram

INPUTS		OPERATING MODE Non-Inverting
$\overline{OE}$	T/R	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; for  $I_{CC}$  reasons, Do Not Float Inputs

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit	
$V_{CCA}$ , $V_{CCB}$	DC Supply Voltage	-0.5 to +7.0		V	
$V_I$	DC Input Voltage	$\overline{OE}$ , T/ $\overline{R}$	-0.5 to $V_{CCA} + 0.5$	V	
$V_{I/O}$	DC Input/Output Voltage	An	-0.5 to $V_{CCA} + 0.5$	V	
		Bn	-0.5 to $V_{CCB} + 0.5$	V	
$I_{IK}$	DC Input Diode Current	$\overline{OE}$ , T/ $\overline{R}$	$\pm 20$	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current		$\pm 50$	$V_O < GND$ ; $V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current		$\pm 50$		mA
$I_{CC}$ , $I_{GND}$	DC Supply Current	Per Output Pin Maximum Current	$\pm 50$ $\pm 200$		mA
$T_{STG}$	Storage Temperature Range		-65 to +150		°C
	DC Latchup Source/Sink Current		$\pm 300$		mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CCA}$ , $V_{CCB}$	Supply Voltage ( $V_{CCA} \leq V_{CCB}$ )	$V_{CCA}$ 2.3 $V_{CCB}$ 3.0	3.6 5.5	V
$V_I$	Input Voltage	$\overline{OE}$ , T/ $\overline{R}$	0 $V_{CCA}$	V
$V_{I/O}$	Input/Output Voltage	An 0 Bn 0	$V_{CCA}$ $V_{CCB}$	V
$T_A$	Operating Free-Air Temperature	-40	+85	°C
$\Delta t/\Delta V$	Minimum Input Edge Rate $V_{IN}$ from 30% to 70% of $V_{CC}$ ; $V_{CC}$ at 3.0 V, 4.5 V, 5.5 V	0	8	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	$V_{CCA}$	$V_{CCB}$	$T_A = 25^\circ\text{C}$		$T_A = -40 \text{ to } +85^\circ\text{C}$		Unit
					Typ	Guaranteed Limits			
$V_{IHA}$	Minimum HIGH Level Input Voltage	An $\overline{OE}$ T/ $\overline{R}$	2.3 3.0 3.6	3.0 3.6 5.5		2.0 2.0 2.0	2.0 2.0 2.0	V	
									Bn
$V_{IHA}$	Maximum LOW Level Input Voltage	An $\overline{OE}$ T/ $\overline{R}$	2.3 3.0 3.6	3.0 3.6 5.5		0.8 0.8 0.8	0.8 0.8 0.8	V	
									Bn
$V_{OHA}$	Minimum HIGH Level Output Voltage	$I_{OUT} = -100 \mu\text{A}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	3.0 3.0 3.0 2.3 2.3	3.0 3.0 3.0 3.0 4.5	2.99 2.85 2.65 2.50 2.30	2.90 2.56 2.35 2.30 2.10	2.90 2.46 2.25 2.20 2.00	V	
									$V_{OHB}$

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to +85°C		Unit
					Typ	Guaranteed Limits			
V <sub>OLA</sub>	Maximum LOW Level Output Voltage	I <sub>OUT</sub> = 100 μA	3.0	3.0	0.002	0.10	0.10		V
		I <sub>OL</sub> = 24 mA	3.0	3.0	0.21	0.36	0.44		
		I <sub>OL</sub> = 12 mA	2.7	3.0	0.11	0.36	0.44		
		I <sub>OL</sub> = 24 mA	2.7	4.5	0.22	0.42	0.50		
V <sub>OLB</sub>		I <sub>OUT</sub> = 100 μA	3.0	3.0	0.002	0.10	0.10		V
		I <sub>OL</sub> = 24 mA	3.0	3.0	0.21	0.36	0.44		
		I <sub>OL</sub> = 24 mA	3.0	4.5	0.18	0.36	0.44		
I <sub>IN</sub>	Max Input Leakage Current	$\overline{OE}$ , T/R V <sub>I</sub> = V <sub>CCA</sub> , GND	3.6 3.6	3.6 5.5		±0.1 ±0.1	±1.0 ±1.0		μA
I <sub>OZA</sub>	Max 3-State Output Leakage	An V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> $\overline{OE}$ = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCA</sub> , GND	3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0		μA
I <sub>OZB</sub>	Max 3-State Output Leakage	Bn V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> $\overline{OE}$ = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCB</sub> , GND	3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0		μA
ΔI <sub>CC</sub>	Maximum I <sub>CC</sub> /Input	Bn V <sub>I</sub> = V <sub>CCB</sub> -2.1 V	3.6	5.5	1.0	1.35	1.5		mA
		All In-puts V <sub>I</sub> = V <sub>CC</sub> -0.6 V	3.6	3.6		0.35	0.5		mA
I <sub>CCA1</sub>	Quiescent V <sub>CCA</sub> Supply Current as B Port Floats	An = V <sub>CCA</sub> or GND Bn = Open, $\overline{OE}$ = V <sub>CCA</sub> , T/R = V <sub>CCA</sub> , V <sub>CCB</sub> = Open	3.6	Open		5	50		μA
I <sub>CCA2</sub>	Quiescent V <sub>CCA</sub> Supply Current	An = V <sub>CCA</sub> or GND Bn = V <sub>CCB</sub> or GND, $\overline{OE}$ = GND, T/R = GND	3.6 3.6	3.6 5.5		5 5	50 50		μA
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current	An = V <sub>CCA</sub> or GND Bn = V <sub>CCB</sub> or GND, $\overline{OE}$ = GND, T/R = V <sub>CCA</sub>	3.6 3.6	3.6 5.5		5 8	50 80		μA
V <sub>OLPA</sub>	Quiet Output Max Dynamic V <sub>OL</sub>	Notes 1, 2	3.3 3.3	3.3 5.0		0.8 0.8			V
V <sub>OLPB</sub>			3.3 3.3	3.3 5.0		0.8 1.5			V
V <sub>OLVA</sub>	Quiet Output Min Dynamic V <sub>OL</sub>	Notes 1, 2	3.3 3.3	3.3 5.0		-0.8 -0.8			V
V <sub>OLVB</sub>			3.3 3.3	3.3 5.0		-0.8 -1.2			V
V <sub>IHDA</sub>	Min HIGH Level Dynamic Input Voltage	Notes 1, 3	3.3 3.3	3.3 5.0		2.0 2.0			V
			3.3 3.3	3.3 5.0		2.0 3.5			V
V <sub>ILDA</sub>	Max LOW Level Dynamic Input Voltage	Notes 1, 3	3.3 3.3	3.3 5.0		0.8 0.8			V
			3.3 3.3	3.3 5.0		0.8 1.5			V

1. Worst case package.
2. Max number of outputs defined as (n). Data inputs are driven 0 V to V<sub>CC</sub> level; one output at GND.
3. Max number of data inputs (n) switching. (n-1) inputs switching 0 V to V<sub>CC</sub> level. Input under test switching: V<sub>CC</sub> level to threshold (V<sub>IHD</sub>), 0 V to threshold (V<sub>ILD</sub>), f = 1 MHz.

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## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	$T_A = -40 \text{ to } +85^\circ\text{C}; C_L = 50 \text{ pF}$						Unit
		$V_{CCA} = 2.7\text{--}3.6 \text{ V}$ $V_{CCB} = 4.5\text{--}5.5 \text{ V}$			$V_{CCA} = 2.7\text{--}3.6 \text{ V}$ $V_{CCB} = 3.0\text{--}3.6 \text{ V}$			
		Min	Typ (Note 4)	Max	Min	Typ (Note 5)	Max	
$t_{PHL}$ $t_{PLH}$	Propagation Delay A to B	1.0 1.0	4.8 3.9	8.5 7.0	1.0 1.0	5.5 5.2	9.0 8.5	ns
$t_{PHL}$ $t_{PLH}$	Propagation Delay B to A	1.0 1.0	3.8 4.3	7.0 8.0	1.0 1.0	4.4 5.1	7.5 8.0	ns
$t_{PZL}$ $t_{PZH}$	Output Enable Time $\overline{OE}$ to B	1.0 1.0	4.7 4.8	8.5 9.0	1.0 1.0	6.0 6.1	9.5 10.0	ns
$t_{PZL}$ $t_{PZH}$	Output Enable Time $\overline{OE}$ to A	1.0 1.0	5.9 5.4	10.0 9.5	1.0 1.0	6.4 5.8	10.5 9.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$ to B	1.0 1.0	4.0 3.8	8.5 8.0	1.0 1.0	6.3 4.5	10.0 8.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$ to A	1.0 1.0	4.6 3.1	10.0 7.0	1.0 1.0	5.2 3.4	10.0 7.0	ns
$t_{OSHL}$ $t_{OSLH}$	Output to Output Skew, Data to Output (Note 6)		1.0	1.5		1.0	1.5	ns

4. Typical values at  $V_{CCA} = 3.3 \text{ V}$ ,  $V_{CCB} = 5.0 \text{ V}$  at  $25^\circ\text{C}$ .

5. Typical values at  $V_{CCA} = 3.3 \text{ V}$ ,  $V_{CCB} = 3.3 \text{ V}$  at  $25^\circ\text{C}$ .

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CCA} = 3.3 \text{ V}; V_{CCB} = 5.0 \text{ V}$	4.5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CCA} = 3.3 \text{ V}; V_{CCB} = 5.0 \text{ V}$	10	pF
$C_{PD}$	Power Dissipation Capacitance (Measured at 10 MHz)	A→B B→A $V_{CCB} = 5.0 \text{ V}$ $V_{CCA} = 3.3 \text{ V}$	50 40	pF

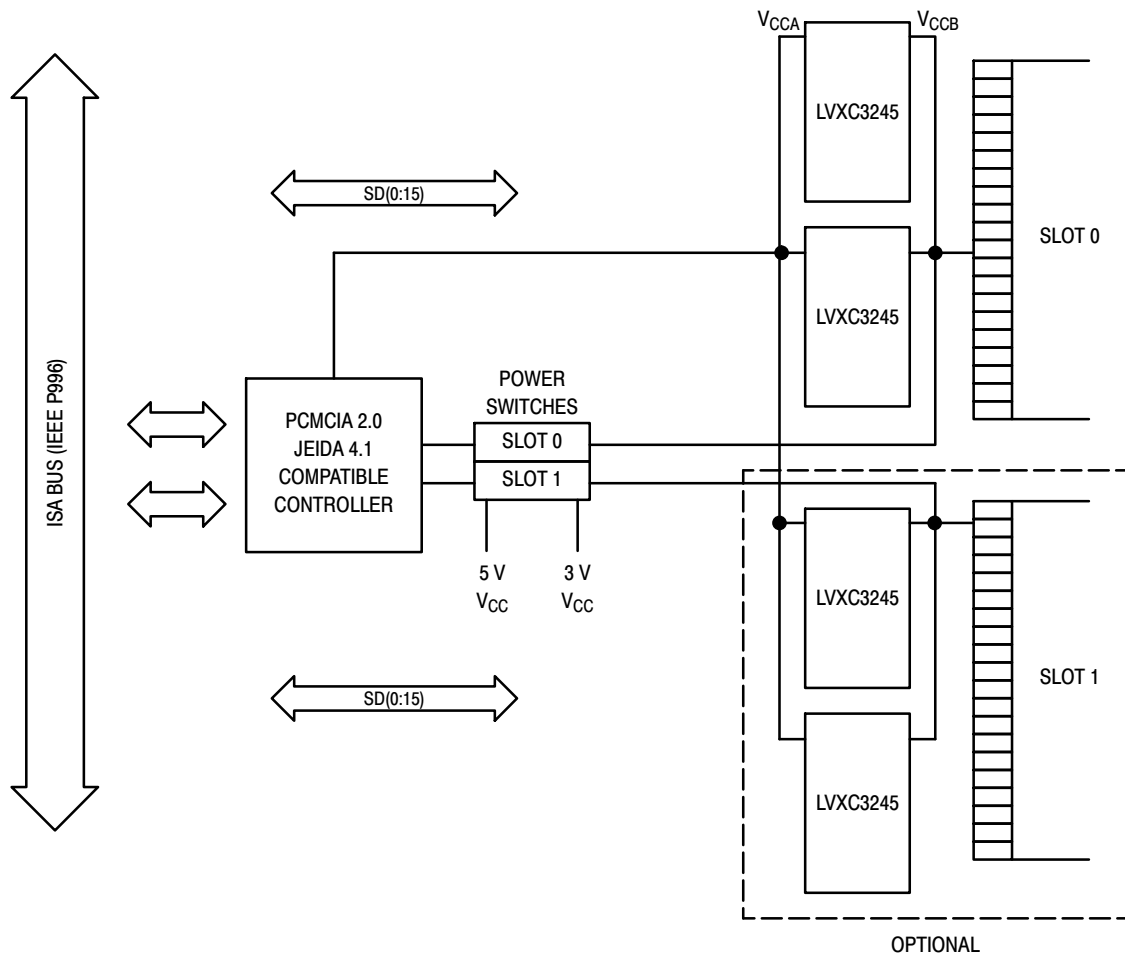
## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74LVXC3245DWR2	SOIC-24	1000 Tape & Reel
MC74LVXC3245DWR2G	SOIC-24 (Pb-Free)	1000 Tape & Reel
MC74LVXC3245DT	TSSOP-24*	62 Units / Rail
MC74LVXC3245DTG	TSSOP-24* (Pb-Free)	62 Units / Rail
MC74LVXC3245DTR2	TSSOP-24*	2500 Tape & Reel
MC74LVXC3245DTR2G	TSSOP-24* (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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**Figure 3. Block Diagram**

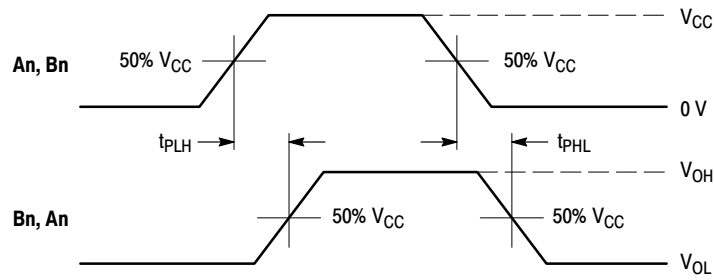
### Configurable I/O Application for PCMCIA Cards

The 74LVXC3245 is a dual-supply device well suited for PCMCIA configurable I/O applications. The LVXC3245 consumes less than 1mW of quiescent power in all modes of operation, making it ideal for low power notebook designs. The LVXC3245 meets all PCMCIA I/O voltage requirements at 5.0 V and 3.3 V operation. By tying the V<sub>CCB</sub> pin to the card voltage supply, the PCMCIA card will always have

rail-to-rail output swings, maximizing the reliability of the interface.

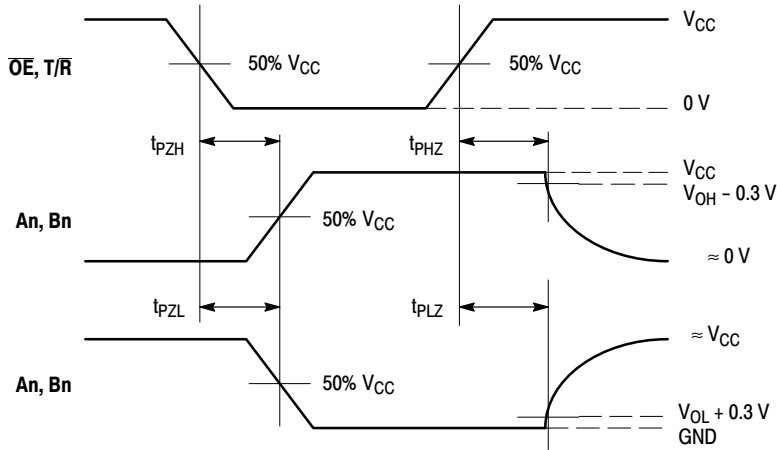
The V<sub>CCA</sub> pin must always be tied to a 3.3 V power supply. This voltage connection provides internal references needed to account for variations in V<sub>CCB</sub>. When connected as in the figure above, the LVXC3245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

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**WAVEFORM 1 - PROPAGATION DELAYS**

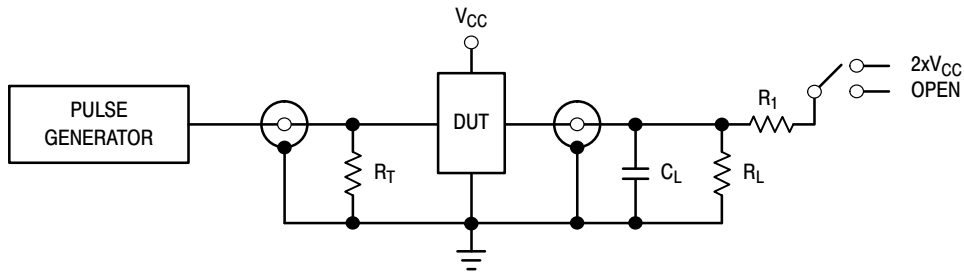
$t_R = t_F = 2.5 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$



**WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES**

$t_R = t_F = 2.5 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

**Figure 4. AC Waveforms**



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$ , $t_{PZH}$ , $t_{PHZ}$	Open
$t_{PZL}$ , $t_{PLZ}$	$2xV_{CC}$

$C_L = 50 \text{ pF}$  or equivalent (Includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$  or equivalent

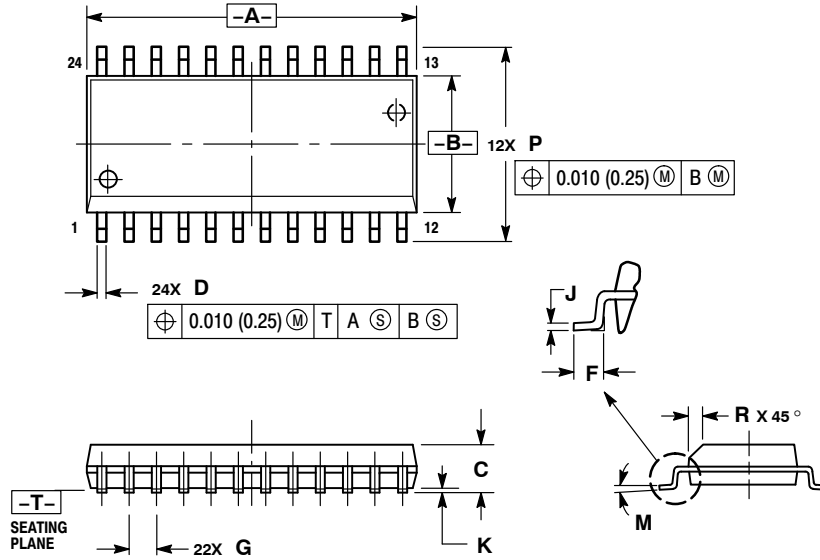
$R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

**Figure 5. Test Circuit**

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## PACKAGE DIMENSIONS

SOIC-24  
DW SUFFIX  
CASE 751E-04  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

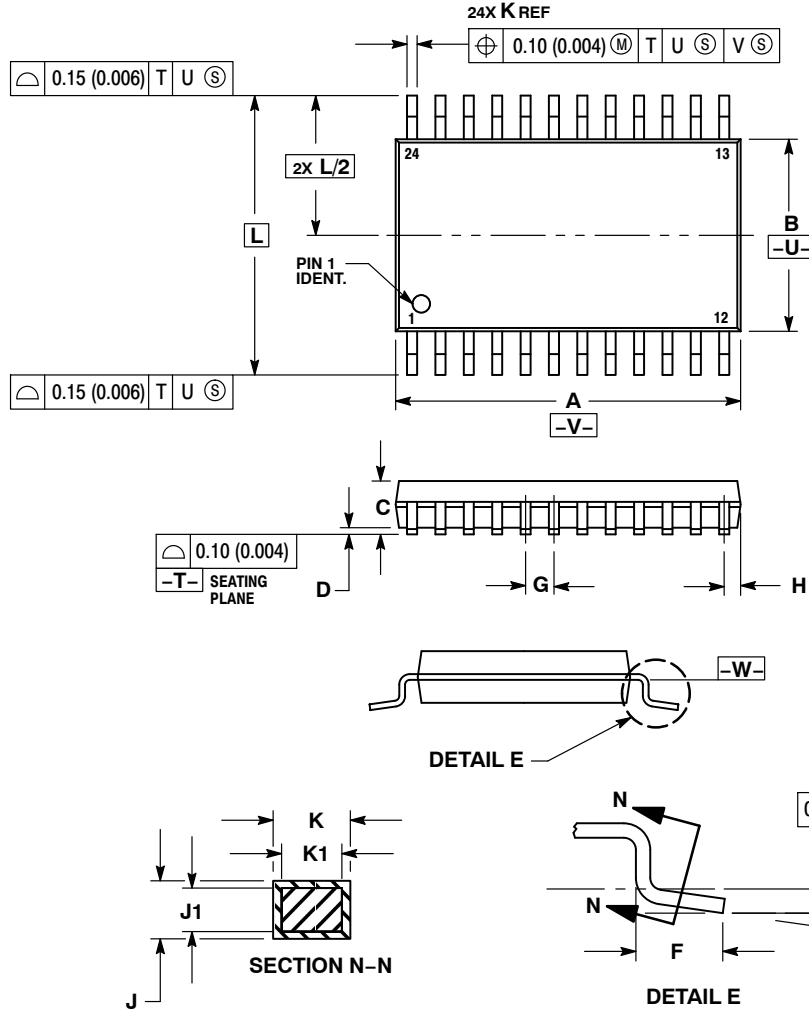
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029



# MC74LVXC3245

## PACKAGE DIMENSIONS

TSSOP-24  
DT SUFFIX  
CASE 948H-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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