

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LVXC3245FS

Dual Supply Octal Configurable Voltage Interface Bus Transceiver

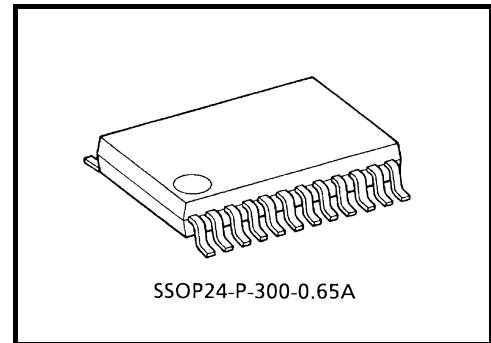
The TC74LVXC3245FS is a dual supply, advanced high-speed CMOS octal configurable voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 3.3 V bus and a 3.3V to 5 V bus in mixed 3.3 V/5 V supply systems' it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses.

The direction of data transmission is determined by the level of the DIR input. The enable input (\bar{G}) can be used to disable the device so that the busses are effectively isolated. The A-port interfaces with the 3.3-V bus, the B-port with the 3.3V to 5V bus. This device will allow the V_{CCB} voltage source pin and I/O pins on the B port to float when \bar{G} is "H".

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



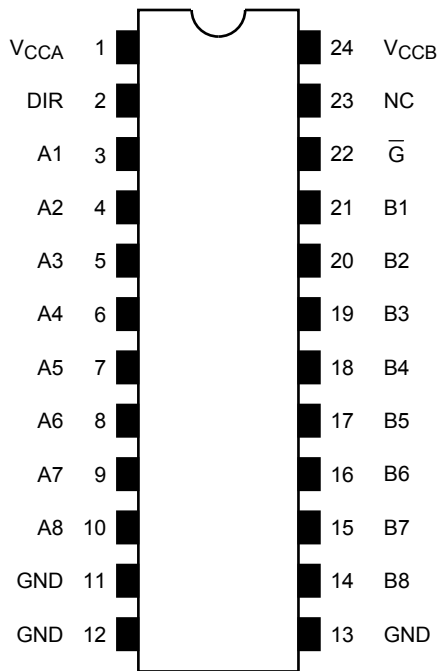
Weight: 0.14 g (typ.)

Features

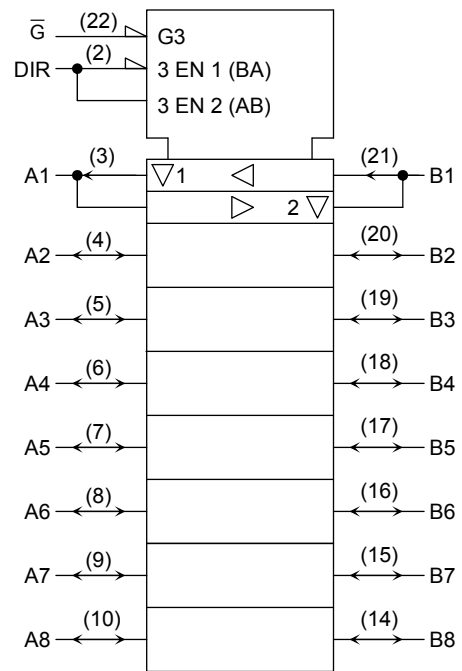
- Bi-directional interface between 3 V and 5 V buses
- High-speed: $t_{pd} = 8.5$ ns (max)
($V_{CCA} = 3.3$ V, $V_{CCB} = 5.0$ V)
- Low power dissipation: $I_{CC} = 8$ μ A (max) ($T_a = 25^\circ$ C)
- Symmetrical output impedance: $I_{OUTA} = \pm 24$ mA (min)
 $I_{OUTB} = \pm 24$ mA (min)
($V_{CCA} = V_{CCB} = 3.0$ V)
- Low noise: $V_{OLP} = 1.5$ V (max)
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when \bar{G} is "H"
- Package: SSOP (shrink small outline package)

Note 1: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pin must have their input levels fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)



IEC Logic Symbol



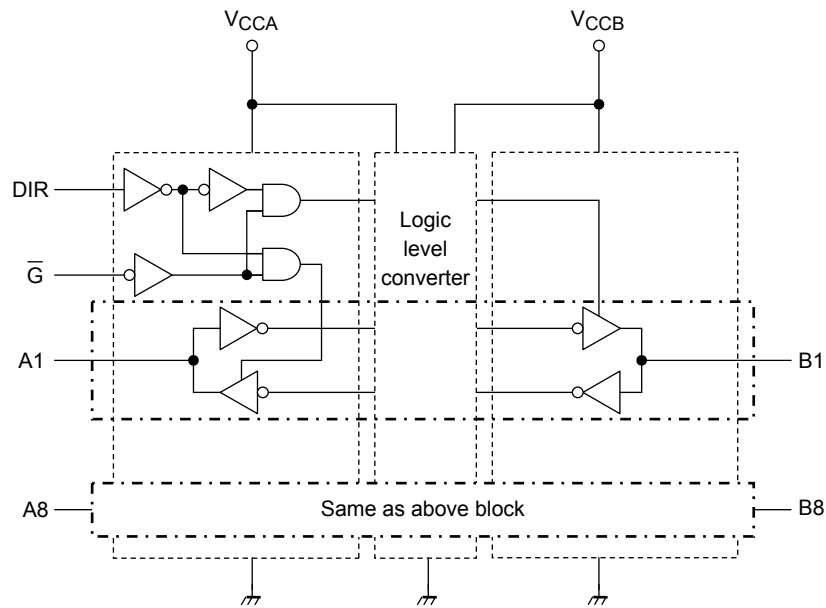
Truth Table

Inputs		Outputs	Function	
\bar{G}	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	High impedance	

X: Don't care

Z: High impedance

Block Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range (Note 2)	V_{CCA}	-0.5 to 7.0	V
	V_{CCB}	-0.5 to 7.0	
DC input voltage (DIR, \bar{G})	V_{IN}	-0.5 to $V_{CCA} + 0.5$	V
DC bus I/O voltage	V_{IOA}	-0.5 to $V_{CCA} + 0.5$	V
	V_{IOB}	-0.5 to $V_{CCB} + 0.5$	
Input diode current	I_{IK}	± 20	mA
Output diode current	$I_{I/OK}$	± 50	mA
DC output current	I_{OUTA}	± 50	mA
	I_{OUTB}	± 50	
DC V_{CC} /ground current	I_{CCA}	± 200	mA
	I_{CCB}	± 200	
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: Don't supply a voltage to V_{CCB} terminal when V_{CCA} is in the OFF state.

Operating Range (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CCA}	2.7 to 3.6	V
	V_{CCB}	3.0 to 5.5	
Input voltage (DIR, \bar{G})	V_{IN}	0 to V_{CCA}	V
Bus I/O voltage	$V_{I/OA}$	0 to V_{CCA}	V
	$V_{I/OB}$	0 to V_{CCB}	
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 8 ($V_{CCA} = 2.7$ to 3.6 V)	ns/V
		0 to 8 ($V_{CCB} = 3.0$ to 5.5 V)	

Note: The operating range is required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either VCC or GND. Please connect both bus inputs and the bus outputs with VCC or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Electrical Characteristics

DC Characteristics

Characteristics		Sym- bol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit		
					V _{CCA} (V)	V _{CCB} (V)	Min	Typ.	Max		Min	Max
Input voltage (V _{CCA})	H-level	V _{IHA}	DIR, \bar{G} , An	2.7	3.0	2.0	—	—	2.0	—	V	
				3.0	3.6	2.0	—	—	2.0	—		
				3.6	5.5	2.0	—	—	2.0	—		
	L-level	V _{ILA}	DIR, \bar{G} , An	2.7	3.0	—	—	0.8	—	0.8		
				3.0	3.6	—	—	0.8	—	0.8		
				3.6	5.5	—	—	0.8	—	0.8		
Input voltage (V _{CCB})	H-level	V _{IHB}	Bn	2.7	3.0	2.0	—	—	2.0	—	V	
				3.0	3.6	2.0	—	—	2.0	—		
				3.6	5.5	3.85	—	—	3.85	—		
	L-level	V _{ILB}	Bn	2.7	3.0	—	—	0.8	—	0.8		
				3.0	3.6	—	—	0.8	—	0.8		
				3.6	5.5	—	—	1.65	—	1.65		
Output voltage (V _{CCA})	H-level	V _{OHA}	V _{INA} = V _{IHA} or V _{ILA} V _{INB} = V _{IHB} or V _{ILB}	I _{OH} = -100 μA	3.0	3.0	2.9	3.0	—	2.9	—	V
				I _{OH} = -12 mA	3.0	3.0	2.56	—	—	2.46	—	
				I _{OH} = -24 mA	3.0	3.0	2.35	—	—	2.25	—	
				I _{OH} = -12 mA	2.7	3.0	2.3	—	—	2.2	—	
				I _{OH} = -24 mA	2.7	4.5	2.1	—	—	2.0	—	
	L-level	V _{OLA}		I _{OL} = 100 μA	3.0	3.0	—	0.0	0.1	—	0.1	
				I _{OL} = 24 mA	3.0	3.0	—	—	0.36	—	0.44	
				I _{OL} = 12 mA	2.7	3.0	—	—	0.36	—	0.44	
				I _{OL} = 24 mA	2.7	4.5	—	—	0.42	—	0.5	
				I _{OL} = 12 mA	2.7	4.5	—	—	0.42	—	0.5	

DC Characteristics (continued)

Characteristics		Sym- bol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit		
					V _{CCA} (V)	V _{CCB} (V)	Min	Typ.	Max		Min	Max
Output voltage (V _{CCB})	H-level	V _{OHB}	V _{INA} = V _{IHA} or V _{ILA} V _{INB} = V _{IHB} or V _{ILB}	I _{OH} = -100 μA	3.0	3.0	2.9	3.0	—	2.9	—	V
				I _{OH} = -12 mA	3.0	3.0	2.56	—	—	2.46	—	
				I _{OH} = -24 mA	3.0	3.0	2.35	—	—	2.25	—	
				I _{OH} = -24 mA	3.0	4.5	3.86	—	—	3.76	—	
	L-level	V _{OLB}		I _{OL} = 100 μA	3.0	3.0	—	0.0	0.1	—	0.1	
				I _{OL} = 24 mA	3.0	3.0	—	—	0.36	—	0.44	
				I _{OL} = 24 mA	3.0	4.5	—	—	0.36	—	0.44	
3-state output Off-state current	I _{OZA}	V _{INA} = V _{IHA} or V _{ILA} V _{INB} = V _{IHB} or V _{ILB}	3.6	3.6	—	—	±0.5	—	±5.0	μA		
			3.6	5.5	—	—	±0.5	—	±5.0			
	I _{OZB}	V _{I/OA} = V _{CCA} or GND V _{I/OB} = V _{CCB} or GND	3.6	3.6	—	—	±0.5	—	±5.0			
			3.6	5.5	—	—	±0.5	—	±5.0			
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{G}) = V _{CCA} or GND	3.6	3.6	—	—	±0.1	—	±1.0	μA		
			3.6	5.5	—	—	±0.1	—	±1.0			
Quiescent supply current	I _{CCT}	PER INPUT: V _{INA} = V _{CCA} - 0.6 V V _{INA} = V _{CCB} - 0.6 V	3.6	3.6	—	—	0.35	—	0.5	mA		
	I _{CCA1}	A _n = V _{CCA} or GND B _n = Open, \overline{G} = V _{CCA} DIR = V _{CCA} , V _{CCB} = Open	3.6	Open	—	—	5	—	50	μA		
	I _{CCA2}	V _{INA} = V _{IHA} or V _{ILA} V _{INB} = V _{IHB} or V _{ILB}	3.6	3.6	—	—	5	—	50			
			3.6	5.5	—	—	5	—	50			
	I _{CCB}	V _{INA} = V _{IHA} or V _{ILA} V _{INB} = V _{IHB} or V _{ILB}	3.6	3.6	—	—	5	—	50			
			3.6	5.5	—	—	8	—	80			

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit			
			VCCA(V)	VCCB(V)	Min	Typ.	Max		Min	Max	
Propagation delay time (An → Bn)	t_{pLH}	Input: An Output: Bn (DIR = "H")	2.7 ~ 3.6	5.0 ± 0.5	—	5.7	8.0	1.0	8.5	ns	
	t_{pHL}			3.3 ± 0.3	—	6.2	8.5	1.0	9.0		
3-state output enable time (\bar{G} → Bn)	t_{pZL}			5.0 ± 0.5	—	6.5	9.5	1.0	10.0	ns	
	t_{pZH}			3.3 ± 0.3	—	7.4	10.5	1.0	11.5		
3-state output disable time (\bar{G} → Bn)	t_{pLZ}			5.0 ± 0.5	—	7.3	9.5	1.0	10.0	ns	
	t_{pHZ}			3.3 ± 0.3	—	6.6	9.5	1.0	10.0		
Propagation delay time (Bn → An)	t_{pLH}	Input: Bn Output: An (DIR = "L")	2.7 ~ 3.6	5.0 ± 0.5	—	4.6	7.5	1.0	8.0	ns	
	t_{pHL}			3.3 ± 0.3	—	5.2	7.5	1.0	8.0		
3-state output enable time (\bar{G} → An)	t_{pZL}			5.0 ± 0.5	—	7.0	10.5	1.0	11.5	ns	
	t_{pZH}			3.3 ± 0.3	—	7.0	10.5	1.0	11.5		
3-state output disable time (\bar{G} → An)	t_{pLZ}			5.0 ± 0.5	—	6.1	9.5	1.0	10.0	ns	
	t_{pHZ}			3.3 ± 0.3	—	6.0	9.5	1.0	10.0		
Output to output skew	t_{osLH}	(Note 1)	2.7 ~ 3.6	5.0 ± 0.5	—	—	1.5	—	1.5	ns	
	t_{osHL}			3.3 ± 0.3	—	—	1.5	—	1.5		
Input capacitance	C_{iNA}	DIR, \bar{G}	3.3 ± 0.3	5.0 ± 0.5	—	5	10	—	10	pF	
Bus input capacitance	$C_{i/O}$	An, Bn			—	8	—	—	—	—	pF
Power dissipation capacitance (Note 2)	C_{pDA}	A → B (DIR = "H")			—	4	—	—	—	—	pF
		B → A (DIR = "L")			—	38	—	—	—	—	
	C_{pDB}	A → B (DIR = "H")	—	88	—	—	—	—			
		B → A (DIR = "L")	—	7	—	—	—	—			

Note 1: Parameter guaranteed by design.
 $(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

Note 2: C_{pD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

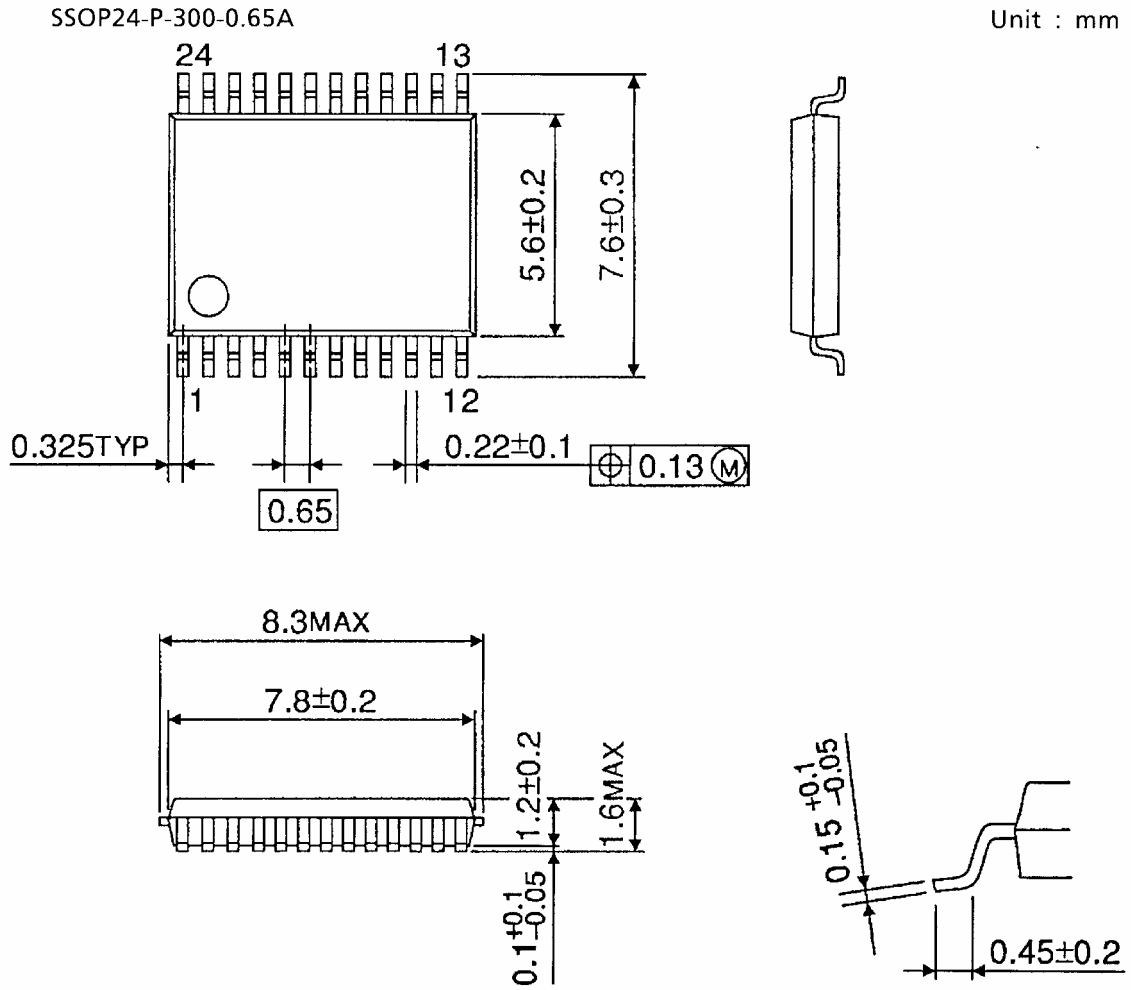
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{pD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

Noise Characteristics (Ta = 25°C, input: tr = tf = 3 ns, CL = 50 pF, RL = 500 Ω)

Characteristics	Symbol	Symbol	Test Condition	VCC (V)		Typ.	Limit	Unit
				VCCA (V)	VCCB (V)			
Quiet output maximum dynamic	VOL (A)	VOLPA	Input: Bn Output: An (DIR = "L")	3.3	3.3	—	0.9	V
				3.3	5.0	—	0.9	
Quiet output minimum dynamic	VOL (A)	VOLVA	(DIR = "L")	3.3	3.3	—	-0.9	
				3.3	5.0	—	-0.9	
Quiet output maximum dynamic	VOL (B)	VOLPB	Input: An Output: Bn (DIR = "H")	3.3	3.3	—	0.8	
				3.3	5.0	—	1.5	
Quiet output minimum dynamic	VOL (B)	VOLVB	(DIR = "H")	3.3	3.3	—	-0.8	
				3.3	5.0	—	-1.2	
Minimum high level dynamic input voltage	VIH (A)	VIHDA	Input: An	3.3	3.3	—	2.0	V
				3.3	5.0	—	2.0	
Maximum low level dynamic input Voltage	VIL (A)	VILDA	Input: An	3.3	3.3	—	0.8	V
				3.3	5.0	—	0.8	
Minimum high level dynamic input voltage	VIH (B)	VIHDB	Input: Bn	3.3	3.3	2.0	—	V
				3.3	5.0	3.5	—	
Maximum low level dynamic input voltage	VIL (B)	VILDB	Input: Bn	3.3	3.3	0.8	—	V
				3.3	5.0	1.5	—	

Package Dimensions



Weight: 0.14 g (typ.)

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20070701-EN

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