

# MC100EPT25

## -3.3V / -5V Differential ECL to +3.3V LVTTTL Translator

### Description

The MC100EPT25 is a Differential ECL to LVTTTL translator. This device requires +3.3 V, -3.3 V to -5.2 V, and ground. The small outline 8-lead package and the single gate of the EPT25 make it ideal for applications which require the translation of a clock or data signal.

The  $V_{BB}$  output allows the EPT25 to also be used in a single-ended input mode. In this mode the  $V_{BB}$  output is tied to the D input for a inverting buffer or the  $\bar{D}$  input for a non-inverting buffer. If used, the  $V_{BB}$  pin should be bypassed to ground with at least a 0.01  $\mu\text{F}$  capacitor.

### Features

- 1.1 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- Operating Range:  $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ ;  
 $V_{EE} = -5.5 \text{ V to } -3.0 \text{ V}$ ;  $GND = 0 \text{ V}$
- 24 mA TTL Outputs
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- $V_{BB}$  Output
- Open Input Default State
- Safety Clamp on Inputs
- Pb-Free Packages are Available



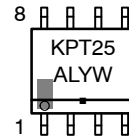
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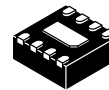
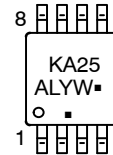
### MARKING DIAGRAMS\*



SOIC-8  
D SUFFIX  
CASE 751



TSSOP-8  
DT SUFFIX  
CASE 948R



DFN8  
MN SUFFIX  
CASE 506AA



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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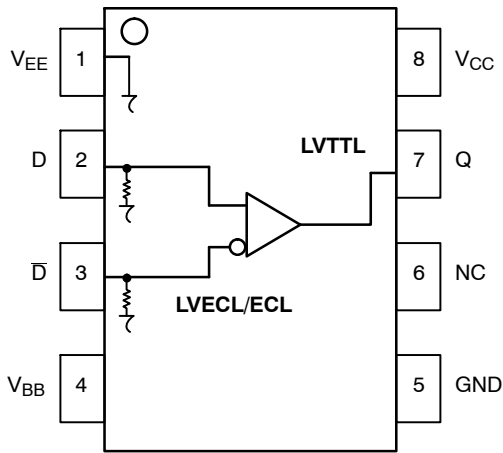


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q	LVTTTL Output
D*, $\bar{D}^*$	Differential ECL Input Pair
V <sub>CC</sub>	Positive Supply
V <sub>BB</sub>	Output Reference Voltage
GND	Ground
V <sub>EE</sub>	Negative Supply
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

\* Pins will default LOW when left open.

Table 2. ATTRIBUTES

Characteristics	Value	
Internal Input Pulldown Resistor	75 k $\Omega$	
Internal Input Pullup Resistor	N/A	
ESD Protection	Human Body Model	> 4 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	SOIC-8	Level 1
	TSSOP-8	Level 1
	DFN8	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL-94 V-0 @ 0.125 in
Transistor Count	111 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

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**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V	V <sub>EE</sub> = -5.0 V	3.8	V
V <sub>EE</sub>	Negative Power Supply	GND = 0 V	V <sub>CC</sub> = +3.3 V	-6	V
V <sub>IN</sub>	Input Voltage	GND = 0 V		0 to V <sub>EE</sub>	V
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	8 SOIC	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	8 TSSOP	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T <sub>sol</sub>	Wave Solder Pb Pb-Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

**Table 4. NECL DC CHARACTERISTICS** V<sub>CC</sub> = 3.3 V; V<sub>EE</sub> = -5.5 V to -3.0 V; GND = 0.0 V (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current	8.0	16	25	8.0	16	25	8.0	16	25	mA
V <sub>IH</sub>	Input HIGH Voltage Single-Ended	-1225		-880	-1225		-880	-1225		-880	mV
V <sub>IL</sub>	Input LOW Voltage Single-Ended	-1945		-1625	-1945		-1625	-1945		-1625	mV
V <sub>BB</sub>	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Note 4)	V <sub>EE</sub> + 2.0		0.0	V <sub>EE</sub> + 2.0		0.0	V <sub>EE</sub> + 2.0		0.0	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input parameters vary 1:1 with GND.

4. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

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**Table 5. TTL OUTPUT DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = -5.5\text{ V to }-3.0\text{ V}$ ;  $GND = 0.0\text{ V}$ ;  $T_A = -40^\circ\text{C to }85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$	2.2			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24\text{ mA}$			0.5	V
$I_{CCH}$	Power Supply Current		6	10	14	mA
$I_{CCL}$	Power Supply Current		7	12	17	mA

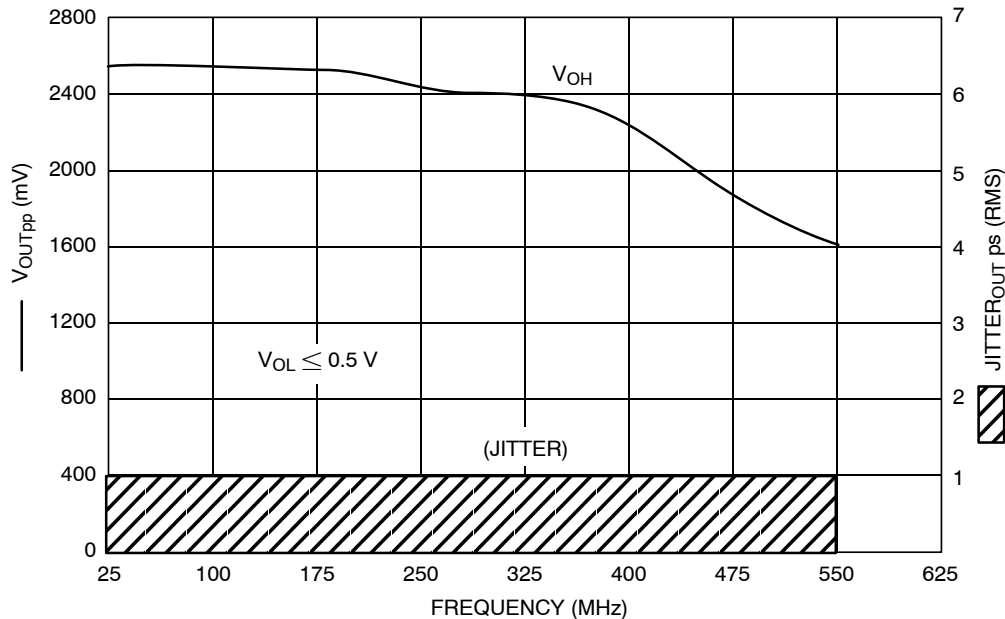
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{EE} = -5.5\text{ V to }-3.0\text{ V}$ ;  $GND = 0.0\text{ V}$  (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 2 $F_{max}/JITTER$ )	275			275			275			MHz
$t_{PLH}, t_{PHL}$	Propagation Delay to Output Differential (Cross-Point to 1.5 V)	500	950	1300	800	950	1600	800	960	1600	ps
$t_{SKPP}$	Device-to-Device Skew (Note 6)			500			500			500	ps
$t_{JITTER}$	Random Clock Jitter (RMS) (See Figure 2 $F_{max}/JITTER$ )		0.2	< 1		0.2	< 1		0.2	< 1	ps
$V_{PP}$	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ $t_f$	Output Rise/Fall Times (0.8 V – 2.0 V)	300 900	474 1160	600 1400	300 900	459 1100	600 1400	300 900	457 1100	600 1400	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measured with a 750 mV 50% duty-cycle clock source.  $R_L = 500\ \Omega$  to GND and  $C_L = 20\text{ pF}$  to GND. Refer to Figure 3.
6. Skews are measured between outputs under identical conditions.



**Figure 2.  $F_{max}/Jitter$**

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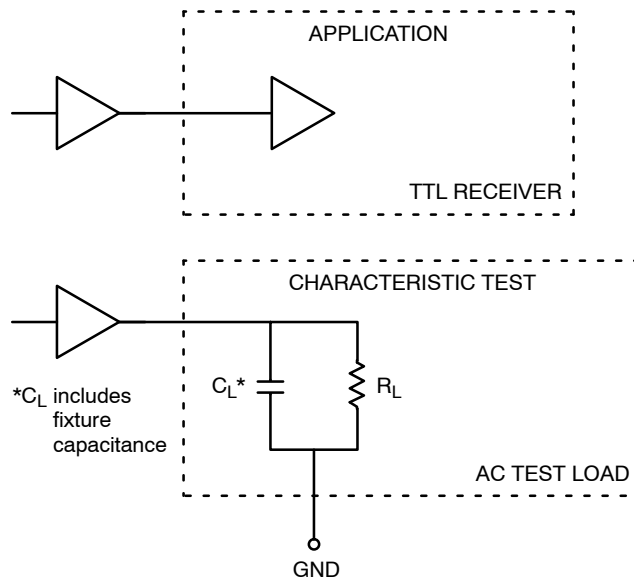


Figure 3. TTL Output Loading Used for Device Evaluation

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100EPT25D	SOIC-8	98 Units / Rail
MC100EPT25DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100EPT25DR2	SOIC-8	2500 / Tape & Reel
MC100EPT25DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100EPT25DT	TSSOP-8	100 Units / Rail
MC100EPT25DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100EPT25DTR2	TSSOP-8	2500 / Tape & Reel
MC100EPT25DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100EPT25MNR4	DFN8	1000 / Tape & Reel
MC100EPT25MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

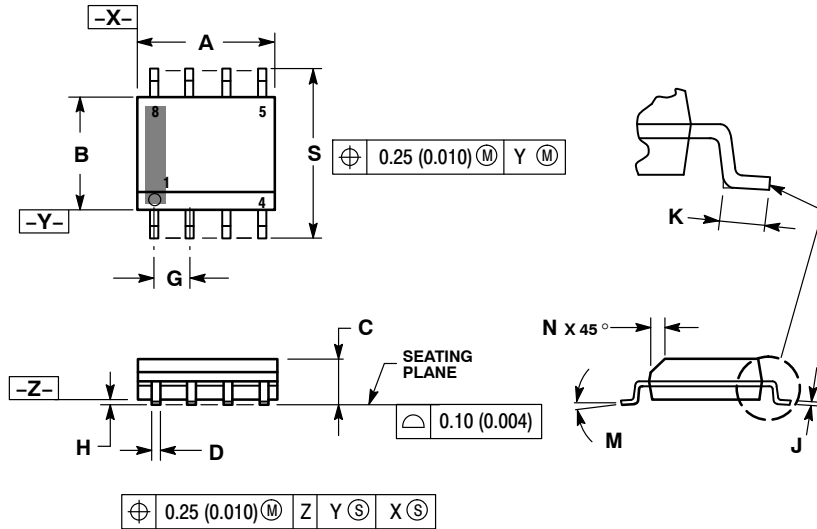
## Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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## PACKAGE DIMENSIONS

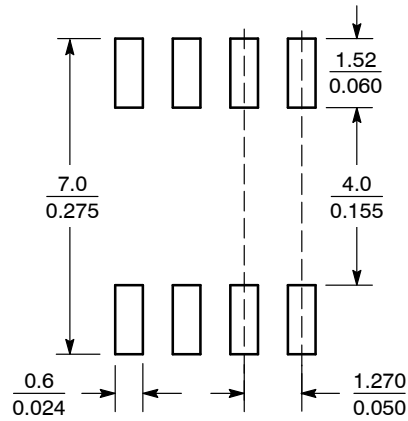
SOIC-8 NB  
CASE 751-07  
ISSUE AJ



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



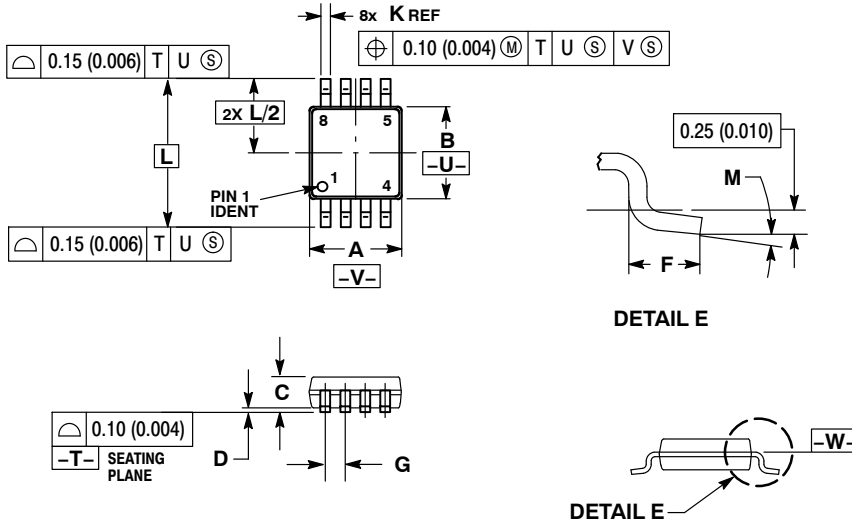
SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

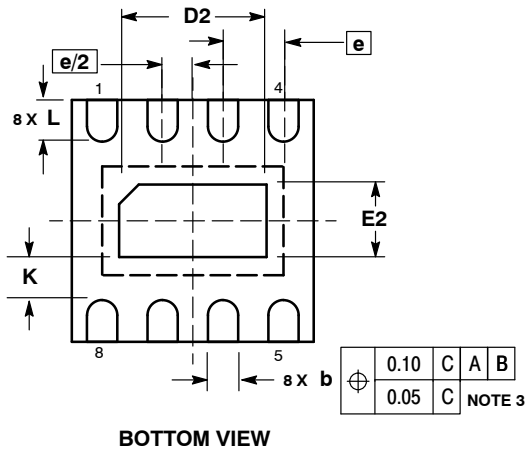
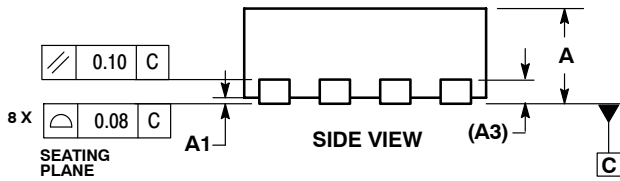
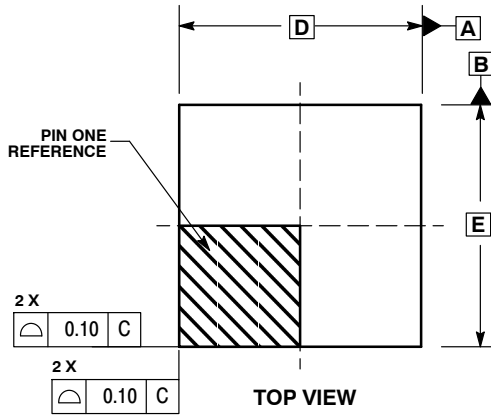
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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## PACKAGE DIMENSIONS

DFN8  
CASE 506AA-01  
ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.20	---
L	0.25	0.35

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