

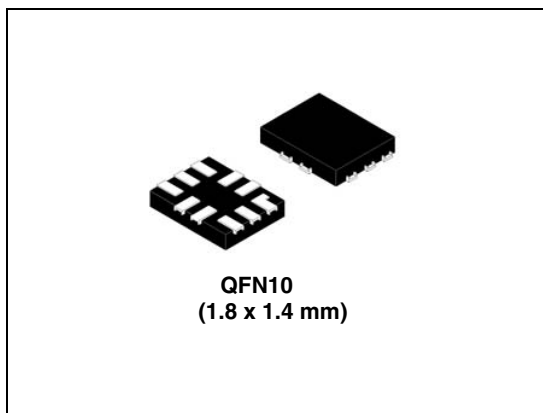
## 2-bit dual supply level translator without direction control pin

### Features

- 42 MHz: 84 Mbps (max) data rate at  $V_L = 1.8\text{ V}$ ,  $V_{CC} = 3.3\text{ V}$
- Bidirectional level translation without direction control pin
- Wide voltage range ( $V_{CC} \geq V_L$ ):
  - $V_L$  ranges from 1.65 to 3.6 V
  - $V_{CC}$  ranges from 1.65 to 5.5 V
- Power down mode feature - when  $V_{CC}$  supply is off, all I/Os are in high impedance
- Totem-pole driving
- 5.5 V tolerant enable pin
- ESD performance on all pins :  $\pm 2\text{ kv HBM}$
- Small package and footprint: QFN10 (1.8 x 1.4 mm)

### Applications

- Low voltage system level translation
- Mobile phones and other mobile devices



### Description

The ST2129 is a 2-bit dual supply level translator which provides the level shifting capability to allow data transfer in a multi-voltage system. Externally applied voltages,  $V_{CC}$  and  $V_L$ , set the logic levels on either side of the device. Its architecture allows bidirectional level translation without a control pin.

The ST2129 accepts  $V_L$  from 1.65 to 3.6 V and  $V_{CC}$  from 1.65 to 5.5 V, making it ideal for data transfer between low-voltage ASICs/PLD and higher voltage systems. This device has a tri-state output mode which can be used to disable all I/Os.

The ST2129 supports power-down mode when  $V_{CC}$  is grounded/floating or when the device is disabled via the OE pin.

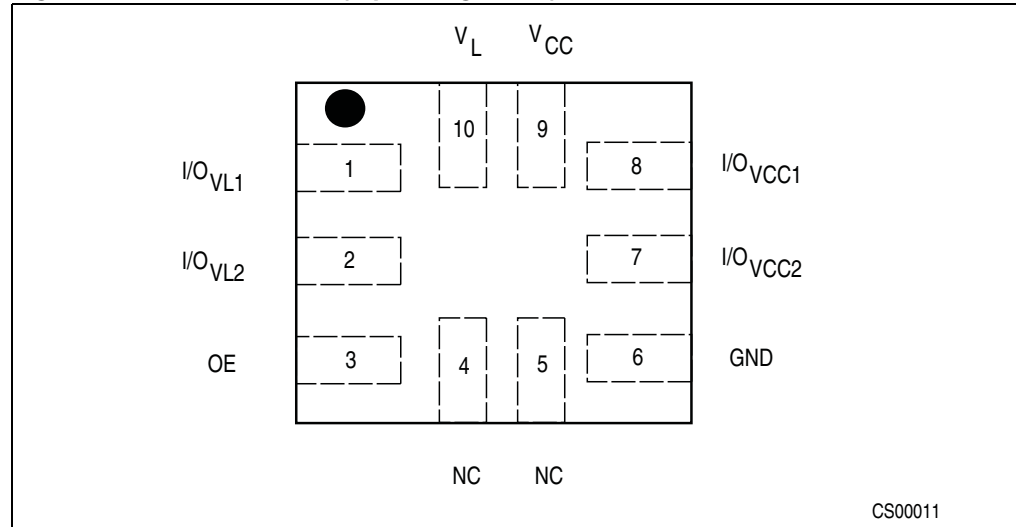
**Table 1. Device summary**

Order Code	Package	Packaging
ST2129QTR	QFN10 (1.8 x 1.4 mm)	Tape & reel (3000 parts per reel)

# 1 Pin settings

## 1.1 Pin connection

Figure 1. Pin connection (top through view)



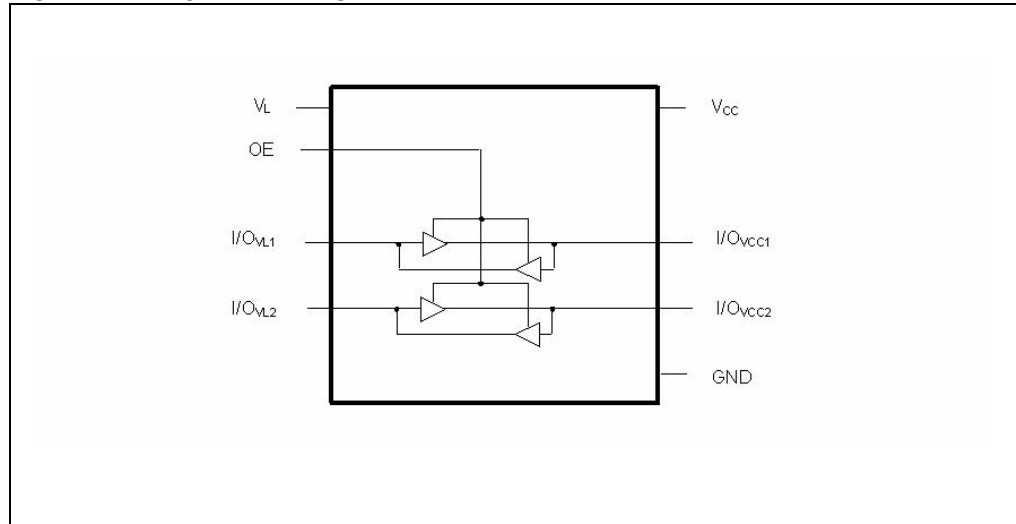
## 1.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	I/O <sub>VL1</sub>	Data input/output
2	I/O <sub>VL2</sub>	Data input/output
3	OE	Output enable
4	NC	No connection
5	NC	No connection
6	GND	Ground
7	I/O <sub>VCC2</sub>	Data input/output
8	I/O <sub>VCC1</sub>	Data input/output
9	V <sub>CC</sub>	Supply voltage
10	V <sub>L</sub>	Supply voltage

## 2 Logic diagram

Figure 2. Logic block diagram



### 2.1 Device block diagrams

Figure 3. ST2129 block diagram

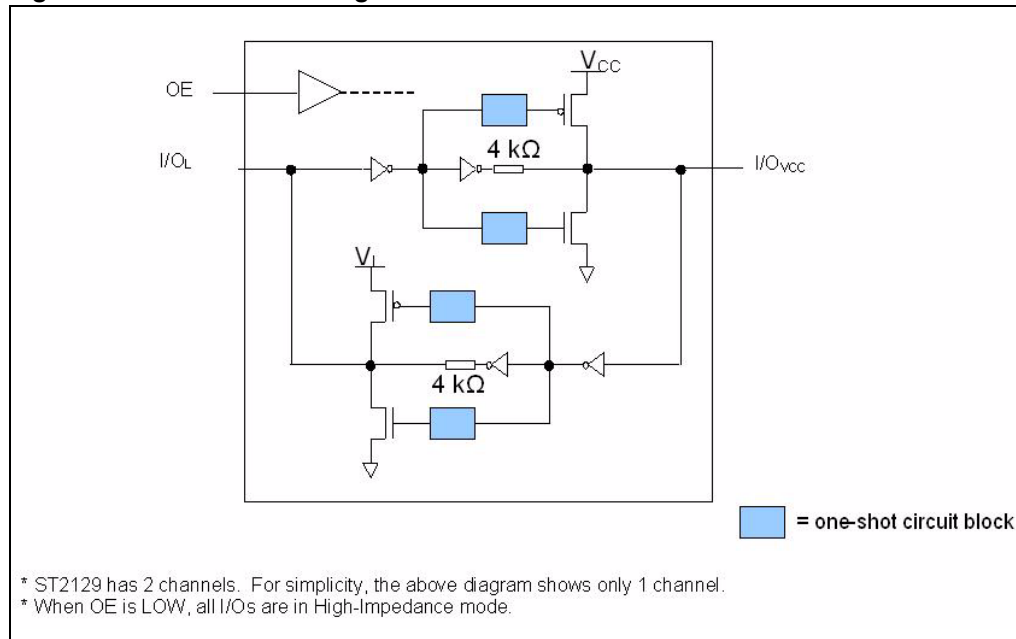
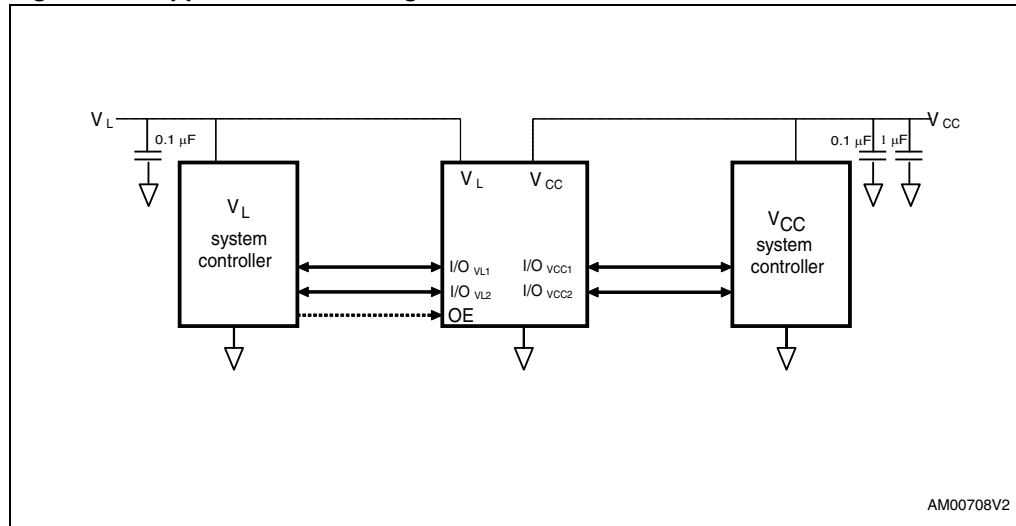


Figure 4. Application block diagram



## 3 Supplementary notes

### 3.1 Driver requirement

For proper operation, the driver from each side of the device must have the capability to source and sink a minimum of 1mA current. The device architecture requires the driver to source/sink a maximum current of  $(V_{CC}/4)$  mA to/from the weak 4 k $\Omega$  output buffer.

### 3.2 Load driving capability

To support the architecture that allows level translation without direction pin, the one-shot transistor is turned on only during state transition at the output side. After the one-shot transistor is turned off, only the 4 k $\Omega$  resistor maintains the state. So, resistive load or pull-up resistor less than 50 k $\Omega$  is not recommended for a proper operation.

### 3.3 Power off feature

In some applications, where it might be required to turn off one of the power supplies powering up the level translator, the device is automatically disabled when  $V_{CC}$  supply is turned off, even if the OE pin is set to HIGH (enabled). In this mode, all I/Os are in high impedance state.

### 3.4 Truth table

**Table 3. Truth table**

Enable	Bidirectional Input/Output	
OE	I/O <sub>VCC</sub>	I/O <sub>VL</sub>
H <sup>(1)</sup>	H <sup>(2)</sup>	H <sup>(1)</sup>
H <sup>(1)</sup>	L	L
L	Z <sup>(3)</sup>	Z <sup>(3)</sup>

(1) High level  $V_L$  power supply referred.

(2) High level  $V_{CC}$  power supply referred.

(3) Z = High impedance.

## 4 Maximum ratings

Stressing the device above the rating listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_L$	Supply voltage	-0.3 to 4.6	V
$V_{CC}$	Supply voltage	-0.3 to 6.5	V
$V_{OE}$	DC control input voltage	-0.3 to 6.5	V
$V_{I/OVL}$	DC I/O <sub>VL</sub> input voltage (OE = GND or $V_L$ )	-0.3 to $V_L + 0.3$	V
$V_{I/OVCC}$	DC I/O <sub>VCC</sub> input voltage (OE = GND or $V_L$ )	-0.3 to $V_{CC} + 0.3$	V
$I_{IK}$	DC input diode current	-20	mA
$I_{I/OVL}$	DC output current	±25	mA
$I_{I/OVCC}$	DC output current	±258	mA
$I_{SCTOUT}$	Short circuit duration, continuous	40	mA
$P_D$	Power dissipation <sup>(1)</sup>	500	mW
$T_{STG}$	Storage temperature	-65 to 150	°C
$T_L$	Lead temperature (10 seconds)	300	°C
ESD	Electrostatic discharge protection (HBM)	±2	kV

### 4.1 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_L$	Supply voltage	1.65	–	3.6	V
$V_{CC}$	Supply voltage	1.65	–	5.5	V
$V_{OE}$	Input voltage (OE output enable pin, $V_L$ power supply referred)	0	–	3.6	V
$V_{I/OVL}$	I/O <sub>VL</sub> voltage	0	–	$V_L$	V
$V_{I/OVCC}$	I/O <sub>VCC</sub> voltage	0	–	$V_{CC}$	V
$T_{OP}$	Operating temperature	-40	–	85	°C
dt/dV	Input rise and fall time	0	–	1	ns/V

## 5 Electrical characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ .

**Table 6. DC characteristics**

Symbol	Parameter	$V_L$	$V_{CC}$	Test conditions	Value					Unit
					$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min	Typ	Max	Min	Max	
$V_{IHL}$	High level input voltage ( $I/O_{VL}$ )	1.65	1.65 to 5.5		1.16	–	–	1.16	–	V
		1.8			1.26	–	–	1.26	–	
		2.5			1.75	–	–	1.75	–	
		3.0			2.10	–	–	2.10	–	
		3.6			2.52	–	–	2.52	–	
$V_{ILL}$	Low level input voltage ( $I/O_{VL}$ )	1.65	1.65 to 5.5		–	–	0.50	–	0.50	V
		1.8			–	–	0.54	–	0.54	
		2.5			–	–	0.75	–	0.75	
		3.0			–	–	0.90	–	0.90	
		3.6			–	–	1.08	–	1.08	
$V_{IHC}$	High level input voltage ( $I/O_{VCC}$ )	1.65 to 3.6	1.65		1.16	–	–	1.16	–	V
			1.8		1.26	–	–	1.26	–	
			2.5		1.75	–	–	1.75	–	
			3.0		2.10	–	–	2.10	–	
			3.6		2.52	–	–	2.52	–	
			4.3		3.01	–	–	3.01	–	
			5.5		3.85	–	–	3.85	–	
$V_{ILC}$	Low level input voltage ( $I/O_{VCC}$ )	1.65 to 3.6	1.65		–	–	0.50	–	0.50	V
			1.8		–	–	0.54	–	0.54	
			2.5		–	–	0.75	–	0.75	
			3.0		–	–	0.90	–	0.90	
			3.6		–	–	1.08	–	1.08	
			4.3		–	–	1.29	–	1.29	
			5.5		–	–	1.65	–	1.65	

Table 6. DC characteristics (continued)

Symbol	Parameter	$V_L$	$V_{CC}$	Test conditions	Value					Unit
					$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min	Typ	Max	Min	Max	
$V_{IH-OE}$	High level input voltage (OE)	1.65	1.65 to 5.5		1.16	–	–	1.16	–	V
		1.8			1.26	–	–	1.26	–	
		2.5			1.75	–	–	1.75	–	
		3.0			2.10	–	–	2.10	–	
		3.6			2.52	–	–	2.52	–	
$V_{IL-OE}$	Low level input voltage (OE)	1.65	1.65 to 5.5		–	–	0.50	–	0.50	V
		1.8			–	–	0.54	–	0.54	
		2.5			–	–	0.75	–	0.75	
		3.0			–	–	0.90	–	0.90	
		3.6			–	–	1.08	–	1.08	
$V_{OHL}$	High level output voltage ( $I/O_{VL}$ )	1.65 to 3.6	1.65 to 5.5	$I_O = -60\mu\text{A}$	$V_L - 0.4$	–	–	$V_L - 0.4$	–	V
$V_{OLL}$	Low level output voltage ( $I/O_{VL}$ )	1.65 to 3.6	1.65 to 5.5	$I_O = +60\mu\text{A}$	–	–	0.4	–	0.4	V
$V_{OHC}$	High level output voltage ( $I/O_{VCC}$ )	1.65 to 3.6	1.65 to 5.5	$I_O = -60\mu\text{A}$	$V_{CC} - 0.4$	–	–	$V_{CC} - 0.4$	–	V
$V_{OLC}$	Low level output voltage ( $I/O_{VCC}$ )	1.65 to 3.6	1.65 to 5.5	$I_O = +60\mu\text{A}$	–	–	0.4	–	0.4	V



Table 7. DC characteristics

Symbol	Parameter	V <sub>L</sub>	V <sub>CC</sub>	Test conditions	Value					Unit
					T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
I <sub>OE</sub>	Control input leakage current (OE)	1.65 to 3.6	1.65 to 5.5	V <sub>I</sub> = GND or V <sub>L</sub>	–	–	0.1	–	1	µA
I <sub>IO_LKG</sub>	High impedance leakage current (I/O <sub>VL</sub> , I/O <sub>VCC</sub> )	1.65 to 3.6	1.65 to 5.5	OE = GND I/O <sub>VL</sub> = High I/O <sub>VCC</sub> = Low	–	–	0.1	–	1	µA
				OE = GND I/O <sub>VL</sub> = Low I/O <sub>VCC</sub> = High	–	–	0.1	–	1	µA
I <sub>OFF</sub>	Partial power down current	1.65 to 3.6	0	OE = V <sub>L</sub> or GND I/O <sub>VL</sub> = High I/O <sub>VCC</sub> = Low	–	–	0.1	–	1	µA
				OE = V <sub>L</sub> or GND I/O <sub>VL</sub> = Low I/O <sub>VCC</sub> = High	–	–	0.1	–	1	
I <sub>QVCC</sub>	Quiescent supply current V <sub>CC</sub>	1.65 to 3.6	1.65 to 5.5	OE = V <sub>L</sub> I/O = Hi-Z	–	–	3.5	–	4.5	µA
I <sub>QVL</sub>	Quiescent supply current V <sub>L</sub>	1.65 to 3.6	1.65 to 5.5	OE = V <sub>L</sub> I/O = Hi-Z	–	–	0.1	–	1	µA
		1.65 to 3.6	0		–	–	0.1	–	1	
I <sub>Z-VCC</sub>	High Impedance quiescent supply current V <sub>CC</sub>	1.65 to 3.6	1.65 to 5.5	OE = GND I/O = Hi-Z	–	–	0.1	–	1	µA
I <sub>Z-VL</sub>	High impedance quiescent supply current V <sub>L</sub>	1.65 to 3.6	1.65 to 5.5	OE = GND I/O = Hi-Z	–	–	0.1	–	1	µA
		1.65 to 3.6	0		–	–	0.1	–	1	

## 6 AC characteristics

Load  $C_L = 15$  pF; driver  $t_r = t_f \leq 2$  ns over temperature range  $-40$  °C to  $85$  °C.

**Table 8. AC characteristics - test conditions:  $V_L = 1.65 - 1.95$  V**

Symbol	Parameter	$V_{CC} = 1.65 - 1.95$ V		$V_{CC} = 2.3 - 2.7$ V		$V_{CC} = 3.0 - 3.6$ V		$V_{CC} = 4.5 - 5.5$ V		Unit	
		Min	Max	Min	Max	Min	Max	Min	Max		
$t_{RVCC}$	Rise time $I/O_{VCC}$	–	5.0	–	3.2	–	2.4	–	1.4	ns	
$t_{FVCC}$	Fall time $I/O_{VCC}$	–	1.5	–	1.4	–	1.3	–	1.2	ns	
$t_{RVL}$	Rise time $I/O_{VL}$	–	2.8	–	2.7	–	2.6	–	2.6	ns	
$t_{FVL}$	Fall time $I/O_{VL}$	–	1.5	–	1.4	–	1.4	–	1.3	ns	
$t_{I/OVL-VCC}$	Propagation delay time $I/O_{VL-LH}$ to $I/O_{VCC-LH}$ $I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PLH}$	–	6.6	–	5.8	–	5.0	–	4.4	ns
		$t_{PHL}$	–	4.1	–	3.8	–	3.6	–	3.4	ns
$t_{I/OVCC-VL}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PLH}$	–	4.9	–	4.4	–	4.1	–	4.4	ns
		$t_{PHL}$	–	4.6	–	4.2	–	4.0	–	3.6	ns
$t_{PZL}$ $t_{PZH}$	Output enable time	–	27	–	27	–	27	–	27	ns	
$t_{PLZ}$ $t_{PHZ}$	Output disable time	–	145	–	145	–	145	–	145		
$D_R$	Data rate <sup>(1)</sup>	41	–	66	–	84	–	86	–	Mbps	

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty-cycle and output I/O signal duty-cycle deviation is less than  $50\% \pm 10\%$ .

**Table 9. AC characteristics - test conditions:  $V_L = 2.3 - 2.7$  V**

Symbol	Parameter	$V_{CC} = 2.3 - 2.7$ V		$V_{CC} = 3.0 - 3.6$ V		$V_{CC} = 4.5 - 5.5$ V		Unit	
		Min	Max	Min	Max	Min	Max		
$t_{RVCC}$	Rise time $I/O_{VCC}$	–	3.3	–	2.2	–	1.6	ns	
$t_{FVCC}$	Fall time $I/O_{VCC}$	–	1.7	–	1.6	–	1.4	ns	
$t_{RVL}$	Rise time $I/O_{VL}$	–	2.2	–	2.0	–	1.9	ns	
$t_{FVL}$	Fall time $I/O_{VL}$	–	1.3	–	1.2	–	1.2	ns	
$t_{I/OVL-VCC}$	Propagation delay time $I/O_{VL-LH}$ to $I/O_{VCC-LH}$ $I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PLH}$	–	4.6	–	4.3	–	3.9	ns
		$t_{PHL}$	–	3.6	–	3.3	–	2.9	ns
$t_{I/OVCC-VL}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PLH}$	–	3.9	–	3.5	–	3.5	ns
		$t_{PHL}$	–	3.6	–	3.0	–	2.5	ns
$t_{PZL}$ $t_{PZH}$	Output enable time	–	20	–	20	–	20	ns	
$t_{PLZ}$ $t_{PHZ}$	Output disable time	–	130	–	130	–	130		
$D_R$	Data rate <sup>(1)</sup>	84	–	85	–	88	–	Mbps	

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty-cycle and output I/O signal duty-cycle deviation is less than  $50\% \pm 10\%$ .

**Table 10. AC characteristics - test conditions:  $V_L = 3.0 - 3.6$  V**

Symbol	Parameter	$V_{CC} = 3.0 - 3.6$ V		$V_{CC} = 4.5 - 5.5$ V		Unit	
		Min	Max	Min	Max		
$t_{RVCC}$	Rise time $I/O_{VCC}$	–	1.8	–	1.7	ns	
$t_{FVCC}$	Fall time $I/O_{VCC}$	–	1.3	–	1.2	ns	
$t_{RVL}$	Rise time $I/O_{VL}$	–	1.6	–	1.5	ns	
$t_{FVL}$	Fall time $I/O_{VL}$	–	1.1	–	1.1	ns	
$t_{I/OVL-VCC}$	Propagation delay time $I/O_{VL-LH}$ to $I/O_{VCC-LH}$ $I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PLH}$	–	4.1	–	4.1	ns
		$t_{PHL}$	–	2.6	–	2.3	ns
$t_{I/OVCC-VL}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PLH}$	–	4.0	–	4.0	ns
		$t_{PHL}$	–	2.6	–	2.4	ns

Table 10. AC characteristics - test conditions:  $V_L = 3.0 - 3.6 \text{ V}$  (continued)

Symbol	Parameter	$V_{CC} = 3.0 - 3.6 \text{ V}$		$V_{CC} = 4.5 - 5.5 \text{ V}$		Unit
		Min	Max	Min	Max	
$t_{PZL} t_{PZH}$	Output enable time	–	15	–	15	ns
$t_{PLZ} t_{PHZ}$	Output disable time	–	110	–	110	
$D_R$	Data rate <sup>(1)</sup>	86	–	89	–	Mbps

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty-cycle and output I/O signal duty-cycle deviation is less than  $50\% \pm 10\%$ .

## 7 Test circuit

Figure 5. Test circuit

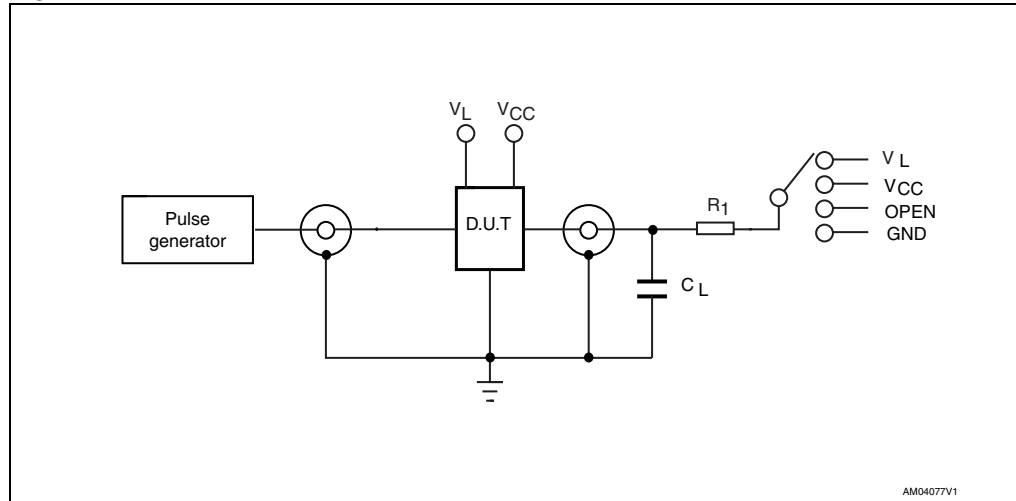


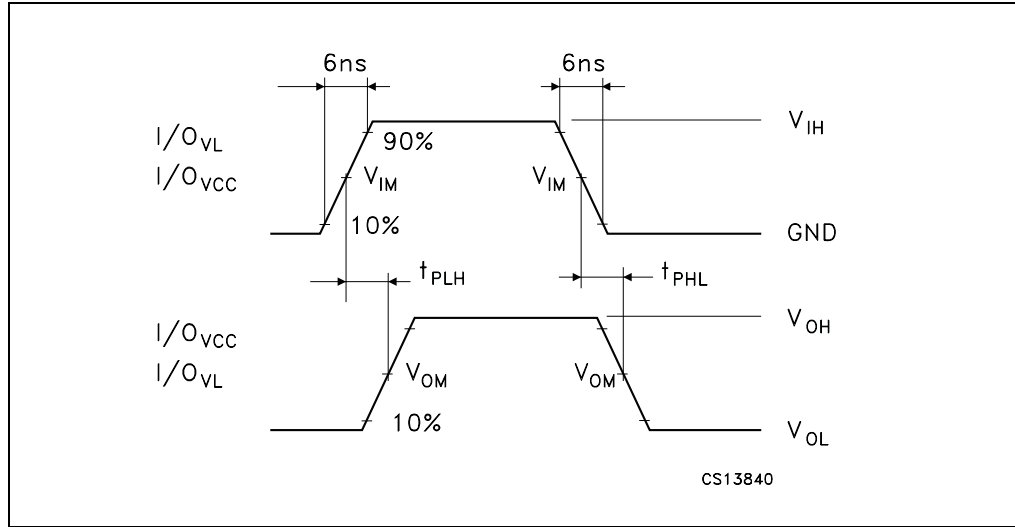
Table 11. Test circuit switches

Test	$C_L$	$R_1$	Switch
$t_{PLH}$ , $t_{PHL}$	15 pF	20 k $\Omega$	Open
$t_r$ , $t_f$	15 pF	20 k $\Omega$	Open
$t_{PZL}$ , $t_{PLZ}$	15 pF	20 k $\Omega$	$V_L$ or $V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	15 pF	20 k $\Omega$	GND

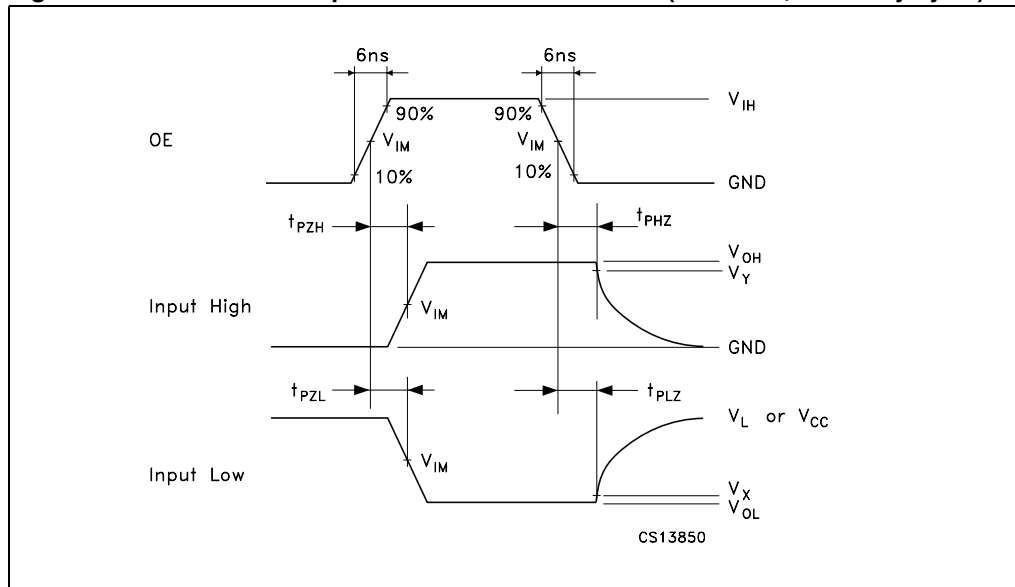
Table 12. Waveform symbol value

Symbol	Driving I/O $V_L$		Driving I/O $V_{CC}$	
	$1.65V \leq V_L \leq V_{CC} \leq 2.5V$	$3.3V \leq V_L \leq V_{CC} \leq 5.5V$	$1.65V \leq V_L \leq V_{CC} \leq 2.5V$	$3.3V \leq V_L \leq V_{CC} \leq 5.5V$
$V_{IH}$	$V_L$	$V_L$	$V_{CC}$	$V_{CC}$
$V_{IM}$	50% $V_L$	50% $V_L$	50% $V_{CC}$	50% $V_{CC}$
$V_{OM}$	50% $V_{CC}$	50% $V_{CC}$	50% $V_L$	50% $V_L$
$V_X$	$V_{OL} + 0.15V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.3V$
$V_Y$	$V_{OH} - 0.15V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.3V$

**Figure 6. Waveform - propagation delay (f = 1 MHz, 50% duty cycle)**



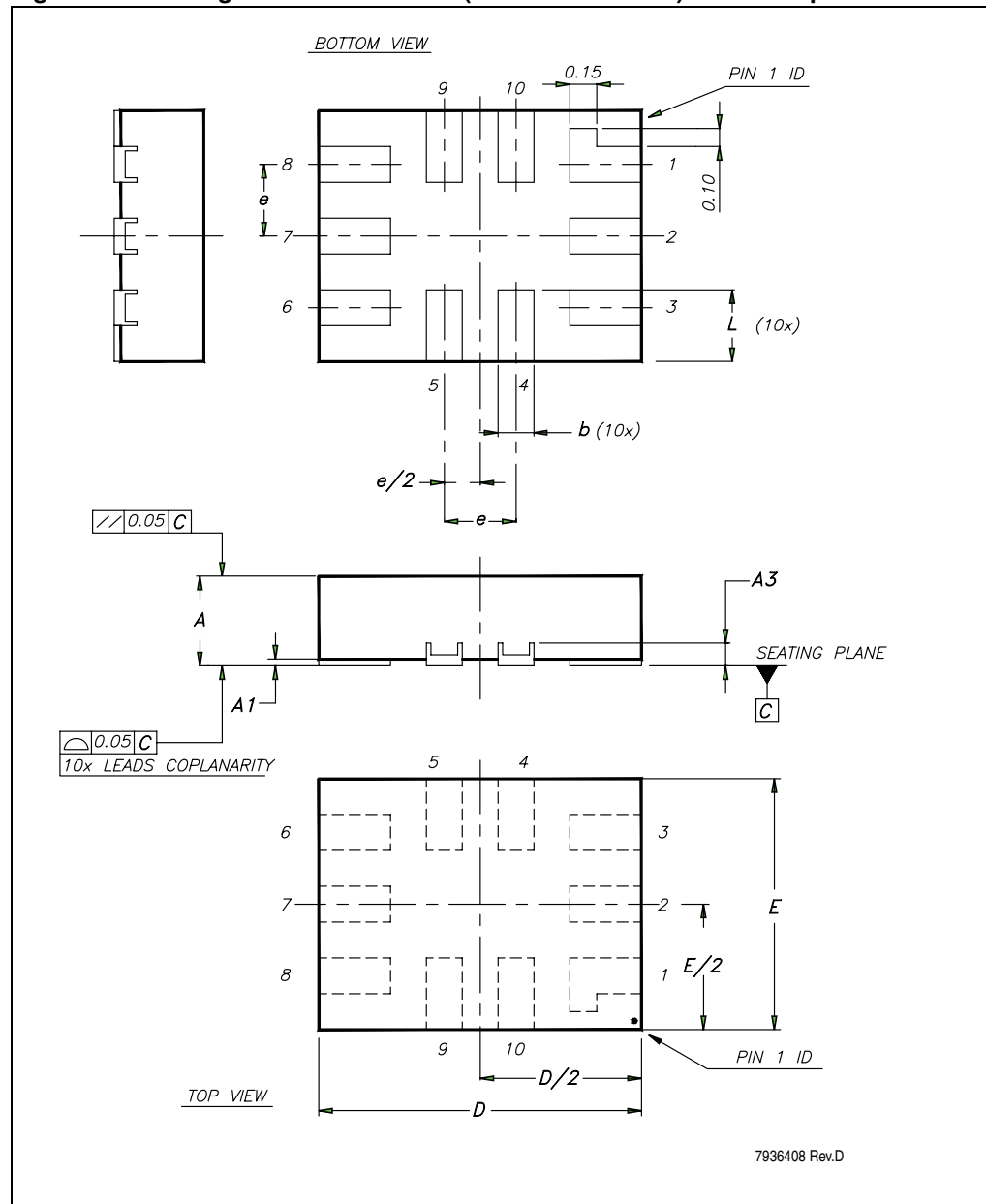
**Figure 7. Waveform - output enable and disable time (f = 1 MHz, 50% duty cycle)**



## 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Figure 8. Package outline for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch**



**Table 13. Mechanical data for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch**

Symbol	Millimeters		
	Typ	Min	Max
A	0.50	0.45	0.55
A1	0.02	0	0.05
A3	0.127	–	–
b	0.20	0.15	0.25
D	1.80	1.75	1.85
E	1.40	1.35	1.45
e	0.40	–	–
L	0.40	0.35	0.45

**Figure 9. Footprint recommendation for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch**

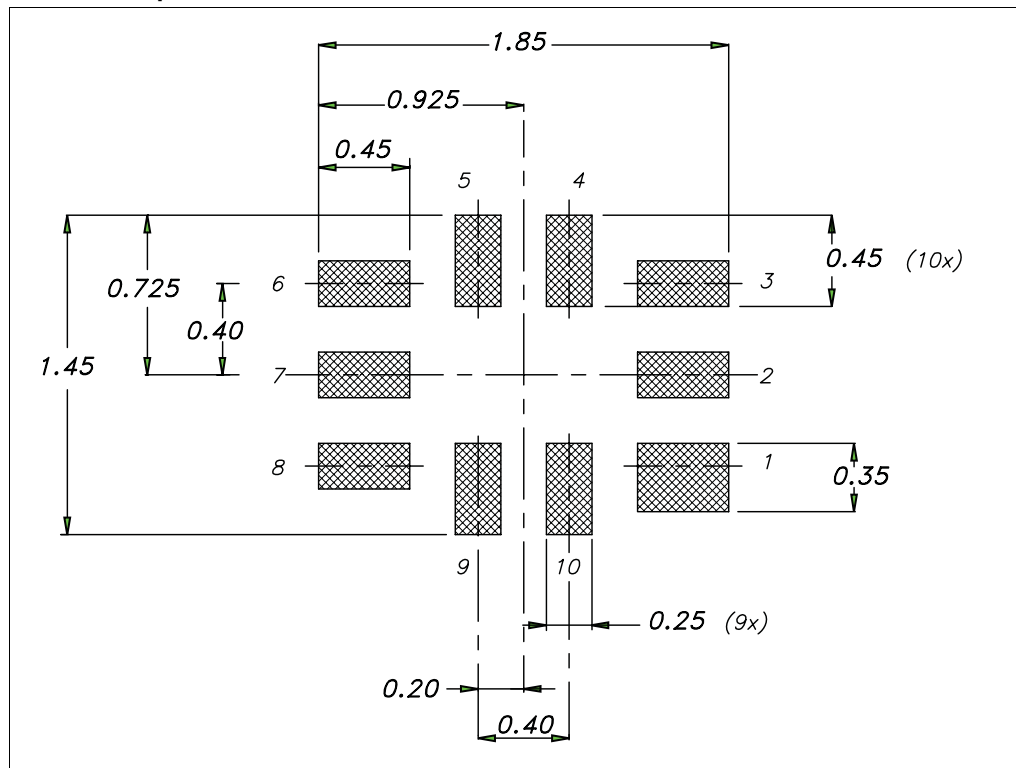




Figure 10. Carrier tape for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

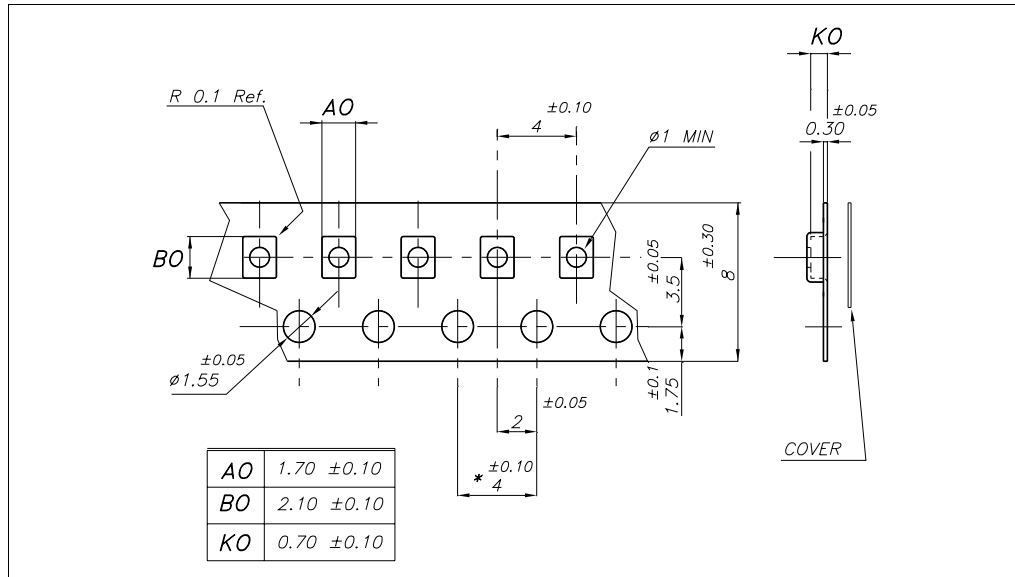


Figure 11. Reel information for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

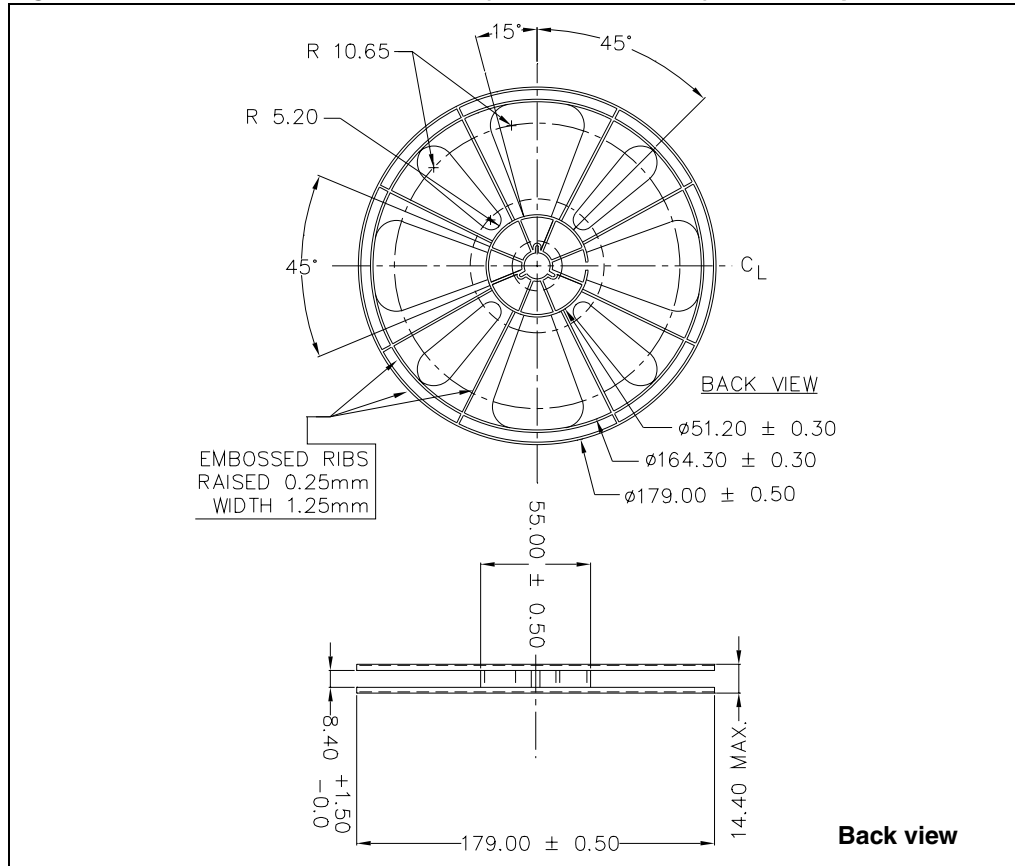
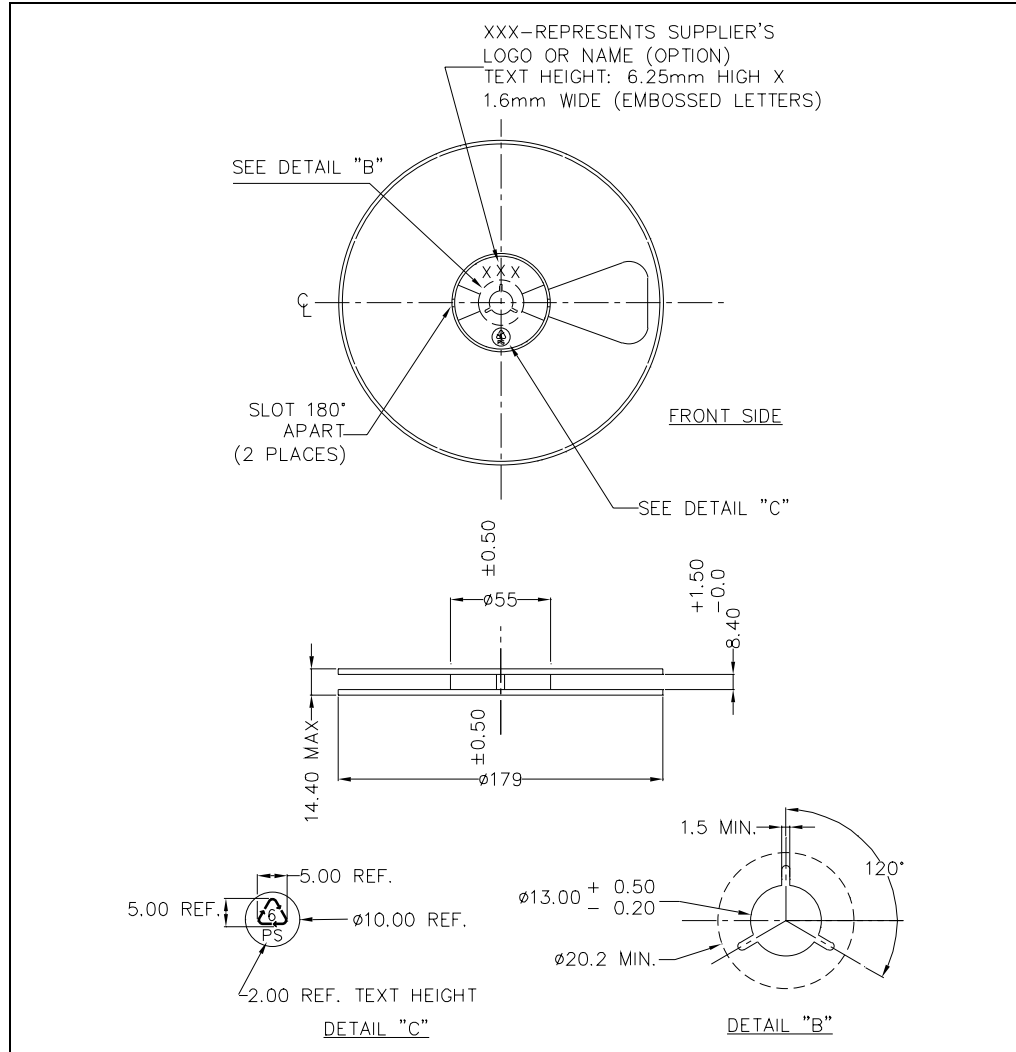


Figure 12. Reel information for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch



## 9 Revision history

Table 14. Document revision history

Date	Revision	Changes
07-Sep-2009	1	Initial release.

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