FAIRCHILD SEMICONDUCTOR™

May 1988
Revised January 2004

74F382
4-Bit Arithmetic Logic Unit

General Description

The 74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, refer to the 74F381 data sheet.

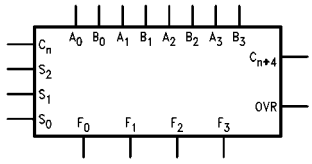
Features

- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- LOW input loading minimizes drive requirements
- Carry output for ripple expansion
- Overflow output for twos complement arithmetic

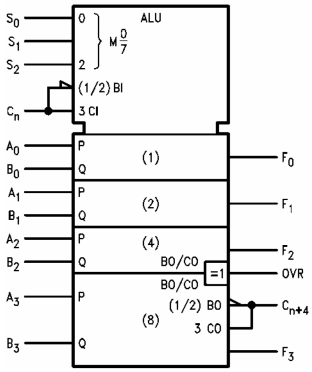
Ordering Code:

Order Number	Package Number	Package Description
74F382SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F382SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F382PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

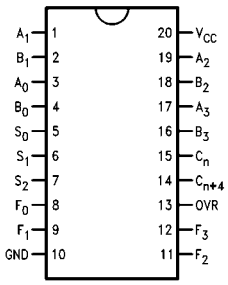
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_3	A Operand Inputs	1.0/4.0	20 µA/–2.4 mA
B_0–B_3	B Operand Inputs	1.0/4.0	20 µA/–2.4 mA
S_0–S_2	Function Select Inputs	1.0/1.0	20 µA/–0.6 mA
C_n	Carry Input	1.0/5.0	20 µA/–3.0 mA
C_{n+4}	Carry Output	50/33.3	–1 mA/20 mA
OVR	Overflow Output	50/33.3	–1 mA/20 mA
F_0–F_3	Function Outputs	50/33.3	–1 mA/20 mA

Functional Description

Signals applied to the Select inputs S_0–S_2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands, LOW for active LOW operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 2. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a HIGH signal on OVR indicates overflow in twos complement operation. Typical delays for Figure 2 are given in Figure 1.

Function Select Table

Select			Operation
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A ⊕ B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level
L = LOW Voltage Level

Path Segment	Toward F	Output C_{n+4}, OVR
A_1 or B_1 to C_{n+4}	6.5 ns	6.5 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

FIGURE 1. 16-Bit Delay Tabulation

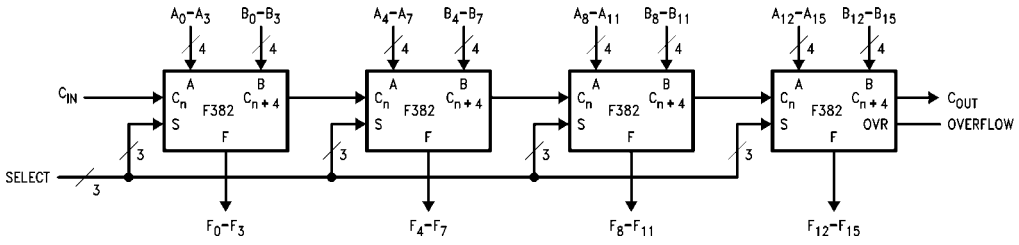


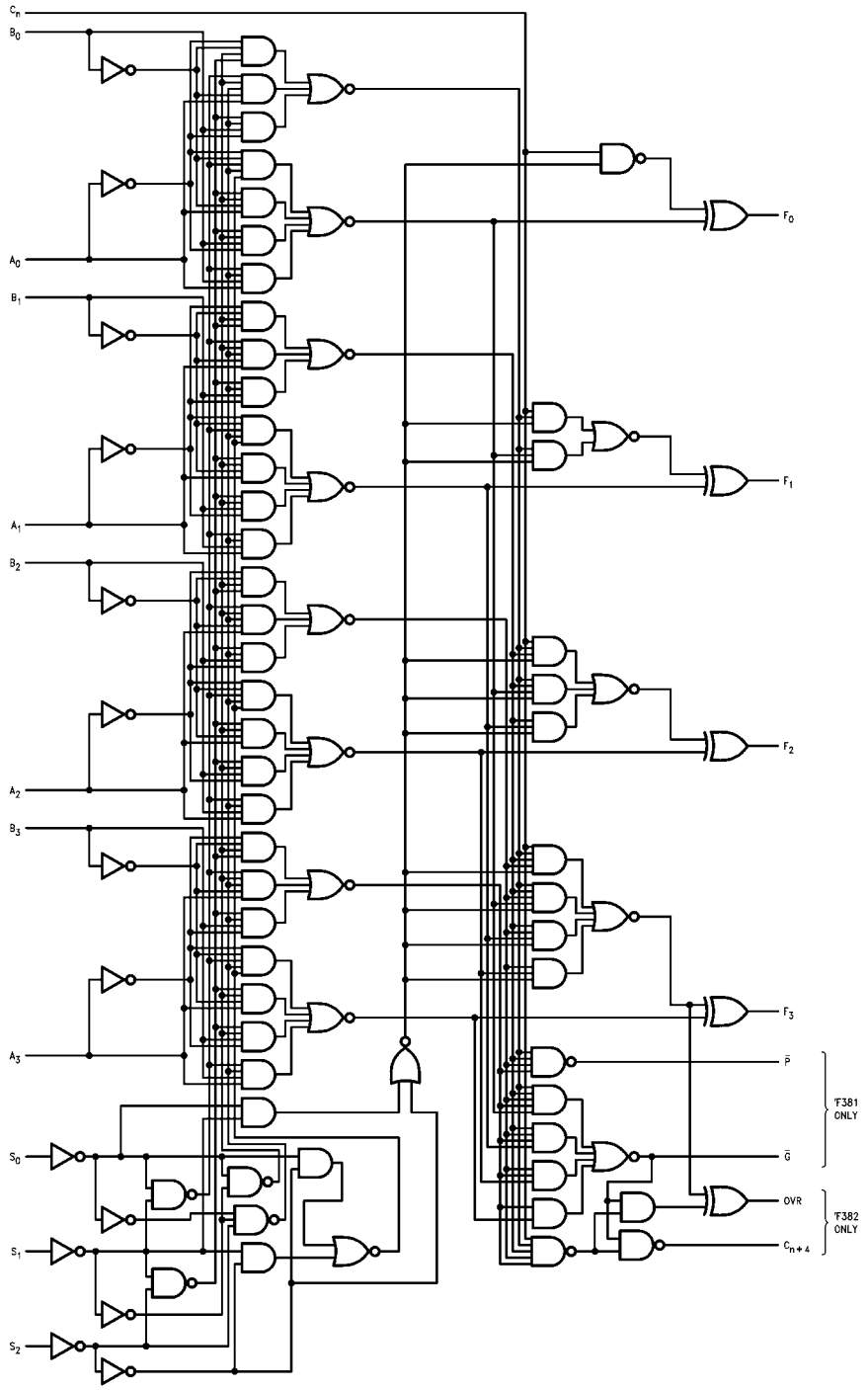
FIGURE 2. 16-Bit Ripply Carry ALU Expansion

Truth Table

	Inputs						Outputs					
Function	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	**OVR**	C_{n+4}
CLEAR	L	L	L	L	X	X	L	L	L	L	H	H
				H	X	X	L	L	L	L	H	H
B MINUS A	H	L	L	L	L	L	H	H	H	H	L	L
				L	L	H	L	H	H	H	L	H
				L	H	L	L	L	L	L	L	L
				L	H	H	H	H	H	H	L	L
				H	L	L	L	L	L	L	L	H
				H	L	H	H	H	H	H	L	H
				H	H	L	H	L	L	L	L	L
				H	H	H	L	L	L	L	L	H
A MINUS B	L	H	L	L	L	L	H	H	H	H	L	L
				L	L	H	L	L	L	L	L	L
				L	H	L	L	H	H	H	L	H
				L	H	H	H	H	H	H	L	L
				H	L	L	L	L	L	L	L	H
				H	L	H	H	L	L	L	L	L
				H	H	L	H	H	H	H	L	H
				H	H	H	L	L	L	L	L	H
A PLUS B	H	H	L	L	L	L	L	L	L	L	L	L
				L	L	H	H	H	H	H	L	L
				L	H	L	H	H	H	H	L	L
				L	H	H	L	H	H	H	L	H
				H	L	L	H	L	L	L	L	L
				H	L	H	L	L	L	L	L	H
				H	H	L	L	L	L	L	L	H
				H	H	H	H	H	H	H	L	H
A ⊕ B	L	L	H	X	L	L	L	L	L	L	L	L
				X	L	H	H	H	H	H	L	L
				L	H	L	H	H	H	H	L	L
				X	H	H	L	L	L	L	H	H
				H	H	L	H	H	H	H	H	H
A + B	H	L	H	X	L	L	L	L	L	L	L	L
				X	L	H	H	H	H	H	L	L
				X	H	L	H	H	H	H	L	L
				L	H	H	H	H	H	H	L	L
				H	H	H	H	H	H	H	H	H
AB	L	H	H	X	L	L	L	L	L	L	H	H
				X	L	H	L	L	L	L	L	L
				X	H	L	L	L	L	L	H	H
				L	H	H	H	H	H	H	L	L
				H	H	H	H	H	H	H	H	H
PRESET	H	H	H	X	L	L	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	H	L	H	H	H	H	L	L
				L	H	H	H	H	H	H	L	L
				H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

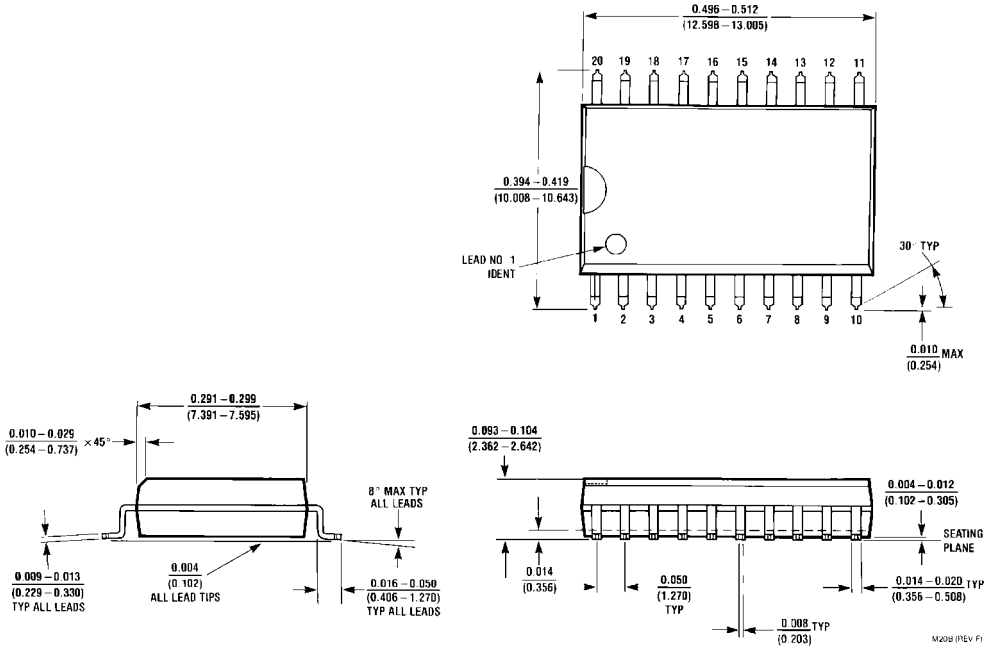
DC Electrical Characteristics over Operating Temperature Range unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (S_0 – S_2)
					−2.4			V_{IN} = 0.5V (A_0 – A_3, B_0 – B_3)
					−3.0			V_{IN} = 0.5V (C_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			54	81	mA	Max	

AC Electrical Characteristics

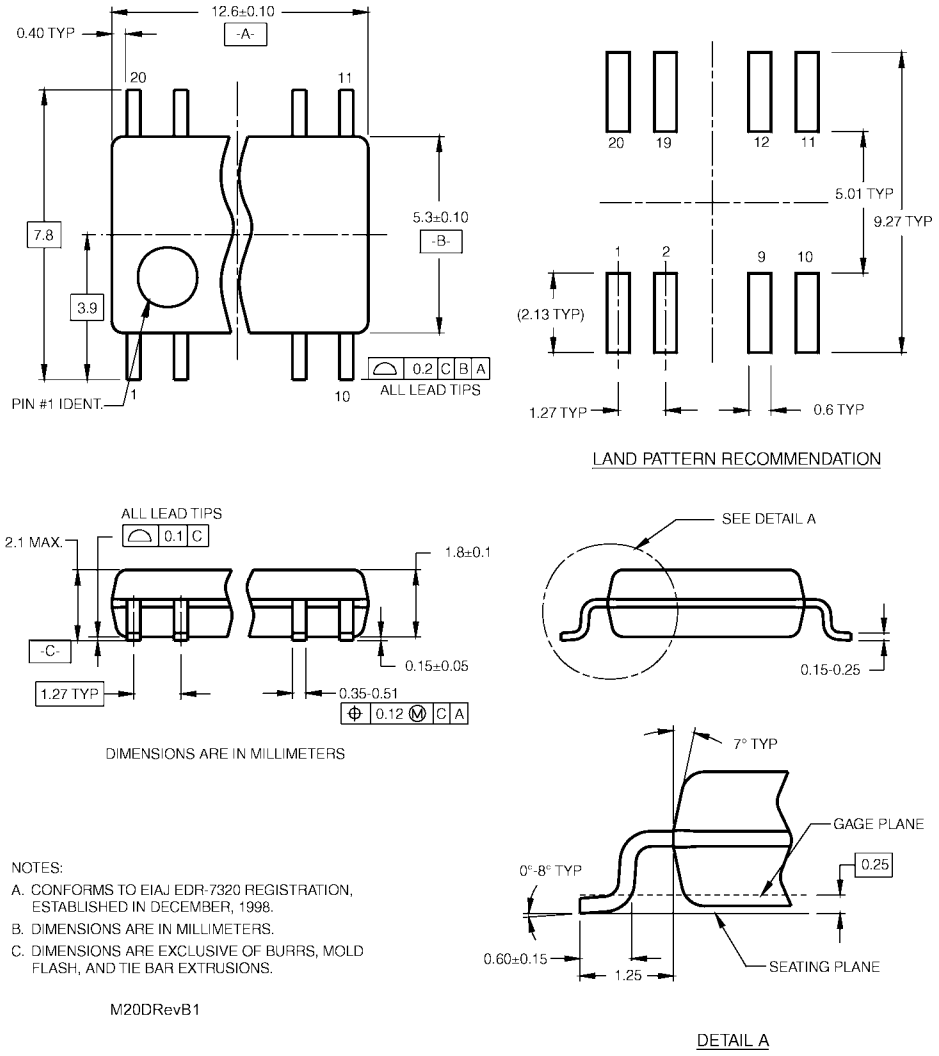
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	8.1	12.0	3.0	13.0	ns
t_{PHL}	C_n to F_i	2.5	5.7	8.0	2.5	9.0	
t_{PLH}	Propagation Delay	4.0	10.4	15.0	3.5	17.0	ns
t_{PHL}	Any A or B to Any F	3.0	8.2	11.0	2.5	12.0	
t_{PLH}	Propagation Delay	6.5	11.0	20.5	5.5	21.5	ns
t_{PHL}	S_i to F_i	4.0	8.2	15.0	4.0	17.5	
t_{PLH}	Propagation Delay	3.5	6.0	8.5	3.5	11.0	ns
t_{PHL}	A_i or B_i to $C_n + 4$	3.5	6.5	9.0	3.5	10.5	
t_{PLH}	Propagation Delay	7.0	12.5	16.5	7.0	17.5	ns
t_{PHL}	S_i to OVR or C_{n+4}	5.0	9.0	12.0	5.0	14.5	
t_{PLH}	Propagation Delay	2.5	5.6	8.0	2.0	9.0	ns
t_{PHL}	C_n to C_{n+4}	3.5	6.3	9.0	2.0	10.0	
t_{PLH}	Propagation Delay	3.5	8.0	11.0	3.5	13.0	ns
t_{PHL}	C_n to OVR	2.5	7.1	10.0	2.5	11.0	
t_{PLH}	Propagation Delay	7.0	11.5	15.5	7.0	16.5	ns
t_{PHL}	A_i or B_i to OVR	3.0	8.0	10.5	3.0	11.5	

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

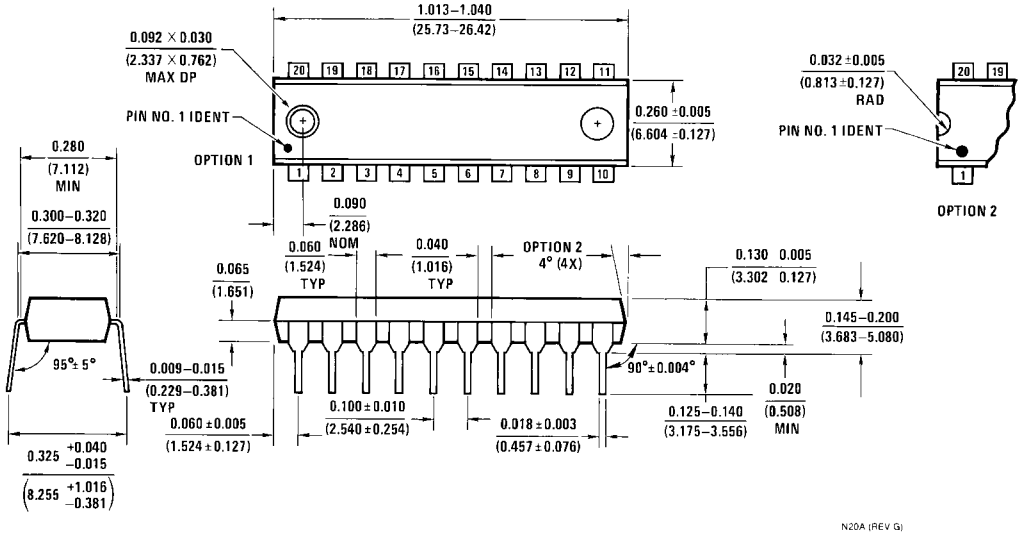
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A