# MC100EP16F

# 3.3V / 5V ECL Differential Receiver/Driver With Reduced Output Swing

ON Semiconductor®

http://onsemi.com

### Description

The MC100EP16F is a differential receiver/driver. The device is functionally equivalent to the EP16 device with higher performance capabilities. With reduced output swings, rise/fall transition times are significantly faster than on the EP16. The EP16F is ideally suited for interfacing with high frequency sources.

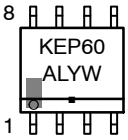
The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

### Features

- 100 ps Typical Rise and Fall Time
- Max Frequency >4 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC}$ = 3.0 V to 5.5 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range: $V_{CC}$ = 0V with $V_{EE}$ = −3.0 V to −5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Pb−Free Packages are Available

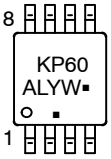
### MARKING DIAGRAMS*

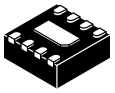

**SOIC−8**
**D SUFFIX**
**CASE 751**



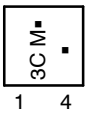


**TSSOP−8**
**DT SUFFIX**
**CASE 948R**



**DFN8**
**MN SUFFIX**
**CASE 506AA**




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

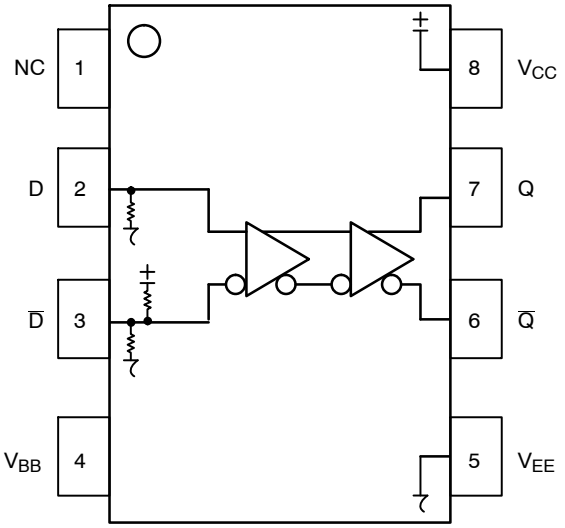



**Figure 1. 8−Lead Pinout** (Top View) **and Logic Diagram**

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| D*, $\overline{D}$** | ECL Data Inputs |
| Q, $\overline{Q}$ | ECL Data Outputs |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |
| EP | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

* Pins will default LOW when left open.

** Pins will default to $V_{CC}/2$ when left open.

**Table 2. ATTRIBUTES**

| Characteristics | | Value | |
|---|---|---|---|
| Internal Input Pulldown Resistor | | 75 kΩ | |
| Internal Input Pullup Resistor | | 37.5 kΩ | |
| ESD Protection | Human Body Model<br>Machine Model<br>Charged Device Model | > 4 kV<br>> 200 V<br>> 2 kV | |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Pb Pkg | Pb−Free Pkg |
| | SOIC−8<br>TSSOP−8<br>DFN8 | Level 1<br>Level 1<br>Level 1 | Level 1<br>Level 3<br>Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| Transistor Count | | 139 | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 6 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −6 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>−6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | 8 SOIC<br>8 SOIC | 190<br>130 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | 8 SOIC | 41 to 44 ± 5% | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | 8 TSSOP<br>8 TSSOP | 185<br>140 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | 8 TSSOP | 41 to 44 ± 5% | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | DFN8<br>DFN8 | 129<br>84 | °C/W<br>°C/W |
| $T_{sol}$ | Wave Solder Pb<br>Pb−Free | <2 to 3 sec @ 248°C<br><2 to 3 sec @ 260°C | | 265<br>265 | °C |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | (Note 2) | DFN8 | 35 to 40 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

**Table 4. DC CHARACTERISTICS, PECL** $V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 3)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 23 | 28 | 40 | 25 | 33 | 45 | 26 | 33 | 45 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 4) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 4) | 1525 | 1690 | 1775 | 1525 | 1690 | 1775 | 1525 | 1690 | 1775 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Note 5) | 1355 | | 1675 | 1355 | | 1675 | 1355 | | 1675 | mV |
| $V_{BB}$ | Output Voltage Reference | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current D<br>$\overline{D}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.3 V to −2.2 V.
4. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
5. Not recommended for Single−Ended operation when using an EP16F to drive another EP16F. $V_{OL}$ has reduced output swing and may not meet the $V_{IL}$ specification over temperature.
6. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 5. DC CHARACTERISTICS, PECL** $V_{CC}$ = 5.0 V, $V_{EE}$ = 0 V (Note 7)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 23 | 28 | 40 | 25 | 35 | 45 | 26 | 33 | 45 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 8) | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 8) | 3225 | 3390 | 3475 | 3225 | 3390 | 3475 | 3225 | 3390 | 3475 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 3775 | | 4120 | 3775 | | 4120 | 3775 | | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Note 9) | 3055 | | 3375 | 3055 | | 3375 | 3055 | | 3375 | mV |
| $V_{BB}$ | Output Voltage Reference | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10) | 2.0 | | 5.0 | 2.0 | | 5.0 | 2.0 | | 5.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current D<br>$\overline{D}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +2.0 V to −0.5 V.
8. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
9. Not recommended for Single−Ended operation when using an EP16F to drive another EP16F. $V_{OL}$ has reduced output swing and may not meet the $V_{IL}$ specification over temperature.
10. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 6. DC CHARACTERISTICS, NECL** $V_{CC}$ = 0 V; $V_{EE}$ = −5.5 V to −3.0 V (Note 11)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 23 | 28 | 40 | 25 | 34 | 45 | 26 | 33 | 45 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 12) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 12) | −1775 | −1610 | −1525 | −1775 | −1610 | −1525 | −1775 | −1610 | −1525 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | −1225 | | −880 | −1225 | | −880 | −1225 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Note 13) | −1810 | | −1625 | −1810 | | −1625 | −1810 | | −1625 | mV |
| $V_{BB}$ | Output Voltage Reference | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 14) | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current D<br>$\overline{D}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with $V_{CC}$.
12. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
13. Not recommended for Single−Ended operation when using an EP16F to drive another EP16F. $V_{OL}$ has reduced output swing and may not meet the $V_{IL}$ specification over temperature.
14. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 7. AC CHARACTERISTICS** $V_{CC}$ = 0 V; $V_{EE}$ = −3.0 V to −5.5 V or $V_{CC}$ = 3.0 V to 5.5 V; $V_{EE}$ = 0 V (Note 15)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Toggle Frequency (See Figure 2. $F_{max}$/JITTER) | | > 4 | | | > 4 | | | > 4 | | GHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential | 170 | 210 | 250 | 180 | 220 | 260 | 200 | 250 | 300 | ps |
| $t_{SKEW}$ | Duty Cycle Skew | | 5.0 | 20 | | 5.0 | 20 | | 5.0 | 20 | ps |
| $t_{JITTER}$ | Cycle−to−Cycle Jitter (RMS) (See Figure 2. $F_{max}$/JITTER) | | 0.2 | < 1 | | 0.2 | < 1 | | 0.2 | < 1 | ps |
| $V_{PP}$ | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times Q<br>(20% − 80%) | 70 | 85 | 110 | 80 | 100 | 120 | 90 | 110 | 130 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

15. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$−2.0 V.

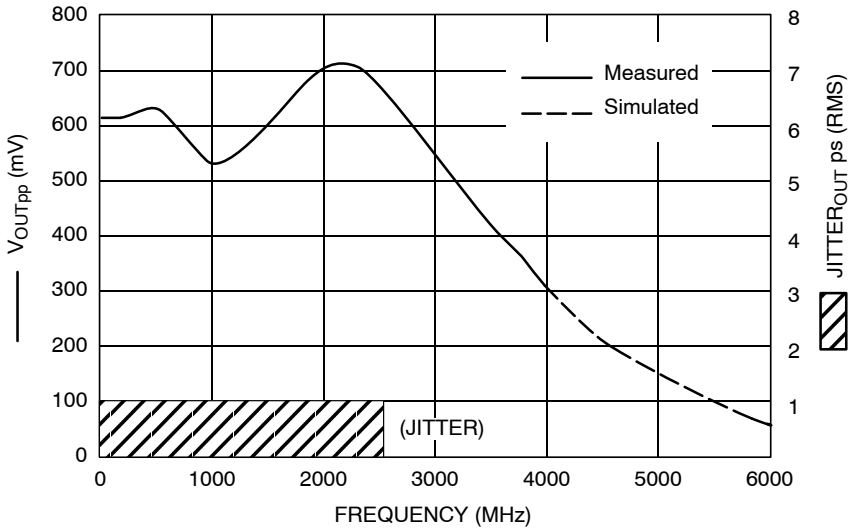



**Figure 2. $F_{max/JITTER}$**

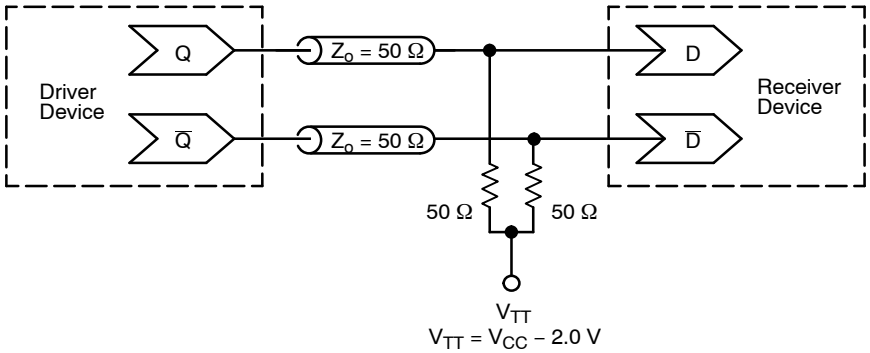



**Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC100EP16FD | SOIC−8 | 98 Units / Rail |
| MC100EP16FDG | SOIC−8 (Pb−Free) | 98 Units / Rail |
| MC100EP16FDR2 | SOIC−8 | 2500 / Tape & Reel |
| MC100EP16FDR2G | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |
| MC100EP16FDT | TSSOP−8 | 100 Units / Rail |
| MC100EP16FDTG | TSSOP−8 (Pb−Free) | 100 Units / Rail |
| MC100EP16FDTR2 | TSSOP−8 | 2500 / Tape & Reel |
| MC100EP16FDTR2G | TSSOP−8 (Pb−Free) | 2500 / Tape & Reel |
| MC100EP16FMNR4 | DFN8 | 1000 / Tape & Reel |
| MC100EP16FMNR4G | DFN8 (Pb−Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

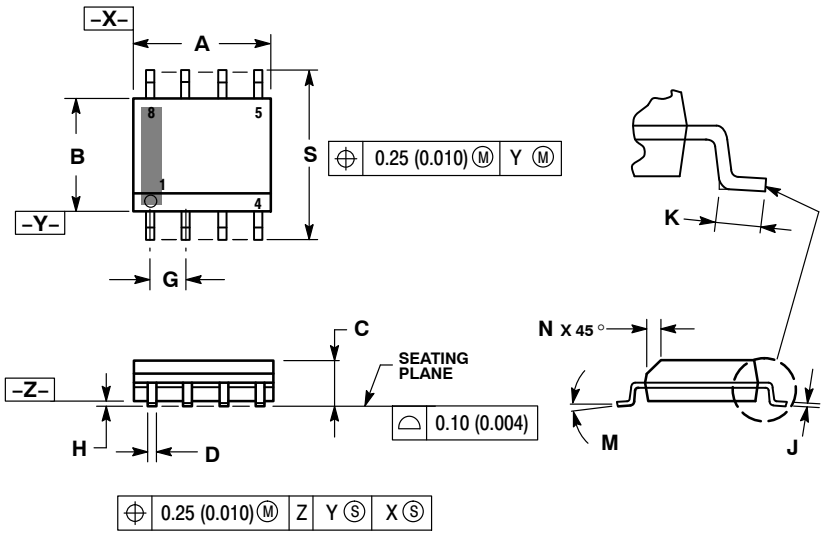
**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

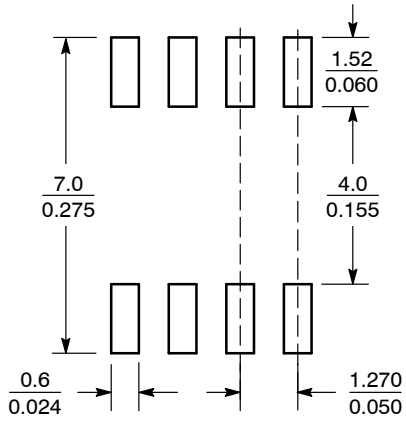
**SOIC−8 NB**
CASE 751−07
ISSUE AH




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

## SOLDERING FOOTPRINT*

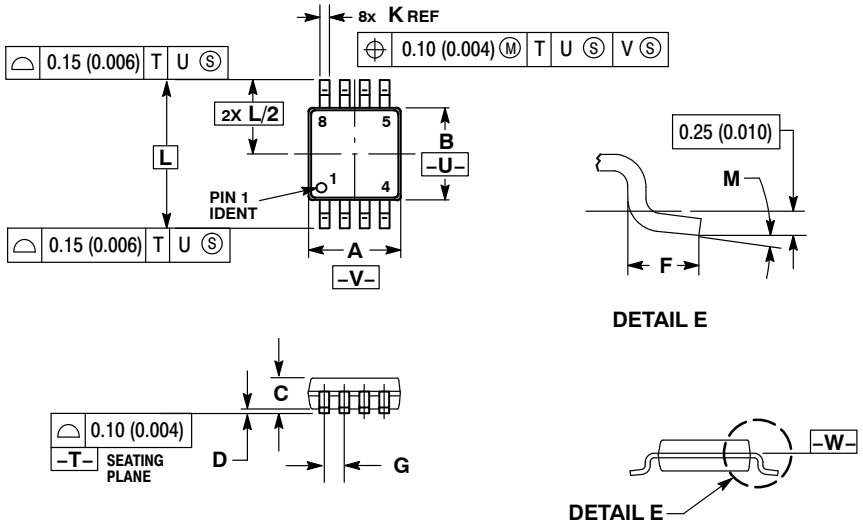



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**TSSOP−8**
**DT SUFFIX**
PLASTIC TSSOP PACKAGE
CASE 948R−02
ISSUE A

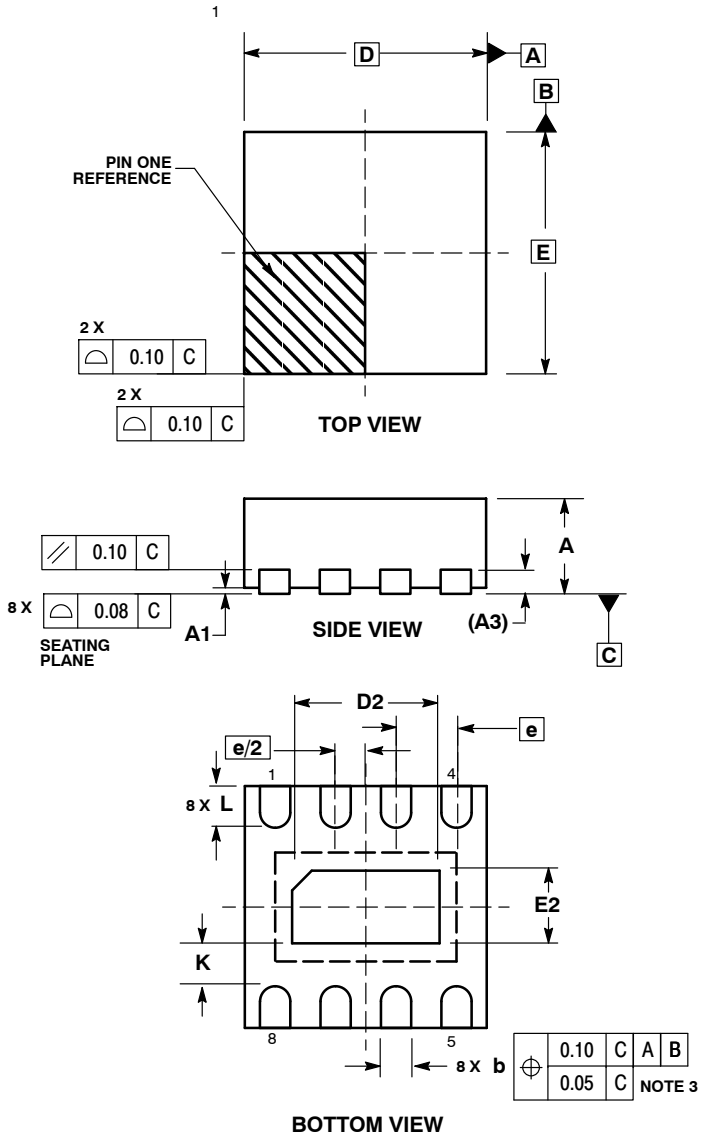



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0 ° | 6 ° | 0 ° | 6 ° |

## PACKAGE DIMENSIONS

**DFN8**
CASE 506AA−01
ISSUE D




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.10 | 1.30 |
| E | 2.00 BSC | |
| E2 | 0.70 | 0.90 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.25 | 0.35 |

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).



## PUBLICATION ORDERING INFORMATION

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