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HD74SSTV16857

1:1 14-bit SSTL 2 Registered Buffer

REJ03D0830-0700

(Previous: ADE-205-336F)

Rev.7.00 Apr 07, 2006

Description

The HD74SSTV16857 is a 14-bit registered buffer designed for 2.3 V to 2.7 V Vcc operation and LVCMOS reset (RESET) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to Q is controlled by differential clock pins (CLK, \overline{CLK}) and the \overline{RESET} . Data is triggered on the positive edge of the positive clock (CLK), and the negative clock (\overline{CLK}) must be used to maintain noise margins. When \overline{RESET} is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

Features

- Supports LVCMOS reset (RESET) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV16857TEL	TSSOP-48 pin	PTSP0048KA-A (TTP-48DBV)	Ţ	EL (1,000 pcs / Reel)
HD74SSTV16857NEL		PTSP0048LA-A (TTP-48DEV)	N	EL (1,000 pcs / Reel)

Note: Please consult the sales office for the above package availability.

Function Table

	Output O			
RESET	CLK	CLK	D	Output Q
L	X	X	X	L
Н	1	↑	Н	Н
Н	↓	↑	L	L
Н	L or H	H or L	Х	Q ₀ *1

H: High level

L: Low level

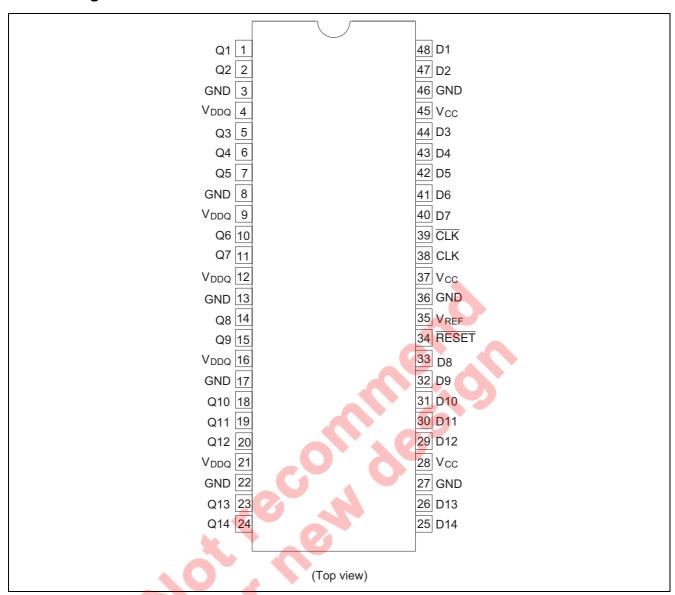
X: Immaterial

1: Low to high transition

 \downarrow : High to low transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC} or V _{DDQ}	-0.5 to 3.6	V	
Input voltage *1	Vı	-0.5 to V _{DDQ} +0.5	V	
Output voltage *1, 2	Vo	-0.5 to V _{DDQ} +0.5	V	
Input clamp current	I _{IK}	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I _{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	Io	±50	mA	$V_O = 0$ to V_{DDQ}
V _{CC} , V _{DDQ} or GND current / pin	I_{CC} , I_{DDQ} or I_{GND}	±100	mA	
Maximum power dissipation	P _T	115	°C / W	TSSOP
at Ta = 55°C (in still air)				
Storage temperature	Tstg	-65 to +150	°C	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

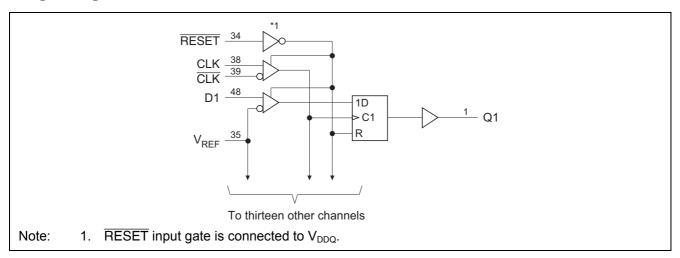
- 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 2. This current will flow only when the output is in the high state and $V_0 > V_{DDQ}$.

Recommended Operating Conditions

	Item	Symbol	Min	Тур	Max	Unit	Conditions
Supply voltage		Vcc	V _{DDQ}	2.5	2.7	V	
Output supply	voltage	V_{DDQ}	2.3	2.5	2.7	V	
Reference vol	tage	V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination vo	oltage	V_{TT}	V _{REF} -40 mV	V _{REF}	V _{REF} +40 mV	V	
Input voltage		Vı	0		V _{CC}	V	
AC high level	input voltage	V _{IH}	V _{REF} +310 mV		_	V	D
AC low level input voltage		VIL		_	V _{REF} -310 mV	V	D
DC high level	DC high level input voltage		V _{REF} +150 mV	_	_	V	D
DC low level in	nput voltage	VIL		_	V _{REF} -150 mV	V	D
High level inpu	ut voltage	V _{IH}	1.7	_	V _{DDQ} +0.3	V	RESET
Low level inpu	t voltage	VIL	-0.3	_	0.7	V	RESET
Differential	(Common mode range)	V_{CMR}	0.97	_	1.53	V	CLK, CLK
input voltage	(Minimum peak to peak input)	V _{PP}	360	_	_	mV	CLK, CLK
High level output current		I _{OH}	_	_	-20	mA	
Low level output current		I _{OL}	_	_	20	mA	
Operating tem	perature	Та	0		70	°C	

Note: The $\overline{\text{RESET}}$ input of the device must be held at V_{DDQ} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.

Logic Diagram



Electrical Characteristics

Ite	m	Symbol	V _{cc} (V)	Min	Тур	Max	Unit	Test Conditions
Input diode volta	age	V _{IK}	2.3	_	_	-1.2	V	I _{IN} = -18 mA
Output voltage		V _{OH}	2.3 to 2.7	V _{CC} -0.2	_		V	I _{OH} = –100 μA
			2.3	1.95		V_{DDQ}		I _{OH} = –16 mA
		V _{OL}	2.3 to 2.7	_		0.2		I _{OL} = 100 μA
			2.3	0		0.35		I _{OL} = 16 mA
Input current	(All inputs)	I _{IN}	2.7	-	_	±5	μΑ	V _{IN} = 2.7 V or 0
Quiescent suppl	y current	Icc *2	2.7		_ (45	mA	$V_{IN} = V_{IH(AC)}$ or $V_{IL(AC)}$, $I_O =$
								0
Standby current		I _{CC (stdy)}	2.7	_		10	μΑ	RESET = GND
Dynamic operati	ing clock only	I _{CCD} *2	2.7		_	90	μΑ/	$\overline{RESET} = V_{CC},$
							clock	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$,
							MHz	CLK and CLK switching 50%
								duty cycle
Dynamic operati	ing per each	I _{CCD} *2	2.7			15	μΑ/	$\overline{RESET} = V_{CC},$
data input				*			clock	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$,
							MHz/	CLK and CLK switching 50%
							data	duty cycle. One data input
							input	switching at half clock
								frequency, 50% duty cycle.
Output high *3		r_{OH}	2.3 to 2.7	7	_	22 *4	Ω	$I_{OH} = -20 \text{ mA}$
Output low *3		r_{OL}	2.3 to 2.7	7		22 *4	Ω	I _{OL} = 20 mA
r _{OH} - r _{OL} each	separate bit *3	$r_{O(\Delta)}$	2.5	_	_	4	Ω	I _O = 20 mA, Ta = 25°C
Input	Data inputs	C _{IN}	2.5 *1	2.5	_	3.5	pF	V _I = V _{REF} ±310 mV
capacitance	CLK and CLK			2.5		3.5		V _{CMR} = 1.25 V, V _{PP} = 360 mV
	RESET			_	3.0			V _I = V _{CC} or GND

Notes: 1. All typical values are at $V_{CC} = 2.5 \text{ V}$, Ta = 25°C.

- 2. Total I_{CC} (max) = I_{CC} + { I_{CCD} (clock)×f(clock)} + { I_{CCD} (Data)×1/2f(clock)×14}
- 3. This is effective in the case that it did terminate by resistance.
- 4. See figure. 1, 2

Switching Characteristics

Item		Symbol	$V_{CC} = 2$.	$V_{CC} = 2.5 \pm 0.2 \text{ V}$		Test Condition
		Syllibol	Min	Max	Unit	rest Condition
Clock frequency	*1	f_{clock}	_	200	MHz	
Setup time	Fast slew rate *4, 6	t_{su}	0.75	_	ns	Data before CLK↑, CLK↓
	Slow slew rate *5, 6		0.9	_		
Hold time	Fast slew rate *4, 6	t _h	0.75	_	ns	Data after CLK↑, CLK↓
	Slow slew rate *5, 6		0.9	_		
Differential inputs active time		t _{act}	22	_	ns	Data inputs must be low after RESET high.
Differential inputs inactive time		t _{inact}	22	_	ns	Data and clock inputs must be held at valid levels (not floating) after RESET low.
Pulse width		t _w	2.5	_	ns	CLK, CLK "H" or "L"
Output slew *3		t _{SL}	1	4	volt/ns	

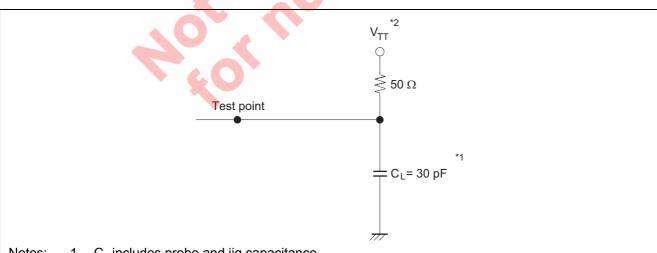
$$(C_L = 30 \text{ pF}, R_L = 50 \Omega, V_{REF} = V_{TT} = V_{DDO} \times 0.5)$$

Item	Symbol	$V_{CC} = 2.5 \pm 0.2 \text{ V}$			Unit	FROM	ТО
item	Syllibol	Min	Тур	Max	Ollik	(Input)	(Output)
Maximum clock frequency	f _{max}	200	_	_	MHz		
Propagation delay time *2	t _{PLH} , t _{PHL}	1.1	_	2.8	ns	CLK, CLK	Q
	t _{PHL}	_	_	5.0		RESET	Q

Notes: 1. Although the clock is differential, all timing is relative to CLK going high and CLK going low.

- 2. This timing relationship is specified into test load (see waveforms 3, 4) with all of the outputs switching.
- 3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
- 4. For data signal input slew rate ≥ 1 V/ns.
- 5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
- 6. CLK, CLK signals input slew rates are ≥ 1 V/ns

Test Circuit



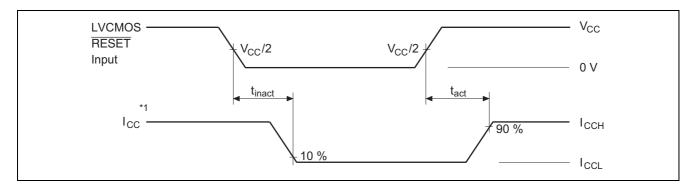
Notes: 1. C_L includes probe and jig capacitance.

2. $V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

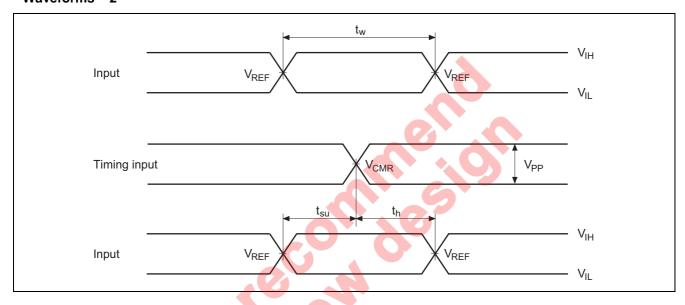
3. Input waveform : PRR \leq 10 MHz, Zo = 50 Ω ,

Input slew rate = 1 V/ns ±20% (unless otherwise noted.)

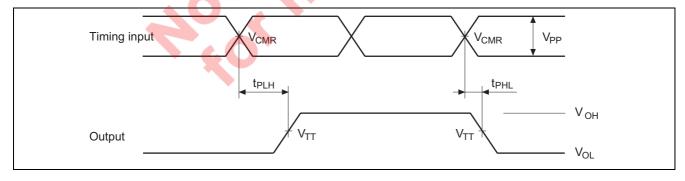
Waveforms - 1



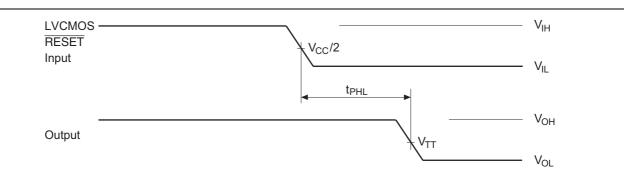
Waveforms - 2



Waveforms - 3



Waveforms - 4



Notes:

- 1. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
- 2. All input pulses are supplied by generators having the following characteristics : PRR \leq 10 MHz, Zo = 50 Ω , input slew rate = 1 V/ns \pm 20% (unless otherwise specified).
- 3. The outputs are measured one at a time with one transition per measurement.

- 4. $V_{TT} = V_{REF} = V_{DDQ}/2$
- 5. $V_{IH} = V_{REF} + 310 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
- 6. $V_{IL} = V_{REF}$ -310 mV (AC voltage levels) for differential inputs. $V_{IL} = GND$ for LVCMOS input.
- 7. t_{PLH} and t_{PHL} are the same as t_{pd}

Application Data

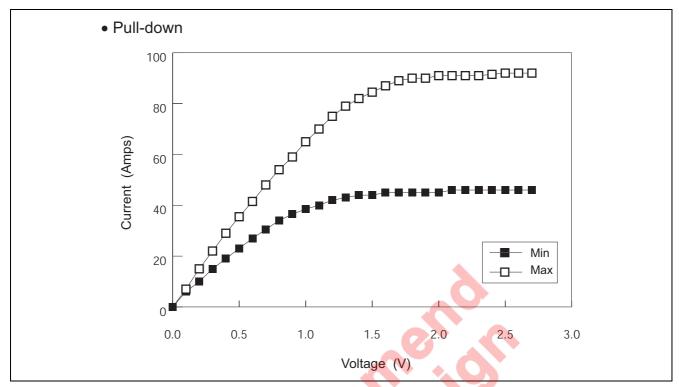


Figure . 1

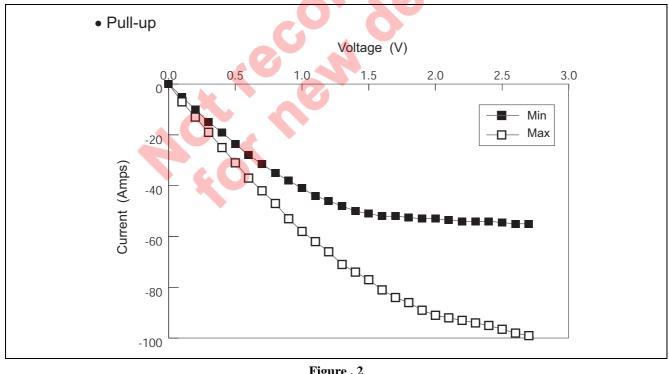
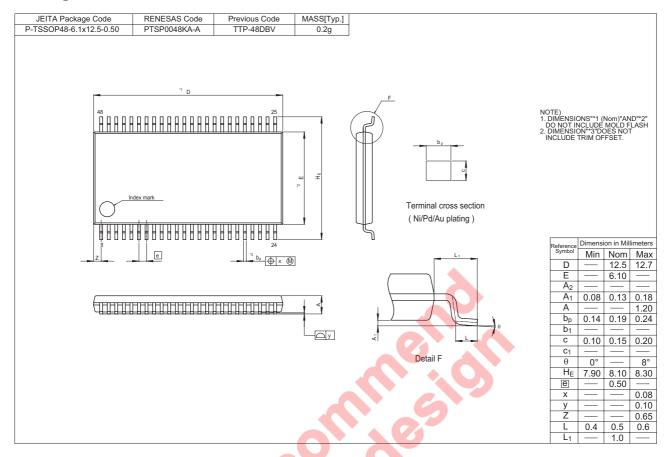


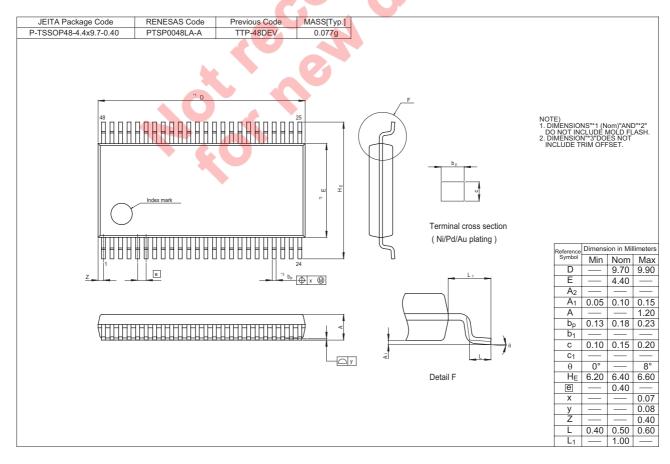
Figure . 2

Curve Data

	Pull-o	down	Pull-up		
Voltage (V)	I (mA)	I (mA)	I (mA)	I (mA)	
	Min	Max	Min	Max	
0.0	0	0	0	0	
0.1	6	7	-5	-7	
0.2	10	15	-10	-13	
0.3	15	22	-15	-19	
0.4	19	29	-19	-25	
0.5	23	35.5	-23.5	-31	
0.6	27	41.5	-28	-37	
0.7	30.5	48	-31.5	-42	
0.8	34	54	-35	-47	
0.9	36.5	59	-38	-53	
1.0	38.5	65	-4 1	-58	
1.1	40	70	-4 4	-62	
1.2	42	75	-46	-66	
1.3	43	79	-48	– 71	
1.4	44	82	-50	-74	
1.5	44	84.5	–51	–77	
1.6	45	87	-52	– 81	
1.7	45	89	-52	-84	
1.8	45	90	-52.5	-86	
1.9	45	90	-53	-89	
2.0	45	91	-53	– 91	
2.1	46	91	-53.5	– 92	
2.2	46	91	– 54	– 93	
2.3	46	91	– 54	-94	
2.4	46	91.5	– 54	– 95	
2.5	46	92	-54.5	-96.5	
2.6	46	92	– 55	– 98	
2.7	46	92	– 55	-99	

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