DATASHEET

14-BIT CONFIGURABLE REGISTERED BUFFER FOR DDR2

ICSSSTUAF32869A

Description

The ICSSSTUAF32869A is 14-bit 1:2 registered buffer with parity, designed for 1.7 V to 1.9 V VDD operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8V CMOS drivers optimized to drive the DDR2 DIMM load. They provide 50% more dynamic driver strength than the standard SSTU32864 outputs.

The ICSSSTUAF32869A operates from a differential clock (CLK and $\overline{CLK}$). Data are registered at the crossing of CLK going high, and $\overline{CLK}$ going low.

The device supports low-power standby operation. When the reset input ($\overline{RESET}$) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when $\overline{RESET}$ is low all registers are reset, and all outputs except $\overline{PTYERR}$ are forced low. The LVCMOS $\overline{RESET}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CLK and $\overline{CLK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. ICSSSTUAF32869A must ensure that the outputs remain low as long as the data inputs are low, the clock is stable during the time from the low-to-high transition of $\overline{RESET}$ and the input receivers are fully enabled. This will ensures that there are no glitches on the output.

The device monitors both $\overline{DCS}$ and $\overline{CSR}$ inputs and will gate the Qn, PPO (Paritial-Parity-Out) and $\overline{PTYERR}$ (Parity Error) Parity outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ are high. If either $\overline{DCS}$ and $\overline{CSR}$ input is low, the Qn, PPO and $\overline{PTYERR}$ outputs will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ controls and will force the Qn and PPO outputs low and the $\overline{PTYERR}$ high.

The ICSSSTUAF32869A includes a parity checking function. The ICSSSTUAF32869A accepts a parity bit from the memory controller at its input pin PARIN one or two cycles after the corresponding data input, compares it with the data received on the D-inputs and indicates on its opendrain $\overline{PTYERR}$ pin (active low) whether a parity error has occurred. The number of cycles depends on the setting of C1.

When used as a single device, the C1 input is tied low. When used in pairs, the C1 inputs is tied low for the first register (front) and the C1 input is tied high for the second register. When used as a single register, the PPO and $\overline{PTYERR}$ signals are produced two clock cycles after the corresponding data input. When used in pairs, the $\overline{PTYERR}$ signals of the first register are left floating. The PPO outputs of the first register are cascaded to the PARIN signas on the second register (back). The PPO and $\overline{PTYERR}$ signals of the second register are produced three clock cycles after the corresponding data input. Parity implimentation and device wiring for single and dual die is described in the diagram below.

If an error occurs, and the $\overline{PTYERR}$ is driven low, it stays low for two clock cycles or until $\overline{RESET}$ is driven low. The DIMM-dependent signals (DCKE, DCS, CSR and DODT) are not included in the parity check computations.

All registers used on an individual DIMM must be of the same configuration, i.e single or dual die.

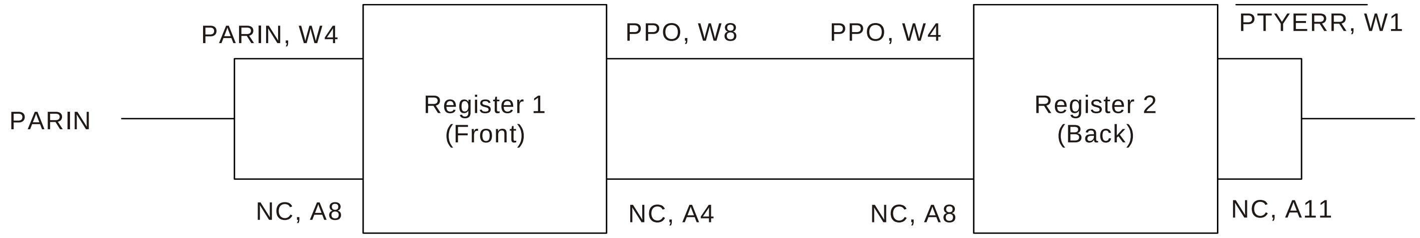
Features

- 14-bit 1:2 registered buffer with parity check functionality
- Supports SSTL_18 JEDEC specification on data inputs and outputs
- 50% more dynamic driver strength than standard SSTU32864
- Supports LVCMOS switching levels on C1 and $\overline{RESET}$ inputs
- Low voltage operation: VDD = 1.7V to 1.9V
- Available in 150 BGA package

Applications

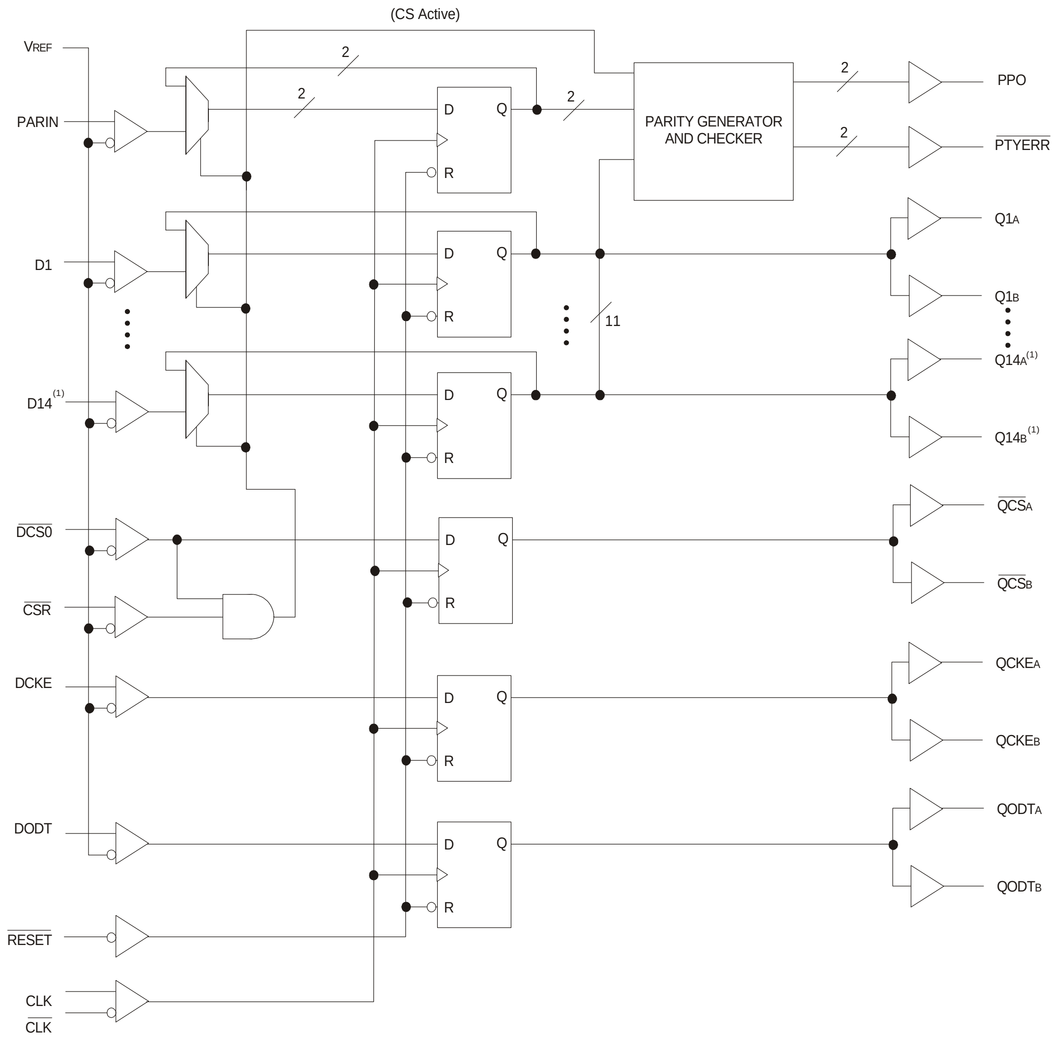
- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS98ULPA877A or IDTCSPUA877A
- Ideal for DDR2 400, 533, and 667

Parity Implementation and Device Wiring



Set C=0 for Register 1, and C=1 for Register 2

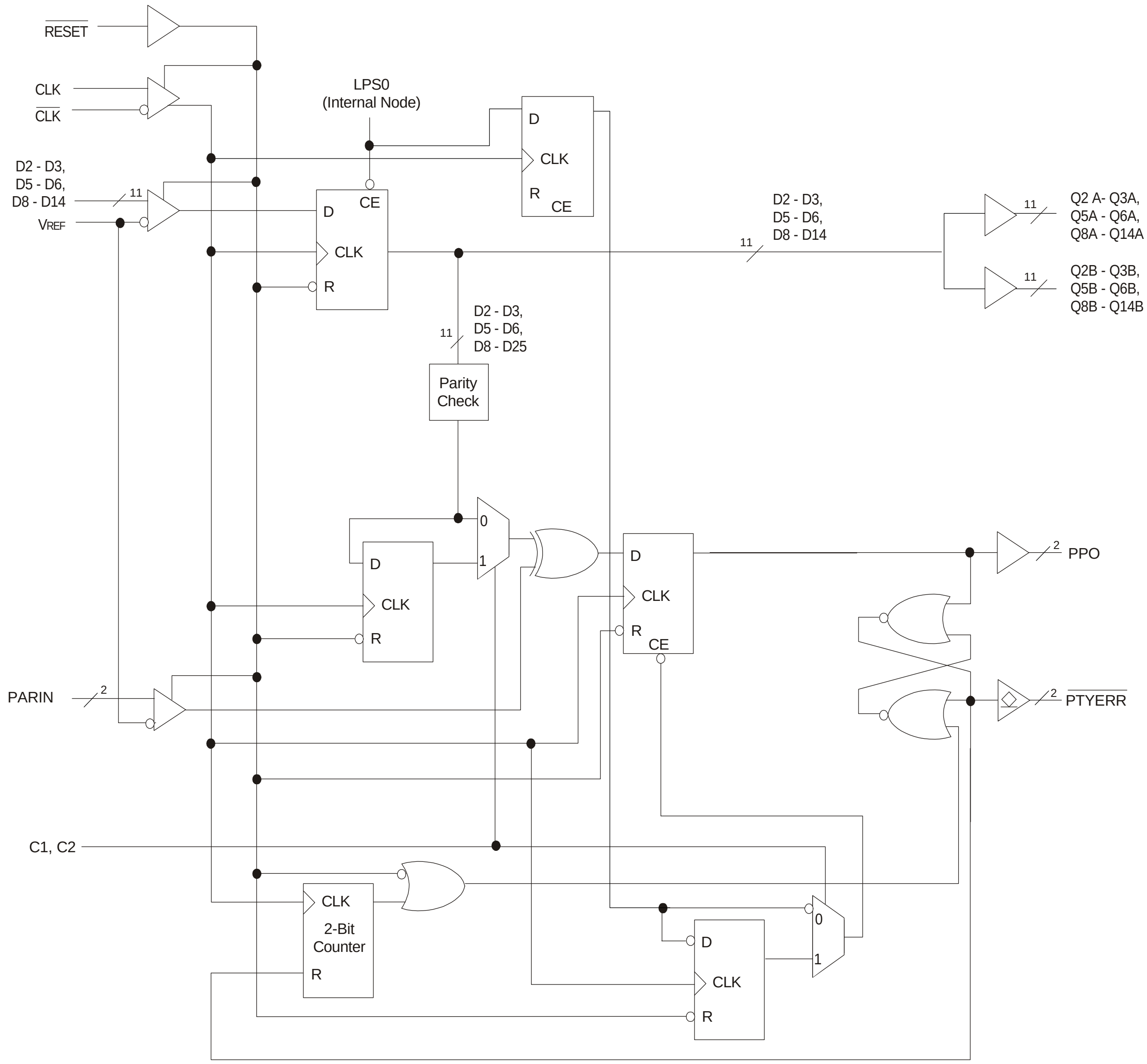
Block Diagram



NOTE:

1.This range does not include D1, D4, and D7, and their corresponding outputs.

Block Diagram



NOTE:

1.PARIN is used to generate PPO and $\overline{\text{PTYERR}}$.

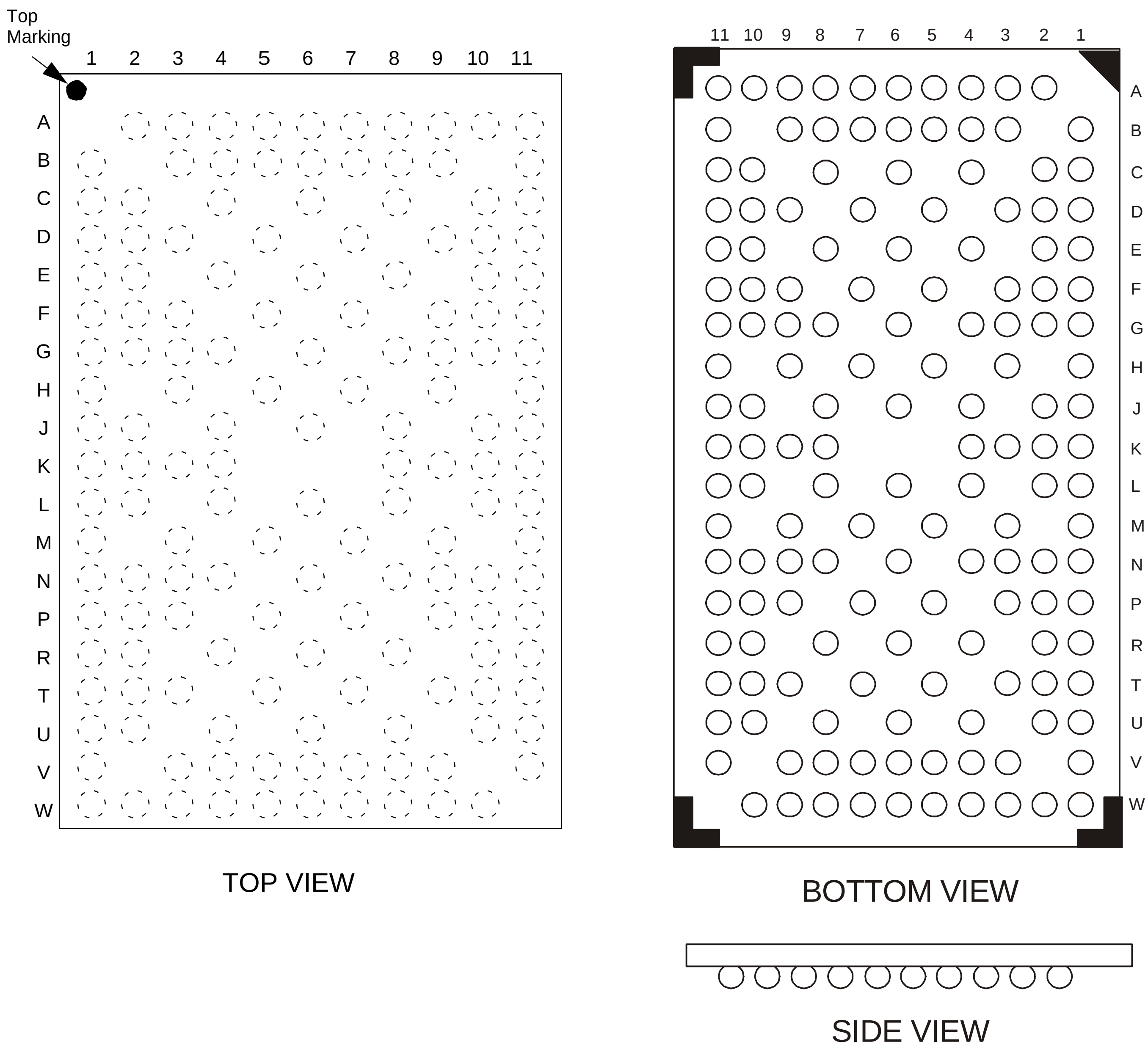
Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11
A	NB	VDD	MCL(1)	NC	GND	VREF	GND	NC	MCL(1)	VDD	NC
B	VDD	NB	VDD	GND	GND	GND	GND	GND	VDD	NB	VDD
C	QCKEA	VDD	NB	GND	NB	GND	NB	GND	NB	VDD	QCKEB
D	Q2A	VDD	GND	NB	DCKE	NB	D2	NB	GND	VDD	Q2B
E	Q3A	VDD	NB	D3	NB	NC	NB	DODT	NB	C1	Q3B
F	QODTA	VDD	GND	NB	NC	NB	NC	NB	GND	VDD	QODTB
G	Q5A	VDD	GND	D5	NB	CLK	NB	D6	GND	VDD	Q5B
H	Q6A	NB	GND	NB	NC	NB	NC	NB	GND	NB	Q6B
J	$\overline{QCSA}$	VDD	NB	NC	NB	$\overline{RESET}$	NB	$\overline{CSR}$	NB	VDD	$\overline{QCSB}$
K	VDD	VDD	GND	GND	NB	NB	NB	GND	VDD	VDD	VDD
L	Q8A	VDD	NB	$\overline{DCS}$	NB	$\overline{CLK}$	NB	D8	NB	VDD	Q8B
M	Q9A	NB	GND	NB	NC	NB	NC	NB	GND	NB	Q9B
N	Q10A	VDD	GND	D9	NB	NC	NB	D10	GND	VDD	Q10B
P	Q11A	VDD	GND	NB	NC	NB	NC	NB	GND	VDD	Q11B
R	Q12A	C1	NB	D11	NB	NC	NB	D12	NB	VDD	Q12B
T	Q13A	VDD	GND	NB	D13	NB	D14	NB	GND	VDD	Q13B
U	Q14A	VDD	NB	GND	NB	GND	NB	GND	NB	VDD	Q14B
V	VDD	NB	VDD	GND	GND	GND	GND	GND	VDD	NB	VDD
W	$\overline{PTYERR}$	VDD	MCL(1)	PARIN	GND	VREF	GND	PPO	MCL(1)	VDD	NB

150-Ball BGA
TOP VIEW

NOTE:
1.NC denotes a no-connect (ball present but not connected to the die). NB indicates no ball is populated at that gridpoint.

150 Ball CTBGA Package Attributes



Function Table

Inputs[1]						Outputs		
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CLK	$\overline{CLK}$	Dn, DODT, DCKE	Qn	$\overline{QCS}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]
H	H	H	↑	↓	L	Q_0[2]	H	L
H	H	H	↑	↓	H	Q_0[2]	H	H
H	H	H	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L

1 H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW to HIGH
↓ = HIGH to LOW

2 Output Level before the indicated steady-state conditions were established.

Terminal Functions

Signal Group	Terminal Name	Type	Description
Ungated Inputs	DCKE, DODT	SSTL_18	DRAM function pins not associated with Chip Select
Chip Select Gated Inputs	D1...D14[1]	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW
Chip Select Inputs	DCS, CSR	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be LOW when a valid address/command is present.
Re-Driven Outputs	Q1A...Q14A[1], Q1B...Q14B[1], QCSnA, B QCKEnA, B QODTnA, B	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock
Parity Input	PARIN	SSTL_18	Input parity is received on pin PARIN, and should maintain odd parity across the D1:D14 inputs, at the rising edge of the clock, one cycle after Chip Select is LOW.
Parity Output	PPO	SSTL_18	Partial Parity Output. Indicates parity out of D1-D14.
Parity Error Output	PTYERR	Open Drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. PTYERR will be active for two clock cycles, and delayed by in total two clock cycles for compatibility with final parity out timing on the industry-standard DDR2 register with parity (in JEDEC definition).
Configuration Inputs	C1	SSTL_18	When LOW, the register is configured as Register 1. When HIGH, the register is configured as Register 2.
Clock Inputs	CLK, CLK	SSTL_18	Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CLK).
Miscellaneous Inputs	RESET	SSTL_18 Input	Asynchronous Reset Input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. RESET also resets the PTYERR signal.
	VREF	0.9V nominal	Input reference voltage for SSTL_18 inputs. Two pins (internally tied together) are used for increased Inputsreliability.
	VDD	Power Input	Power Supply Voltage
	GND	Ground Input	Ground

1 This range does not include D1, D4, and D7, and their corresponding outputs.

Parity and Standby Function Table

Inputs[1]							Outputs	
$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CLK	$\overline{\text{CLK}}$	Σ of Inputs = H (D1 - D14)[2]	PARIN[3]	PPO	$\overline{\text{PTYERR}}$[4]
H	L	X	↑	↓	Even	L	L	H
H	L	X	↑	↓	Odd	L	H	L
H	L	X	↑	↓	Even	H	H	L
H	L	X	↑	↓	Odd	H	L	H
H	L	L	↑	↓	Even	L	L	H
H	L	L	↑	↓	Odd	L	H	L
H	L	L	↑	↓	Even	H	H	L
H	L	L	↑	↓	Odd	H	L	H
H	H	H	↑	↓	X	X	$PPOn_0$	$\overline{\text{PTYERRn}}_0$
H	X	X	L or H	L or H	X	X	$PPOn_0$	$\overline{\text{PTYERRn}}_0$
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	H

1 H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW to HIGH
↓ = HIGH to LOW

2 This range does not include D1, D4, and D7.

3 PARIN arrives one clock cycle (C1 = 0), or two clock cycles (C1 = 1), after the data to which it applies.

4 This transition assumes $\overline{\text{PTYERR}}$ is HIGH at the crossing of CLK going HIGH and $\overline{\text{CLK}}$ going LOW. If $\overline{\text{PTYERR}}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{\text{RESET}}$ is driven LOW. PARIN is used to generate PPO and $\overline{\text{PTYERR}}$.

Absolute Maximum Ratings

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Item		Rating
Supply Voltage, V_{DD}		-0.5V to 2.5V
Input Voltage Range, V_I[1]		-0.5V to V_{DD} + 2.5V
Output Voltage Range, V_O[1,2]		-0.5V to V_{DDQ} + 0.5V
Input Clamp Current, I_{IK}		±50mA
Output Clamp Current, I_{OK}		±50mA
Continuous Output Clamp Current, I_O		±50mA
Continuous Current through each V_{DD} or GND		±100mA
Package Thermal Impedance (θja)[3]	0m/s Airflow	40° C/W
	1m/s Airflow	29° C/W
Storage Temperature		-65 to +150° C

1 The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
2 This current will flow only when the output is in the high state level $V_O > V_{DDQ}$.
3 The package thermal impedance is calculated in accordance with JESD 51.

Mode Select

C1	Device Mode
0	First device in pair, Front
1	Second device in pair, Back

Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range

Parameter	V_{DD} = 1.8V ± 0.1V		Units
	Min.	Max.	
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	V/ns
dV/dt_Δ[1]		1	V/ns

1 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

Operating Characteristics, T_A = 25° C

The $\overline{RESET}$ and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is LOW.

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{DD}	I/O Supply Voltage		1.7	1.8	1.9	V
V_{REF}	Reference Voltage		0.49 * V_{DD}	0.5 * V_{DD}	0.51 * V_{DD}	V
V_{TT}	Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_I	Input Voltage		0		V_{DD}	V
V_{IH}	AC High-Level Input Voltage	Dn, PARIN, $\overline{DCS}$, $\overline{CSR}$, DCKEn, DODTn	V_{REF} + 0.25			V
V_{IL}	AC Low-Level Input Voltage				V_{REF} - 0.25	
V_{IH}	DC High-Level Input Voltage		V_{REF} + 0.125			
V_{IL}	DC Low-Level Input Voltage				V_{REF} - 0.125	
V_{IH}	High-Level Input Voltage	$\overline{RESET}$, C1	0.65 * V_{DDQ}			V
V_{IL}	Low-Level Input Voltage				0.35 * V_{DDQ}	
V_{ICR}	Common Mode Input Range	CLK, $\overline{CLK}$	0.675		1.125	V
V_{ID}	Differential Input Voltage		600			mV
I_{OH}	High-Level Output Current				-12	mA
I_{OL}	Low-Level Output Current				12	
I_{ERROL}	$\overline{PTYERR}$ Low-Level Output Current		25			mA
T_A	Operating Free-Air Temperature		0		+70	°C

DC Electrical Characteristics Over Operating Range

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = 0°C to +70°C, V_{DDQ}/V_{DD} = 1.8V ± 0.1V.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IK}		I_I = -18mA			-1.2	V
V_{OH}		V_{DDQ} = 1.7V, I_{OH} = -100µA	V_{DDQ}-0.2			V
		V_{DDQ} = 1.7V, I_{OH} = -12mA	1.2			
V_{OL}		V_{DDQ} = 1.7V, I_{OL} = 100µA			0.2	V
		V_{DDQ} = 1.7V, I_{OL} = 12mA			0.5	
V_{ERROL}	$\overline{PTYERR}$ Output Low Voltage	I_{ERROL} = 25mA; V_{DD} = 1.7V			0.5	V
I_{IL}	All Inputs	V_I = V_{DD} or GND	-5		+5	µA
I_{DD}	Static Standby	I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = GND			200	µA
	Static Operating	I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK = $\overline{CLK}$ = $V_{IH(AC)}$ or $V_{IL(AC)}$			10	mA
		I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK = $V_{IH(AC)}$, $\overline{CLK}$ = $V_{IL(AC)}$		120		
I_{DDD}	Dynamic Operating (clock only)	I_O = 0, V_{DD} = 1.8V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle		247		µA/Clock MHz
	Dynamic Operating (per each data input)	I_O = 0, V_{DD} = 1.8V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.		52		µA/Clock MHz/ Data
C_{IN}	Dn, PARIN, $\overline{DSCn}$ inputs	V_I = V_{REF} ± 250mV	2		3	pF
	CLK and $\overline{CLK}$ inputs	V_{ICR} = 0.9V, V_{IPP} = 600mV	3.5		4.5	
	$\overline{RESET}$	V_I = V_{DD} or GND		5		

Timing Requirements Over Recommended Operating Free-Air Temperature Range

Symbol	Parameter		VDD = 1.8V ± 0.1V Min.	Max.	Units
fCLOCK	Clock Frequency			410	MHz
tW	Pulse Duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW		1		ns
tACT[1]	Differential Inputs Active Time			10	ns
tINACT[2]	Differential Inputs Inactive Time			15	ns
tSU	Setup Time	$\overline{\text{DCS}}$ before CLK↑ , $\overline{\text{CLK}}$↓, $\overline{\text{CSR}}$ HIGH; $\overline{\text{CSR}}$ before CLK↑ , $\overline{\text{CLK}}$↓, $\overline{\text{DCS}}$ HIGH	0.7		ns
		$\overline{\text{DCS}}$ before CLK↑ , $\overline{\text{CLK}}$↓, $\overline{\text{CSR}}$ LOW	0.5		
		DODT, DOCKE, and data before CLK↑ , $\overline{\text{CLK}}$↓	0.5		
		PAR_IN before CLK↑ , $\overline{\text{CLK}}$↓	0.5		
tH	Hold Time	$\overline{\text{DCS}}$, DODT, DCKE, and data after CLK↑ , $\overline{\text{CLK}}$↓	0.5		ns
		PAR_IN after CLK↑ , $\overline{\text{CLK}}$↓	0.5		

1 VREF must be held at a valid input voltage level and data inputs must be held at valid logic levels for a minimum time of tACT(max) after $\overline{\text{RESET}}$ is taken HIGH.
2 VREF, data, and clock inputs must be held at a valid input voltage levels (not floating) for a minimum time of tINACT(max) after $\overline{\text{RESET}}$ is taken LOW.

Switching Characteristics Over Recommended Free Air Operating Range (unless otherwise noted)

Symbol	Parameter	VDD = 1.8V ± 0.1V Min.	Max.	Units
fMAX	Max Input Clock Frequency	340		MHz
tPDM	Propagation Delay, single-bit switching, CLK↑ / $\overline{\text{CLK}}$↓to Qn	1.1	1.9	ns
tPDMSS	Propagation Delay, simultaneous switching, CLK↑ / $\overline{\text{CLK}}$↓to Qn		2	ns
tLH	LOW to HIGH Propagation Delay, CLK↑ / $\overline{\text{CLK}}$↓to $\overline{\text{PTYERR}}$	0.9	3	ns
tHL	HIGH to LOW Propagation Delay, CLK↑ / $\overline{\text{CLK}}$↓to $\overline{\text{PTYERR}}$	0.4	2.4	ns
tPD	Propagation Delay from CLK↑ / $\overline{\text{CLK}}$↓to PPO	0.3	1.6	ns
tPHL	HIGH to LOW Propagation Delay, $\overline{\text{RESET}}$↓to Qn↓		3	ns
tPLH	LOW to HIGH Propagation Delay, $\overline{\text{RESET}}$↓to $\overline{\text{PTYERR}}$↑		3	ns

Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range

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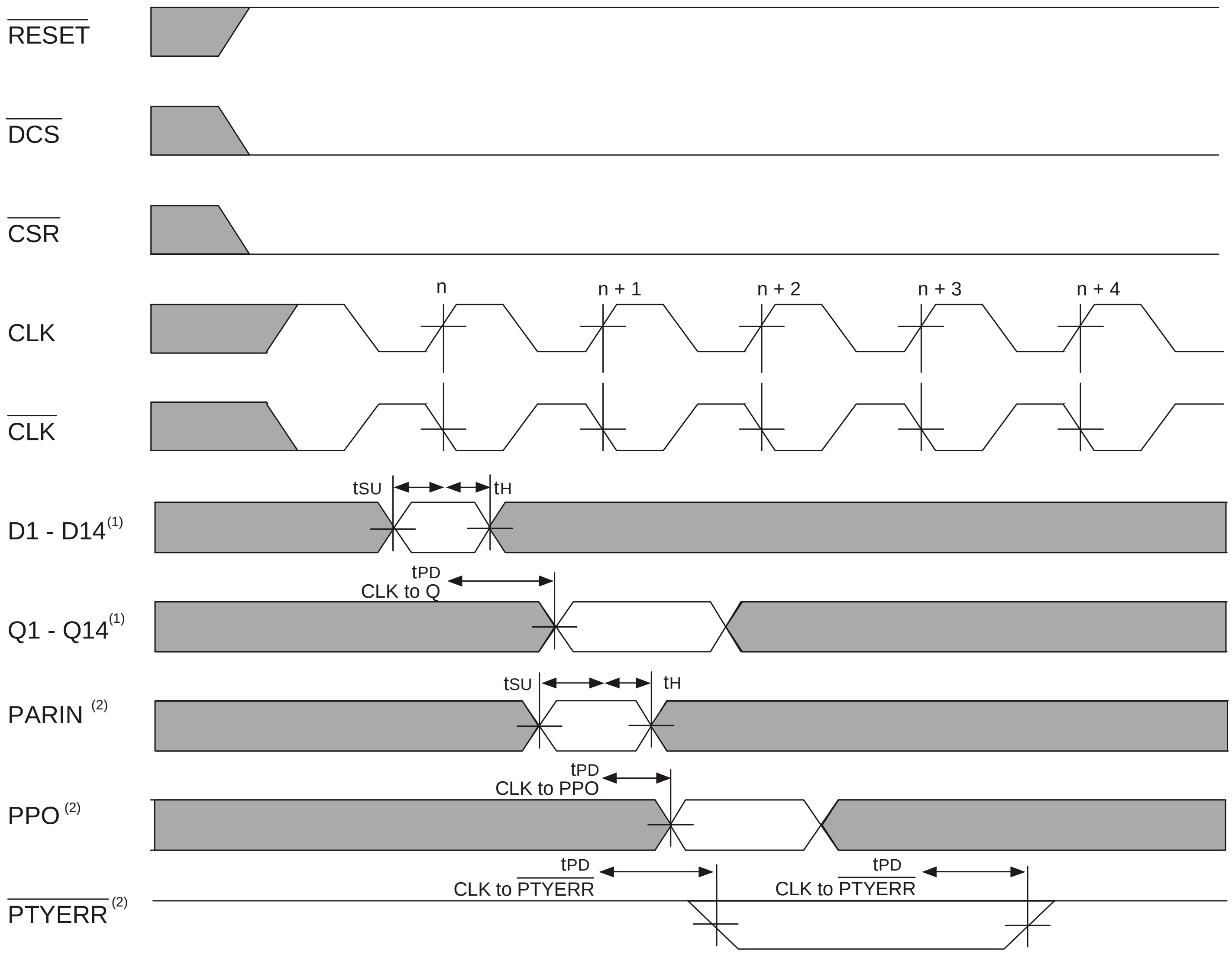
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	V/ns
dV/dt_Δ[1]		1	V/ns

1 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

Register Timing



NOTES:

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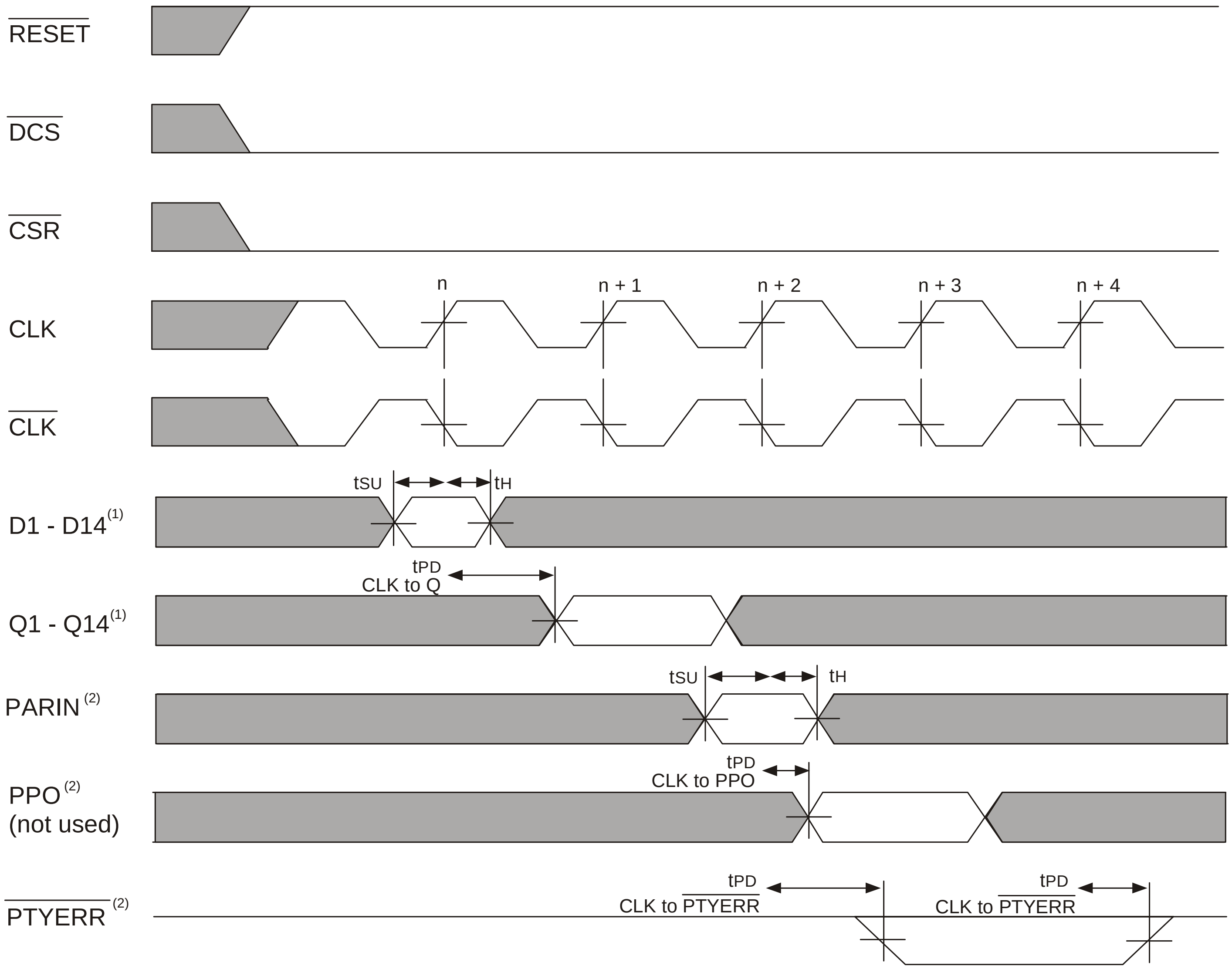
Register Timing



NOTES:

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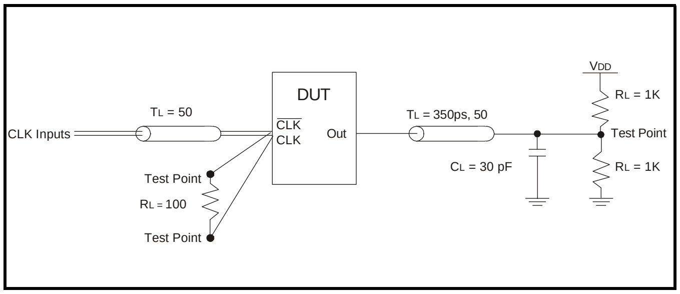
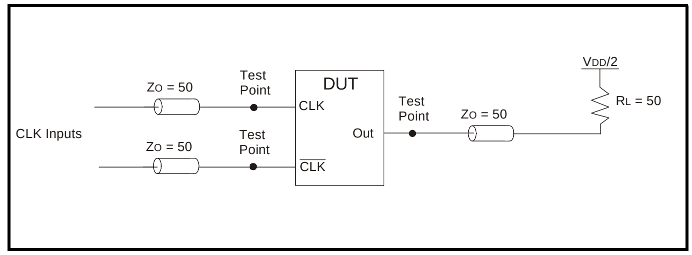
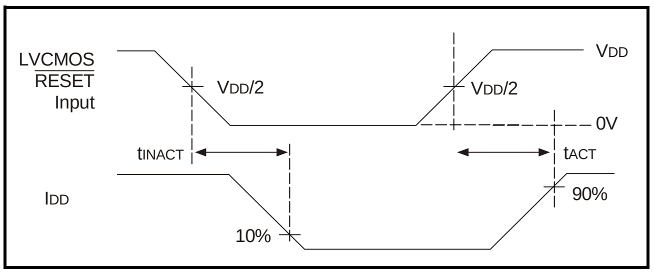
Test Circuits and Waveforms (V_{DD} = 1.8V ± 0.1V)



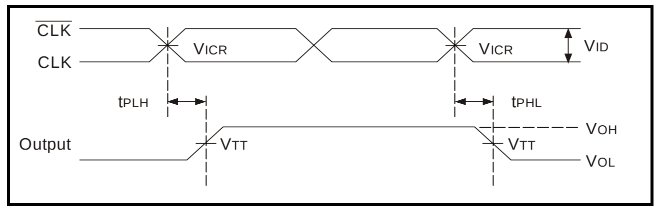
Simulation Load Circuit



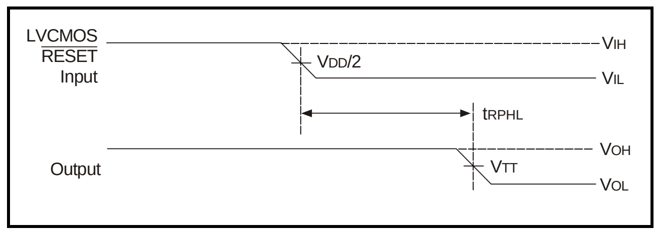
Production-Test Load Circuit



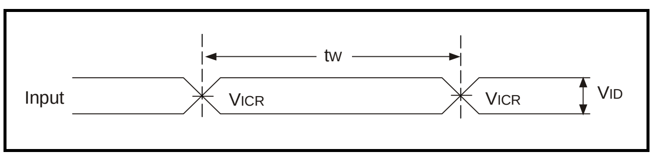
Voltage and Current Waveforms Inputs Active and Inactive Times



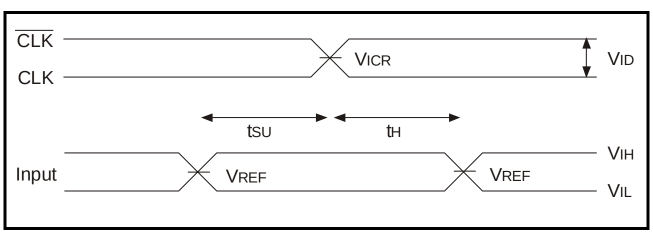
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Propagation Delay Times



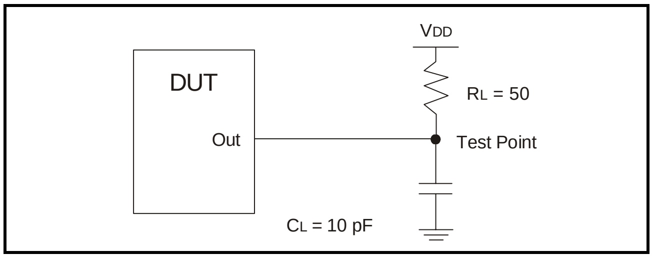
Voltage Waveforms - Pulse Duration



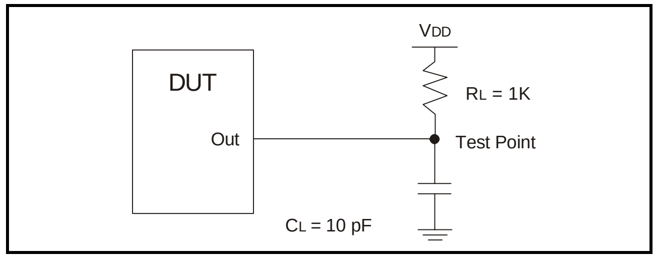
Voltage Waveforms - Setup and Hold Times

NOTES:
1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. V_{TT} = V_{REF} = V_{DD}/2
6. V_{IH} = V_{REF} + 250mV (AC voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.
7. V_{IL} = V_{REF} - 250mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. V_{ID} = 600mV.
9. t_{PLH} and t_{PHL} are the same as t_{PDM}.

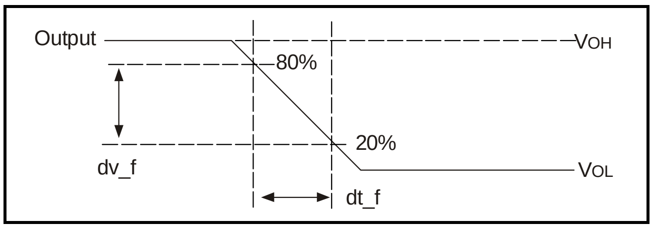
Test Circuits and Waveforms (V_{DD} = 1.8V ± 0.1V)



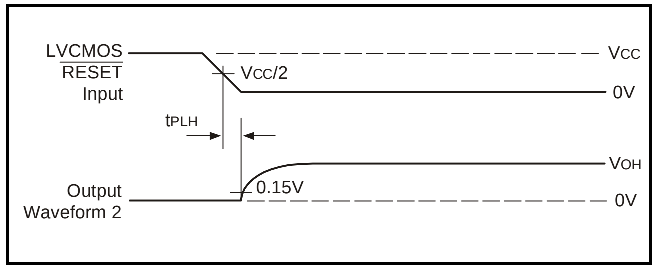
Load Circuit: High-to-Low Slew-Rate Adjustment



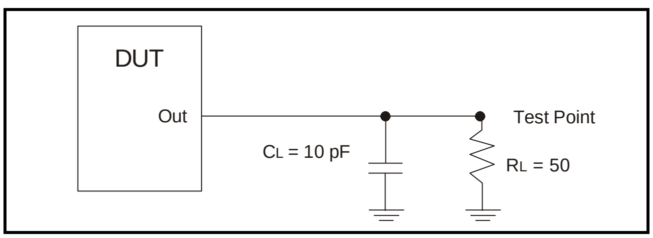
Load Circuit: Error Output Measurements



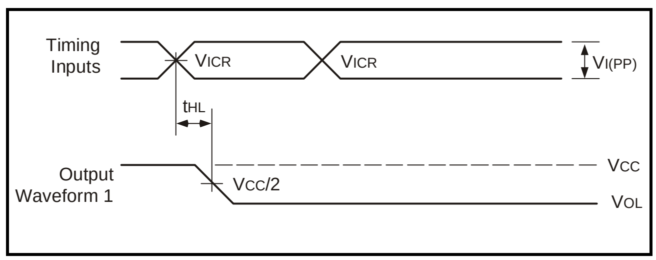
Voltage Waveforms: High-to-Low Slew-Rate Adjustment



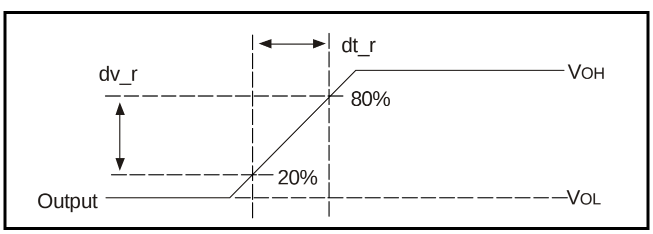
Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with respect to RESET input)



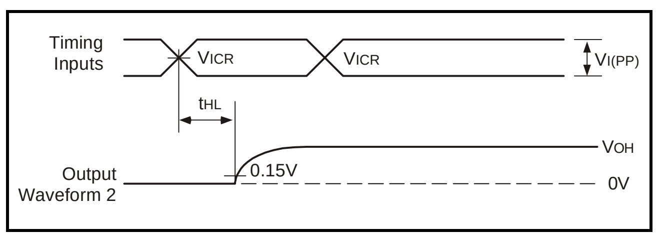
Load Circuit: Low-to-High Slew-Rate Adjustment



Voltage Waveforms: Open Drain Output High-to-Low Transition Time (with respect to clock inputs)



Voltage Waveforms: Low-to-High Slew-Rate Adjustment

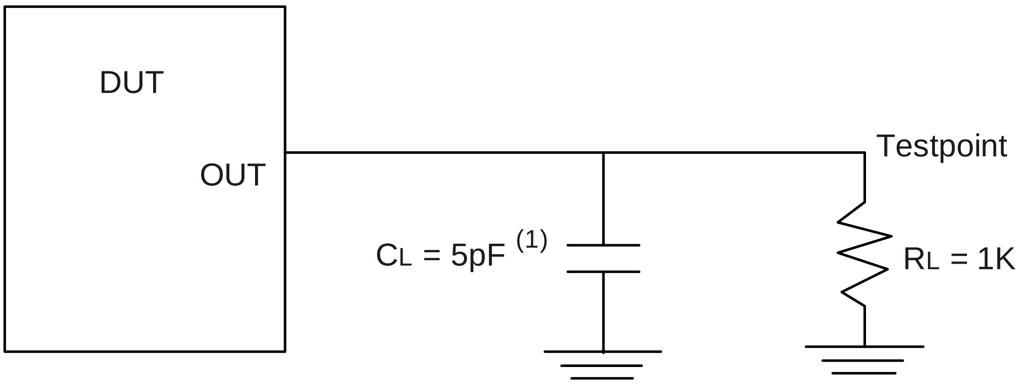


Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with respect to clock inputs)

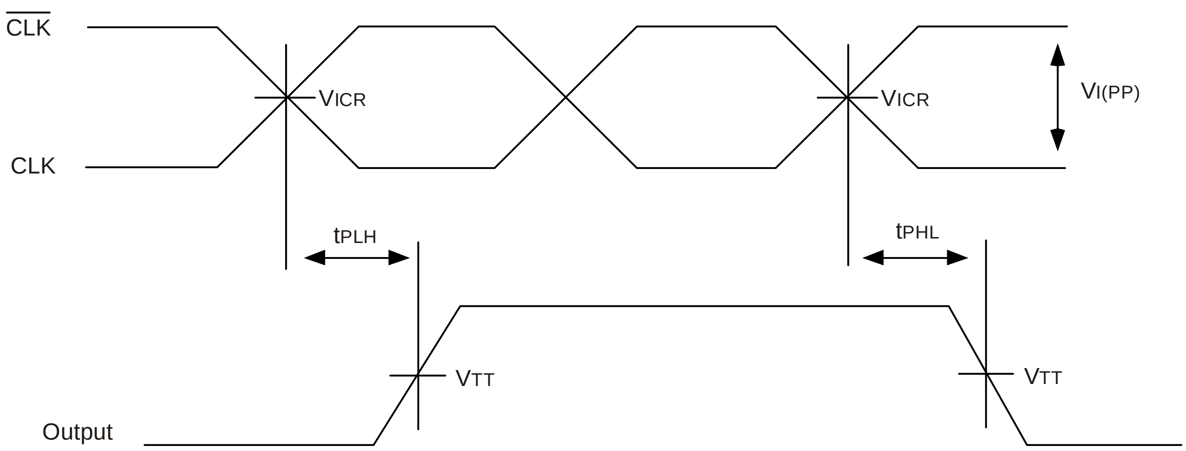
NOTES:

1. CL includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

Test Circuits and Waveforms (V_{DD} = 1.8V ± 0.1V)



Partial Parity Out Load Circuit



Partial Parity Out Voltage Waveform, Propagation Delay Time with Respect to CLK Input

$V_{TT} = V_{TT}/2$

V_{ICR} Cross Point Voltage

$V_{I(PP)}$ = 600mV

t_{PLH} and t_{PHL} are the same as t_{PD}.

Ordering Information

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