FAIRCHILD SEMICONDUCTOR™

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# FSTUD16450
# Configurable 4-Bit to 20-Bit Bus Switch with -2V Undershoot Protection and Selectable Level Shifting

## General Description

The Fairchild Universal Bus Switch FSTUD16450 provides 4-bit, 5-bit, 8-bit, 10-bit, 16-bit, 20-bit of high-speed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The FSTUD16450 is designed to allow "customer" configuration control of the enable connections. The device is organized as either a 4-bit, 5-bit, 10-bit or 20-bit bus switch. 8-bit and 16-bit configurations are also achievable (see Functional Description). The device's bit configuration is chosen through select pin logic. (see Truth Table). When $\overline{OE}_x$ is LOW, Port $A_x$ is connected to Port $B_x$. When $\overline{OE}_x$ is HIGH, the switch is OPEN.

The A and B Ports are "undershoot hardened" with UHC™ protection to support an extended range to 2.0V below ground. Fairchild's integrated "Undershoot Hardened Circuit" (UHC) senses undershoot at the I/O's, and responds by preventing voltage differentials from developing and turning on the switch.

Another key device feature is the addition of a level shifting select pin, "$S_2$". When $S_2$ is LOW, the device behaves as a standard N-MOS switch. When $S_2$ is HIGH, a diode to $V_{CC}$ is integrated into the circuit allowing for level shifting between 5V inputs and 3.3V outputs.

## Features

- Undershoot hardened to −2V (A and B Ports)
- Voltage level shifting
- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low $I_{CC}$
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- See Applications Note AN-5008 for details
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

## Applications Note

Select pins $S_0$, $S_1$, $S_2$ are intended to be used as static user configurable control pins. The AC performance of these pins has not been characterized or tested. Switching of these select pins during system operation may temporarily disrupt output logic states and/or enable pin controls.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| FSTUD16450GX (Note 1) | BGA54A (Preliminary) | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel] |
| FSTUD16450MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

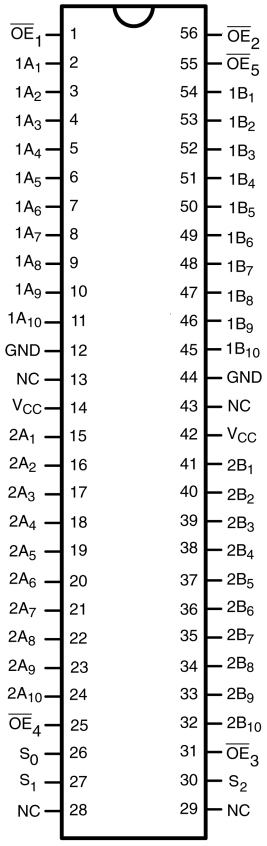
**Note 1:** BGA package available in Tape and Reel only.

UHC™ is a trademark of Fairchild Semiconductor Corporation.

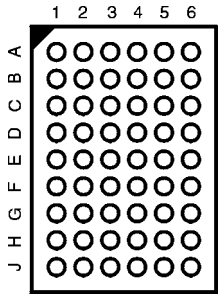
 

## Connection Diagrams

**Pin Assignment for TSSOP**




**Pin Assignment for FBGA**




**(Top Thru View)**

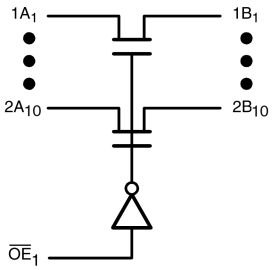
## Pin Descriptions

| Pin Name | Description |
|---|---|
| $\overline{OE}_1$, $\overline{OE}_2$ | Bus Switch Enables |
| 1A, 2A | Bus A |
| 1B, 2B | Bus B |
| $S_0$, $S_1$ | Bit Configuration Enables |
| $S_2$ | Level Shifting Diode Enable |
| NC | No Connect |

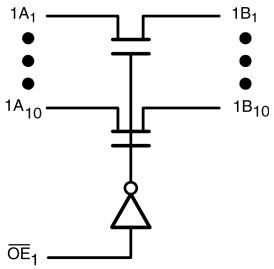
## FBGA Pin Assignments

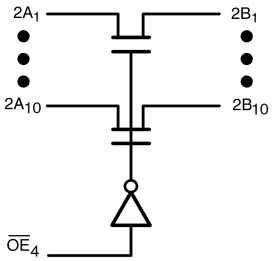
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $1A_3$ | $1A_2$ | $\overline{OE}_1$ | $\overline{OE}_2$ | $1B_2$ | $1B_3$ |
| **B** | $1A_5$ | $1A_4$ | $1A_1$ | $1B_1$ | $1B_4$ | $1B_5$ |
| **C** | $1A_7$ | $1A_6$ | GND | $\overline{OE}_5$ | $1B_6$ | $1B_7$ |
| **D** | $1A_9$ | $1A_8$ | GND | $V_{CC}$ | $1B_8$ | $1B_9$ |
| **E** | $2A_1$ | $1A_{10}$ | $S_0$ | $V_{CC}$ | $1B_{10}$ | $2B_1$ |
| **F** | $2A_3$ | $2A_2$ | $S_1$ | $S_2$ | $2B_2$ | $2B_3$ |
| **G** | $2A_5$ | $2A_4$ | $V_{CC}$ | GND | $2B_4$ | $2B_5$ |
| **H** | $2A_7$ | $2A_6$ | $2A_{10}$ | $2B_{10}$ | $2B_6$ | $2B_7$ |
| **J** | $2A_9$ | $2A_8$ | $\overline{OE}4$ | $\overline{OE}_3$ | $2B_8$ | $2B_9$ |

## Logic Diagrams

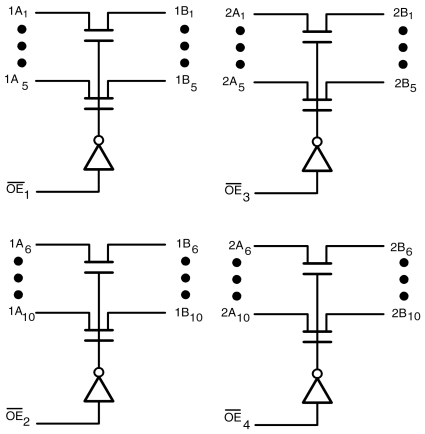



**20-Bit Configuration**
**(Configuration 1)**

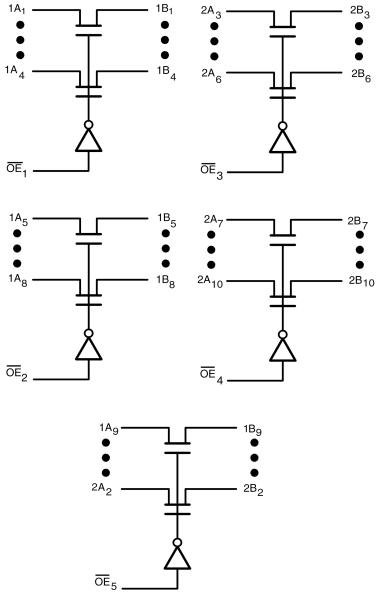



**10-Bit Configuration**
**(Configuration 2)**




**5-Bit Configuration**
**(Configuration 3)**




**4-Bit Configuration**
**(Configuration 4)**

## Functional Description

The device can also be configured as an 8 and 16-bit device by grounding the unused pins in Configurations 2 and 1 respectively. The 8-bit configuration may also be achieved by tying two of the 4-bit enables from configuration together and tying the remaining enable pin ($\overline{OE}$) HIGH.

## Truth Tables ($X = V_{CC}$ or GND)

**(see Functional Description)**

| Select Pin | |
|---|---|
| $S_2$ | Mode |
| L | Std. NMOS Switch |
| H | Level Shifting Diode Enabled |

| Configuration 1 | | $S_0 = S_1 = L$ | | | 20-Bit Configuration |
|---|---|---|---|---|---|
| Inputs | | | | | Inputs/Outputs |
| $\overline{OE}_1$ | $\overline{OE}_2$ | $\overline{OE}_3$ | $\overline{OE}_4$ | $\overline{OE}_5$ | |
| L | X | X | X | X | $1A_{1-10} = 1B_{1-10}$, $2A_{1-10} = 2B_{1-10}$ |
| H | X | X | X | X | Z |

| Configuration 2 | | $S_0 = L, S_1 = H$ | | | 10-Bit Configuration | |
|---|---|---|---|---|---|---|
| Inputs | | | | | Inputs/Outputs | |
| $\overline{OE}_1$ | $\overline{OE}_2$ | $\overline{OE}_3$ | $\overline{OE}_4$ | $\overline{OE}_5$ | $1A_{1-10} = 1B_{1-10}$ | $2A_{1-10} = 2B_{1-10}$ |
| L | X | X | L | X | $1A_X = 1B_X$ | $2A_X = 2B_X$ |
| L | X | X | H | X | $1A_X = 1B_X$ | Z |
| H | X | X | L | X | Z | $2A_X = 2B_X$ |
| H | X | X | H | X | Z | Z |

| Configuration 3 | | | $S_0 = H, S_1 = L$ | | 5-Bit Configuration | | | |
|---|---|---|---|---|---|---|---|---|
| Inputs | | | | | Inputs/Outputs | | | |
| $\overline{OE}_1$ | $\overline{OE}_2$ | $\overline{OE}_3$ | $\overline{OE}_4$ | $\overline{OE}_5$ | $1A_{1-5}, 1B_{1-5}$ | $1A_{6-10}, 1B_{6-10}$ | $2A_{1-5}, 2B_{1-5}$ | $2A_{6-10}, 2B_{6-10}$ |
| L | L | L | L | X | $1A_x = 1B_x$ | $1A_y = 1B_y$ | $2A_x = 2B_x$ | $2A_y = 2B_y$ |
| L | L | L | H | X | $1A_x = 1B_x$ | $1A_y = 1B_y$ | $2A_x = 2B_x$ | Z |
| L | L | H | L | X | $1A_x = 1B_x$ | $1A_y = 1B_y$ | Z | $2A_y = 2B_y$ |
| L | L | H | H | X | $1A_x = 1B_x$ | $1A_y = 1B_y$ | Z | Z |
| L | H | L | L | X | $1A_x = 1B_x$ | Z | $2A_x = 2B_x$ | $2A_y = 2B_y$ |
| L | H | L | H | X | $1A_x = 1B_x$ | Z | $2A_x = 2B_x$ | Z |
| L | H | H | L | X | $1A_x = 1B_x$ | Z | Z | $2A_y = 2B_y$ |
| L | H | H | H | X | $1A_x = 1B_x$ | Z | Z | Z |
| H | L | L | L | X | Z | $1A_y = 1B_y$ | $2A_x = 2B_x$ | $2A_y = 2B_y$ |
| H | L | L | H | X | Z | $1A_y = 1B_y$ | $2A_x = 2B_x$ | Z |
| H | L | H | L | X | Z | $1A_y = 1B_y$ | Z | $2A_y = 2B_y$ |
| H | L | H | H | X | Z | $1A_y = 1B_y$ | Z | Z |
| H | H | L | L | X | Z | Z | $2A_x = 2B_x$ | $2A_y = 2B_y$ |
| H | H | L | H | X | Z | Z | $2A_x = 2B_x$ | Z |
| H | H | H | L | X | Z | Z | Z | $2A_y = 2B_y$ |
| H | H | H | H | X | Z | Z | Z | Z |

## Truth Tables (Continued)

| Configuration 4 | | | $S_0 = S_1 = H$ | | 4-Bit Configuration | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Inputs | | | | | Inputs/Outputs | | | | |
| $OE_1$ | $OE_2$ | $OE_3$ | $OE_4$ | $OE_5$ | $1A_{1-4}$, $1B_{1-4}$ | $1A_{5-8}$, $1B_{5-8}$ | $2A_{3-6}$, $2B_{3-6}$ | $2A_{7-10}$, $2B_{7-10}$ | $1A_{9-10}$, $2B_{9-10}$ $2A_{1-2}$, $2B_{1-2}$ |
| L | L | L | L | L | $1A_x = 1B_x$ | $1A_y = 1B_y$ | $2A_x = 2B_x$ | $2A_y = 2B_y$ | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| L | L | L | L | H | $1A_x = 1B_x$ | $1A_y = 1B_y$ | $2A_x = 2B_x$ | $2A_y = 2B_y$ | Z |
| L | L | L | H | L | $1A_x = 1B_x$ | $1A_y = 1B_y$ | $2A_x = 2B_x$ | Z | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| L | L | L | H | H | $1A_x = 1B_x$ | $1A_y = 1B_y$ | $2A_x = 2B_x$ | Z | Z |
| L | L | H | L | L | $1A_x = 1B_x$ | $1A_y = 1B_y$ | Z | $2A_y = 2B_y$ | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| L | L | H | L | H | $1A_x = 1B_x$ | $1A_y = 1B_y$ | Z | $2A_y = 2B_y$ | Z |
| L | L | H | H | L | $1A_x = 1B_x$ | $1A_y = 1B_y$ | Z | Z | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| L | L | H | H | H | $1A_x = 1B_x$ | $1A_y = 1B_y$ | Z | Z | Z |
| L | H | L | L | L | $1A_x = 1B_x$ | Z | $2A_x = 2B_x$ | $2A_y = 2B_y$ | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| L | H | L | L | H | $1A_x = 1B_x$ | Z | $2A_x = 2B_x$ | $2A_y = 2B_y$ | Z |
| L | H | L | H | L | $1A_x = 1B_x$ | Z | $2A_x = 2B_x$ | Z | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| L | H | L | H | H | $1A_x = 1B_x$ | Z | $2A_x = 2B_x$ | Z | Z |
| L | H | H | L | L | $1A_x = 1B_x$ | Z | Z | $2A_y = 2B_y$ | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| L | H | H | L | H | $1A_x = 1B_x$ | Z | Z | $2A_y = 2B_y$ | Z |
| L | H | H | H | L | $1A_x = 1B_x$ | Z | Z | Z | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| L | H | H | H | H | $1A_x = 1B_x$ | Z | Z | Z | Z |
| H | L | L | L | L | Z | $1A_y = 1B_y$ | $2A_x = 2B_x$ | $2A_y = 2B_y$ | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| H | L | L | L | H | Z | $1A_y = 1B_y$ | $2A_x = 2B_x$ | $2A_y = 2B_y$ | Z |
| H | L | L | H | L | Z | $1A_y = 1B_y$ | $2A_x = 2B_x$ | Z | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| H | L | L | H | H | Z | $1A_y = 1B_y$ | $2A_x = 2B_x$ | Z | Z |
| H | L | H | L | L | Z | $1A_y = 1B_y$ | Z | $2A_y = 2B_y$ | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| H | L | H | L | H | Z | $1A_y = 1B_y$ | Z | $2A_y = 2B_y$ | Z |
| H | L | H | H | L | Z | $1A_y = 1B_y$ | Z | Z | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| H | L | H | H | H | Z | $1A_y = 1B_y$ | Z | Z | Z |
| H | H | L | L | L | Z | Z | $2A_x = 2B_x$ | $2A_y = 2B_y$ | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| H | H | L | L | H | Z | Z | $2A_x = 2B_x$ | $2A_y = 2B_y$ | Z |
| H | H | L | H | L | Z | Z | $2A_x = 2B_x$ | Z | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| H | H | L | H | H | Z | Z | $2A_x = 2B_x$ | Z | Z |
| H | H | H | L | L | Z | Z | Z | $2A_y = 2B_y$ | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| H | H | H | L | H | Z | Z | Z | $2A_y = 2B_y$ | Z |
| H | H | H | H | L | Z | Z | Z | Z | $1A_z = 1B_z$ $2A_z = 2B_z$ |
| H | H | H | H | H | Z | Z | Z | Z | Z |

## Absolute Maximum Ratings (Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Switch Voltage ($V_S$) (Note 3) | −2.0V to +7.0V |
| DC Input Control Pin Voltage ($V_{IN}$) (Note 4) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) $V_{IN}$ < 0V | −50 mA |
| DC Output ($I_{OUT}$) Current | 128 mA |
| DC $V_{CC}$/GND Current ($I_{CC}$/$I_{GND}$) | +/− 100 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150 °C |

## Recommended Operating Conditions (Note 5)

| | |
|---|---|
| Power Supply Operating ($V_{CC}$) | 4.0V to 5.5V |
| Input Voltage ($V_{IN}$) | 0V to 5.5V |
| Output Voltage ($V_{OUT}$) | 0V to 5.5V |
| Free Air Operating Temperature ($T_A$) | -40 °C to +85 °C |

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** $V_S$ is the voltage observed/applied at either the A or B Ports across the switch.

**Note 4:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 5:** Unused control inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = −40 °C to +85 °C | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ (Note 6) | Max | | |
| $V_{IK}$ | Clamp Diode Voltage | 4.5 | | | −1.2 | V | $I_{IN}$ = −18 mA |
| $V_{IH}$ | HIGH Level Input Voltage | 4.0-5.5 | 2.0 | | | V | IF $S_2$ = HIGH 4.5V ≤ $V_{CC}$ ≤ 5.5V |
| $V_{IL}$ | LOW Level Input Voltage | 4.0-5.5 | | | 0.8 | V | IF $S_2$ = HIGH 4.5V ≤ $V_{CC}$ ≤ 5.5V |
| $V_{OH}$ | HIGH Level Output Voltage | 4.5-5.5 | See Figure 4 | | | V | $S_2$ = $V_{CC}$ |
| $I_I$ | Input Leakage Current | 5.5 | | | ±1.0 | µA | 0 ≤ $V_{IN}$ ≤ 5.5V |
| | | 0 | | | 10 | µA | $V_{IN}$ = 5.5V |
| $I_{OZ}$ | OFF-STATE Leakage Current | 5.5 | | | ±1.0 | µA | 0 ≤ A, B ≤ $V_{CC}$ |
| $R_{ON}$ | Switch On Resistance (Note 7) | 4.5 | | 4 | 7 | Ω | $V_{IN}$ = 0V, $I_{IN}$ = 64 mA, $S_2$ = 0V or $V_{CC}$ |
| | | 4.5 | | 4 | 7 | Ω | $V_{IN}$ = 0V, $I_{IN}$ = 30 mA, $S_2$ = 0V or $V_{CC}$ |
| | | 4.5 | | 8 | 12 | Ω | $V_{IN}$ = 2.4V, $I_{IN}$ = 15 mA, $S_2$ = 0V |
| | | 4.0 | | 11 | 20 | Ω | $V_{IN}$ = 2.4V, $I_{IN}$ = 15 mA, $S_2$ = 0V |
| | | 4.5 | | 35 | 50 | Ω | $V_{IN}$ = 2.4V, $I_{IN}$ = 15 mA, $S_2$ = $V_{CC}$ |
| $I_{CC}$ | Quiescent Supply Current | 5.5 | | | 3 | µA | $S_2$ = GND, $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 |
| | | | | | 10 | µA | $S_2$ = $V_{CC}$, $\overline{OE}_x$ = $V_{CC}$, $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 |
| | | | | | 1.5 | mA | $S_2$ = $V_{CC}$, $\overline{OE}_x$ = GND, $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | 5.5 | | | 2.5 | mA | One Input at 3.4V<br>Other Inputs at $V_{CC}$ or GND, $S_2$ = 0V |
| | | | | | 4.0 | mA | One Input at 3.4V<br>Other Inputs at $V_{CC}$ or GND, $S_2$ = $V_{CC}$ |
| $V_{IKU}$ | Voltage Undershoot | 5.5 | | | −2.0 | V | 0.0 mA ≥ $I_{IN}$ ≥ −50 mA<br>$\overline{OE}_x$ = 5.5V |

**Note 6:** Typical values are at $V_{CC}$ = 5.0V and $T_A$ = +25°C

**Note 7:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$ | | | | Units | Conditions ($S_2 = 0V$) | Figure Number |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC} = 4.5 - 5.5V$ | | $V_{CC} = 4.0V$ | | | | |
| | | Min | Max | Min | Max | | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Bus-to-Bus (Note 8) | | 0.25 | | 0.25 | ns | $V_I$ = OPEN | Figures 2, 3 |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time | 1.5 | 6.5 | | 7.0 | ns | $V_I$ = 7V for $t_{PZL}$<br>$V_I$ = OPEN for $t_{PZH}$ | Figures 2, 3 |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time | 1.5 | 6.7 | | 7.2 | ns | $V_I$ = 7V for $t_{PLZ}$<br>$V_I$ = OPEN for $t_{PHZ}$ | Figures 2, 3 |
| $t_{PZH}$, $t_{PZL}$ | $S_{el}$ ($S_{0,1}$) to Output Enable Time | 1.5 | 7.0 | | 7.5 | ns | $V_I$ = 7V for $t_{PZL}$<br>$V_I$ = OPEN for $t_{PZH}$ | Figures 2, 3 |
| $t_{PHZ}$, $t_{PLZ}$ | $S_{el}$ ($S_{0,1}$) to Output Disable Time | 1.5 | 7.5 | | 7.7 | ns | $V_I$ = 7V for $t_{PLZ}$<br>$V_I$ = OPEN for $t_{PHZ}$ | Figures 2, 3 |

**Note 8:** This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

## AC Electrical Characteristics: Translating Diode

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$ | | Units | Conditions ($S_2 = V_{CC}$) | Figure Number |
|---|---|---|---|---|---|---|
| | | $V_{CC} = 4.5 - 5.5V$ | | | | |
| | | Min | Max | | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Bus-to-Bus (Note 9) | | 0.25 | ns | $V_I$ = OPEN | Figures 2, 3 |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time | 1.5 | 10.0 | ns | $V_I$ = 7V for $t_{PZL}$<br>$V_I$ = OPEN for $t_{PZH}$ | Figures 2, 3 |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time | 1.5 | 9.0 | ns | $V_I$ = 7V for $t_{PLZ}$<br>$V_I$ = OPEN for $t_{PHZ}$ | Figures 2, 3 |
| $t_{PZH}$, $t_{PZL}$ | $S_{el}$ ($S_{0,1}$) to Output Enable Time | 1.5 | 11.0 | ns | $V_I$ = 7V for $t_{PZL}$<br>$V_I$ = OPEN for $t_{PZH}$ | Figures 2, 3 |
| $t_{PHZ}$, $t_{PLZ}$ | $S_{el}$ ($S_{0,1}$) to Output Disable Time | 1.5 | 10.0 | ns | $V_I$ = 7V for $t_{PLZ}$<br>$V_I$ = OPEN for $t_{PHZ}$ | Figures 2, 3 |

**Note 9:** This parameter is guaranteed by design but is not tested. This bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

## Capacitance (Note 10)

| Symbol | Parameter | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Control Pin Input Capacitance | 4 | | pF | $V_{CC}$ = 5.0V, $V_{IN}$ = 0V |
| $C_{I/O}$ | Input/Output Capacitance "OFF State" | 8 | | pF | $V_{CC}$, $\overline{OE}$ = 5.0V, $V_{IN}$ = 0V |

**Note 10:** $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

## Undershoot Characteristic (Note 11)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OUTU}$ | Output Voltage During Undershoot | 2.5 | $V_{OH} - 0.3$ | | V | $S_2 = 0V$, Figure 1 |
| | | TBD | TBD | | V | $S_2 = V_{CC}$ |

**Note 11:** This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

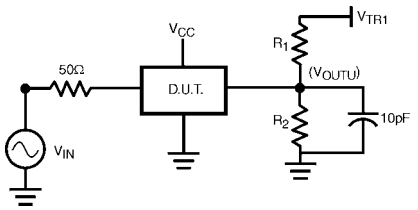
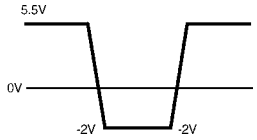



**FIGURE 1.**

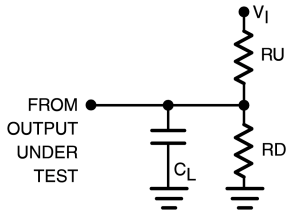
## Device Test Conditions

| Parameter | Value | Units |
|---|---|---|
| $V_{IN}$ | see Waveform | V |
| $R_1 = R_2$ | 100K | Ω |
| $V_{TRI}$ | 11.0 | V |
| $V_{CC}$ | 5.5 | V |

## Transient Input Voltage ($V_{IN}$) Waveform




## AC Loading and Waveforms




**Note:** Input driven by 50Ω source terminated in 50Ω

**Note:** $C_L$ includes load and stray capacitance

**Note:** Input Frequency = 1.0 MHz, $t_W = 500$ ns

**FIGURE 2. AC Test Circuit**

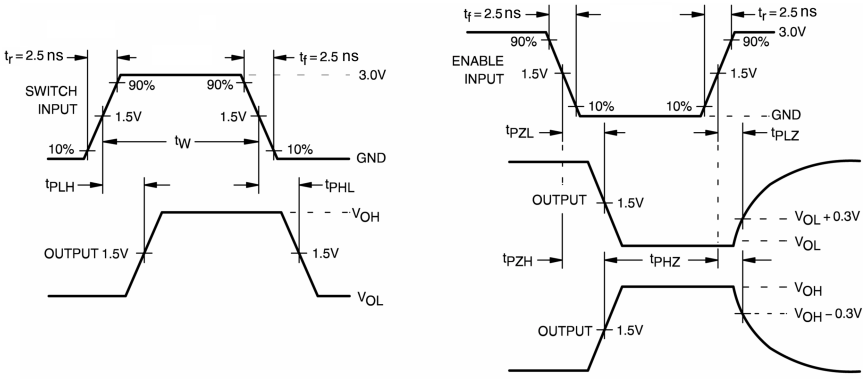
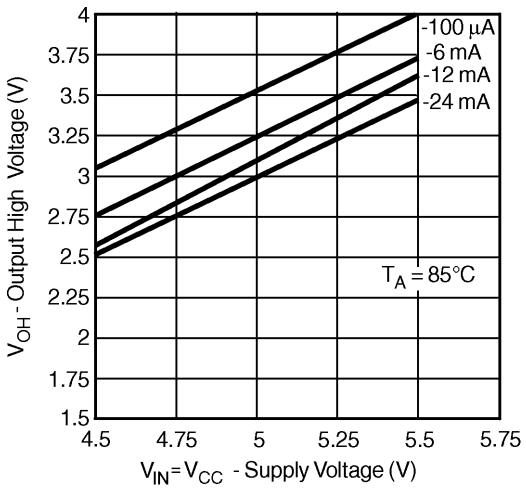
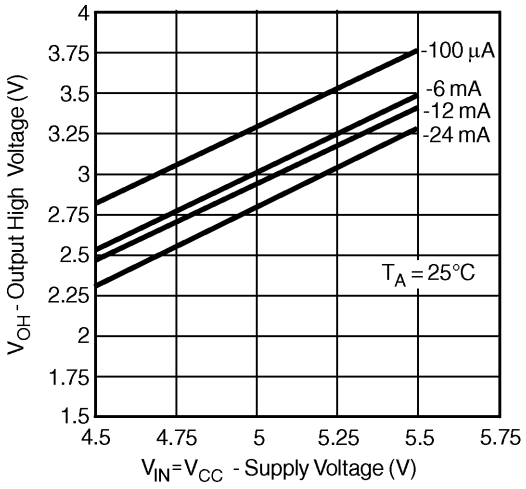



**FIGURE 3. AC Waveforms**



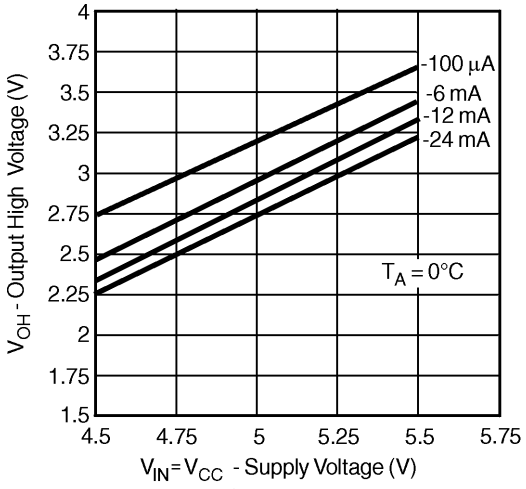
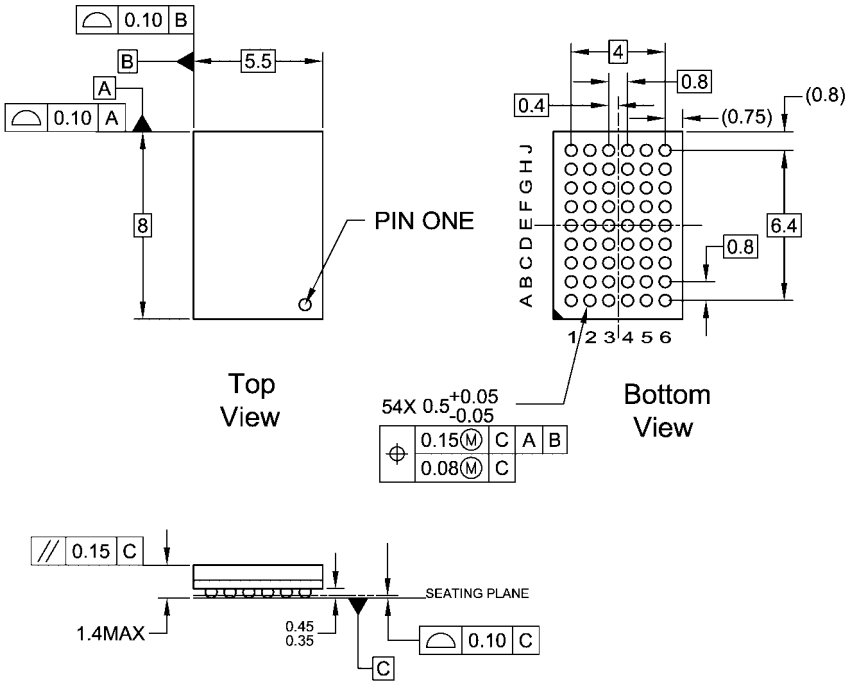




**FIGURE 4.**

## Physical Dimensions inches (millimeters) unless otherwise noted



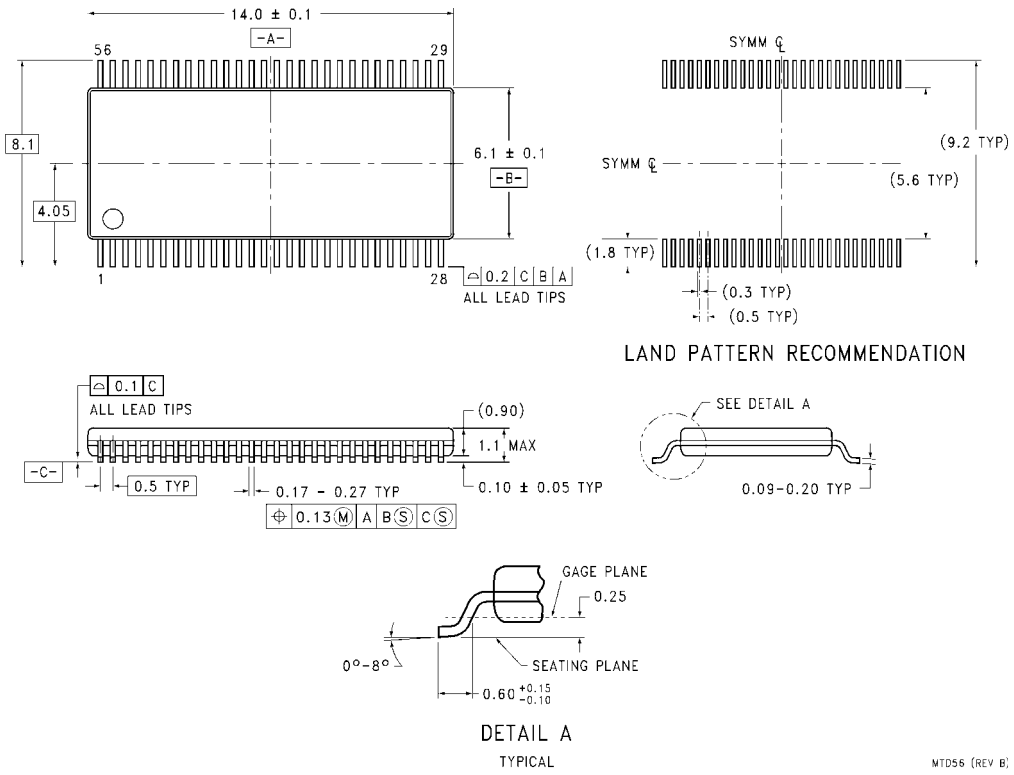

NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide**
**Package Number BGA54A**
**Preliminary**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD56**

## Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.