# MC74VHCT139A

# Dual 2-to-4 Decoder/ Demultiplexer

The MC74VHCT139A is an advanced high speed CMOS 2−to−4 decoder/demultiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL devices while maintaining CMOS low power dissipation.

When the device is enabled ($\overline{E}$ = low), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device output is compatible with TTL−type input thresholds and the output has a full 5.0 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic−level translator from 3.0 V CMOS logic to 5.0 V CMOS logic, or from 1.8 V CMOS logic to 3.0 V CMOS logic while operating at the high−voltage power supply

The MC74VHCT139A input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHCT139A to be used to interface 5.0 V circuits to 3.0 V circuits. The output structures also provide protection when $V_{CC}$ = 0 V. These input and output structures help prevent device destruction caused by supply voltage−input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

- High Speed: $t_{PD}$ = 5.0 ns (Typ) at $V_{CC}$ = 5.0 V
- Low Power Dissipation: $I_{CC}$ = 4 μA (Max) at $T_A$ = 25°C
- TTL−Compatible Inputs: $V_{IL}$ = 0.8 V; $V_{IH}$ = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP}$ = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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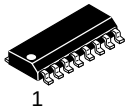
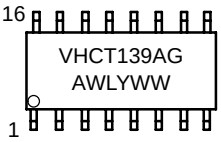
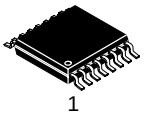
http://onsemi.com

### MARKING DIAGRAMS

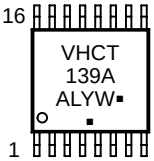


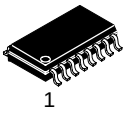
SOIC−16
D SUFFIX
CASE 751B



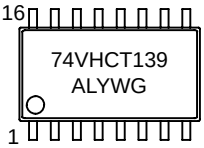



TSSOP−16
DT SUFFIX
CASE 948F



SOEIAJ−16
M SUFFIX
CASE 966




| | | |
|---|---|---|
| A | = | Assembly Location |
| WL, L | = | Wafer Lot |
| Y | = | Year |
| WW, W | = | Work Week |
| G or ▪ | = | Pb−Free Package |

(Note: Microdot may be in either location)

### FUNCTION TABLE

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| $\overline{E}$ | A1 | A0 | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

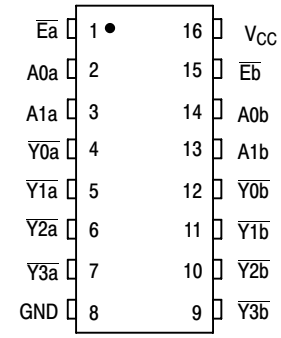



**Figure 1. Pin Assignment**

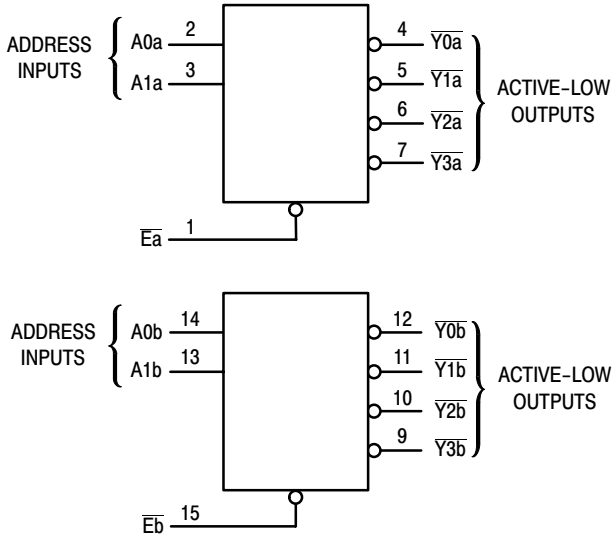



**Figure 2. Logic Diagram**

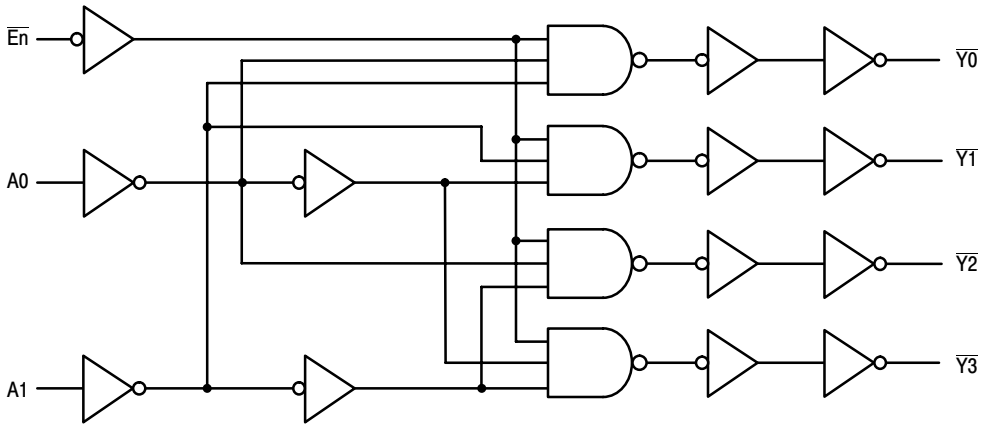



**Figure 3. Expanded Logic Diagram**
(1/2 of Device)

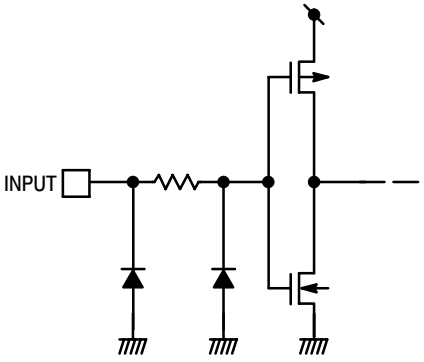



**Figure 4. Input Equivalent Circuit**

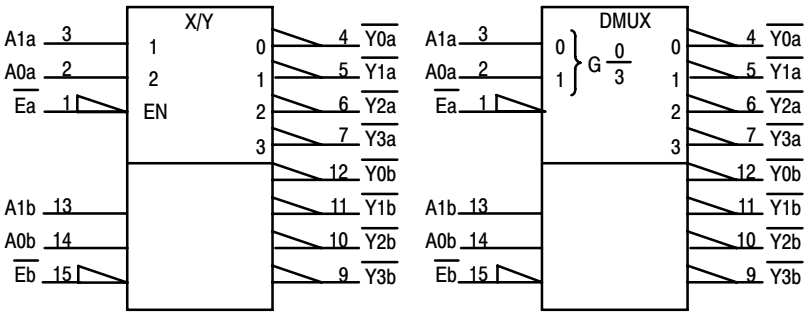



**Figure 5. IEC Logic Diagram**

**MAXIMUM RATINGS** (Note 1)

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | Digital Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | Output in 3−State<br>High or Low State | −0.5 to +7.0<br>−0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | Input Diode Current | | −20 | mA |
| $I_{OK}$ | Output Diode Current | | ± 20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ± 75 | mA |
| $P_D$ | Power Dissipation in Still Air | SOIC Package<br>TSSOP | 200<br>180 | mW |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 2)<br>Machine Model (Note 3)<br>Charged Device Model (Note 4) | >2000<br>>200<br>>2000 | V |
| $I_{LATCHUP}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 125°C (Note 5) | ± 300 | mA |
| $\theta_{JA}$ | Thermal Resistance, Junction−to−Ambient | SOIC Package<br>TSSOP | 143<br>164 | °C/W |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22−A114−A
3. Tested to EIA/JESD22−A115−A
4. Tested to JESD22−C101−A
5. Tested to EIA/JESD78

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | 4.5 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage | 0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage Output in 3−State<br>High or Low State | 0<br>0 | 5.5<br>$V_{CC}$ | V |
| $T_A$ | Operating Temperature Range, all Package Types | −55 | 125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Time $V_{CC}$ = 5.0 V ± 0.5 V | 0 | 20 | ns/V |

**DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES**

| Junction Temperature °C | Time, Hours | Time, Years |
|---|---|---|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

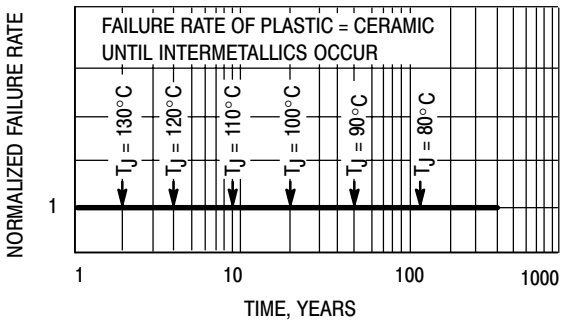



**Figure 6. Failure Rate vs. Time Junction Temperature**

**DC CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | $T_A \le$ 85°C Min | $T_A \le$ 85°C Max | $T_A$ = − 55 to 125°C Min | $T_A$ = − 55 to 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High−Level Input Voltage | | 4.5 to 5.5 | 2 | | | 2 | | 2 | | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | | 0.8 | V |
| $V_{OH}$ | Maximum High−Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -50$ μA | 4.5 | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -8$ mA | 4.5 | 3.94 | | | 3.8 | | 3.66 | | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL} = 50$ μA | 4.5 | | 0 | 0.1 | | 0.1 | | 0.1 | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = 8$ mA | 4.5 | | | 0.36 | | 0.44 | | 0.52 | |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 4.0 | | 40.0 | | 40.0 | μA |
| $I_{CCT}$ | Additional Quiescent Supply Current (per Pin) | Any one input:<br>$V_{IN}$ = 3.4 V<br>All other inputs:<br>$V_{IN} = V_{CC}$ or GND | 5.5 | | | 1.35 | | 1.5 | | 1.5 | μA |
| $I_{OPD}$ | Output Leakage Current | $V_{OUT}$ = 5.5 V | 0 | | | 0.5 | | 5 | | 5 | μA |

**AC ELECTRICAL CHARACTERISTICS** (Input $t_r = t_f$ = 3.0ns)

| Symbol | Parameter | Test Conditions | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | $T_A \le$ 85°C Min | $T_A \le$ 85°C Max | $T_A$ = − 55 to 125°C Min | $T_A$ = − 55 to 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, A to Y | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF | | 7.2 | 11.0 | 1.0 | 13.0 | 1.0 | 13.0 | ns |
| | | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 50 pF | | 9.7 | 14.5 | 1.0 | 16.5 | 1.0 | 16.5 | |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF | | 5.0 | 7.2 | 1.0 | 8.5 | 1.0 | 8.5 | |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 50 pF | | 6.5 | 9.2 | 1.0 | 10.5 | 1.0 | 10.5 | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, $\overline{E}$ to Y | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF | | 6.4 | 9.2 | 1.0 | 11.0 | 1.0 | 11.0 | ns |
| | | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 50 pF | | 8.9 | 12.7 | 1.0 | 14.5 | 1.0 | 14.5 | |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF | | 4.4 | 6.3 | 1.0 | 7.5 | 1.0 | 7.5 | |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 50 pF | | 5.9 | 8.3 | 1.0 | 9.5 | 1.0 | 9.5 | |
| $C_{IN}$ | Maximum Input Capacitance | | | 4 | 10 | | 10 | | 10 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 6) | 26 | pF |

6. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per decoder). $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

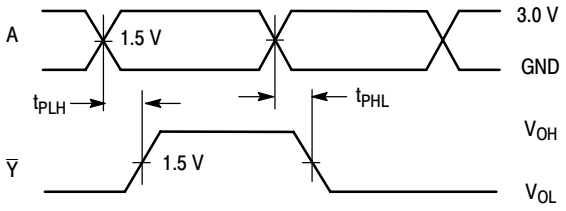



**Figure 7. Switching Waveform**

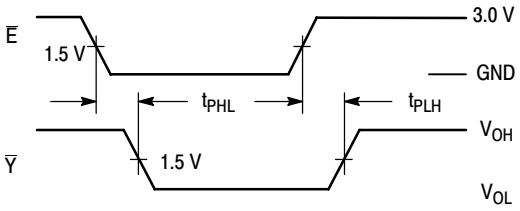
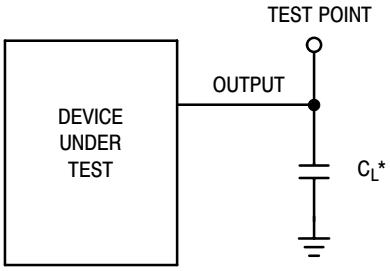



**Figure 8. Switching Waveform**




*Includes all probe and jig capacitance

**Figure 9. Test Circuit**

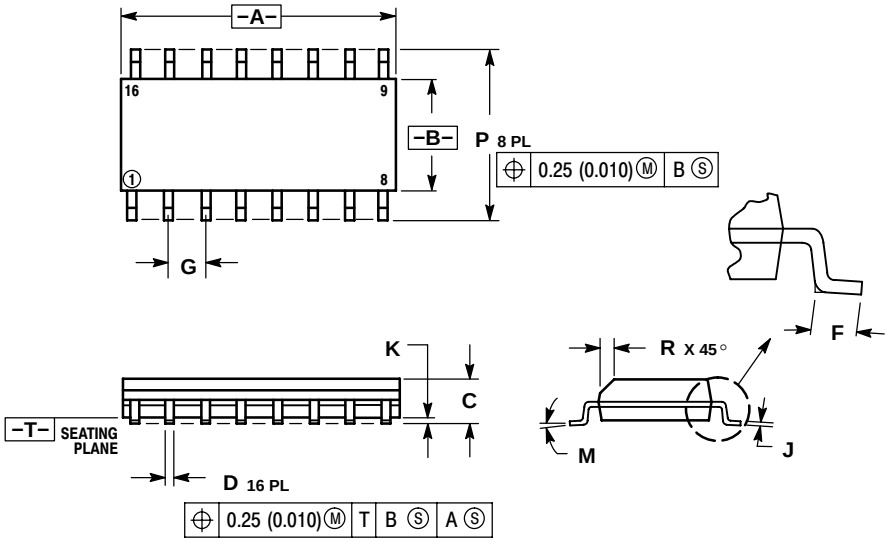
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74VHCT139AD | SOIC−16 | 48 Units / Rail |
| MC74VHCT139ADG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74VHCT139ADR2 | SOIC−16 | 2500 Tape & Reel |
| MC74VHCT139ADR2G | SOIC−16 (Pb−Free) | 2500 Tape & Reel |
| MC74VHCT139ADT | TSSOP−16* | 96 Units / Rail |
| MC74VHCT139ADTG | TSSOP−16* | 96 Units / Rail |
| MC74VHCT139ADTR2 | TSSOP−16* | 2500 Tape & Reel |
| MC74VHCT139ADTRG | TSSOP−16* | 2500 Tape & Reel |
| MC74VHCT139AM | SOEIAJ−16 | 50 Units / Rail |
| MC74VHCT139AMG | SOEIAJ−16 (Pb−Free) | 50 Units / Rail |
| MC74VHCT139AMEL | SOEIAJ−16 | 2000 Tape & Reel |
| MC74VHCT139AMELG | SOEIAJ−16 (Pb−Free) | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

## PACKAGE DIMENSIONS

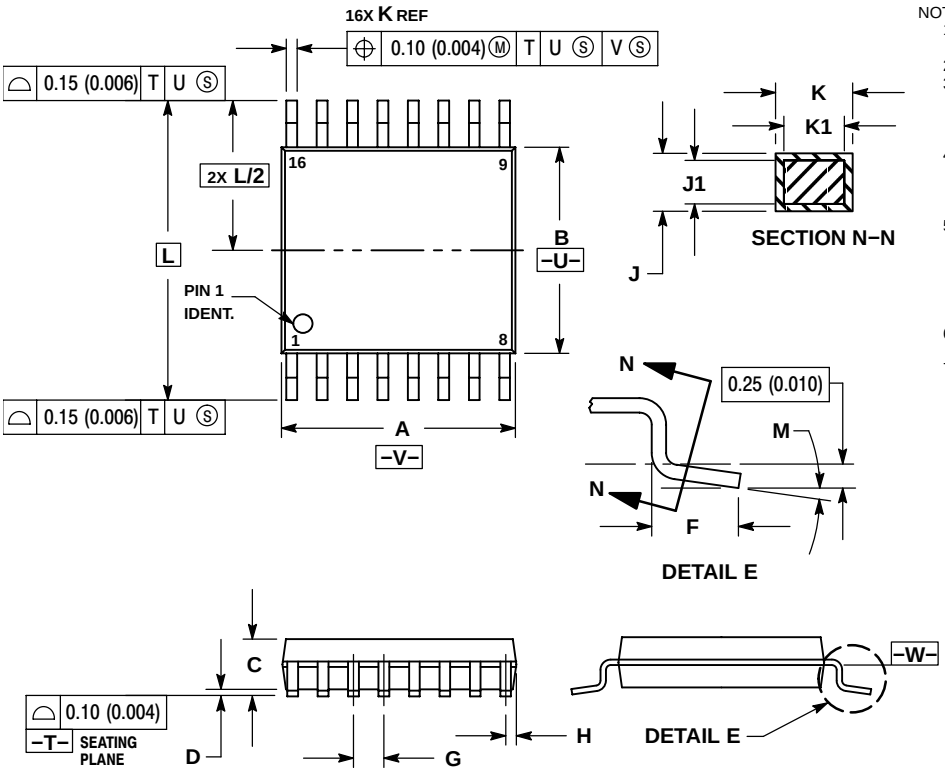
**SOIC−16**
**D SUFFIX**
CASE 751B−05
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

**TSSOP−16**
**DT SUFFIX**
CASE 948F−01
ISSUE A

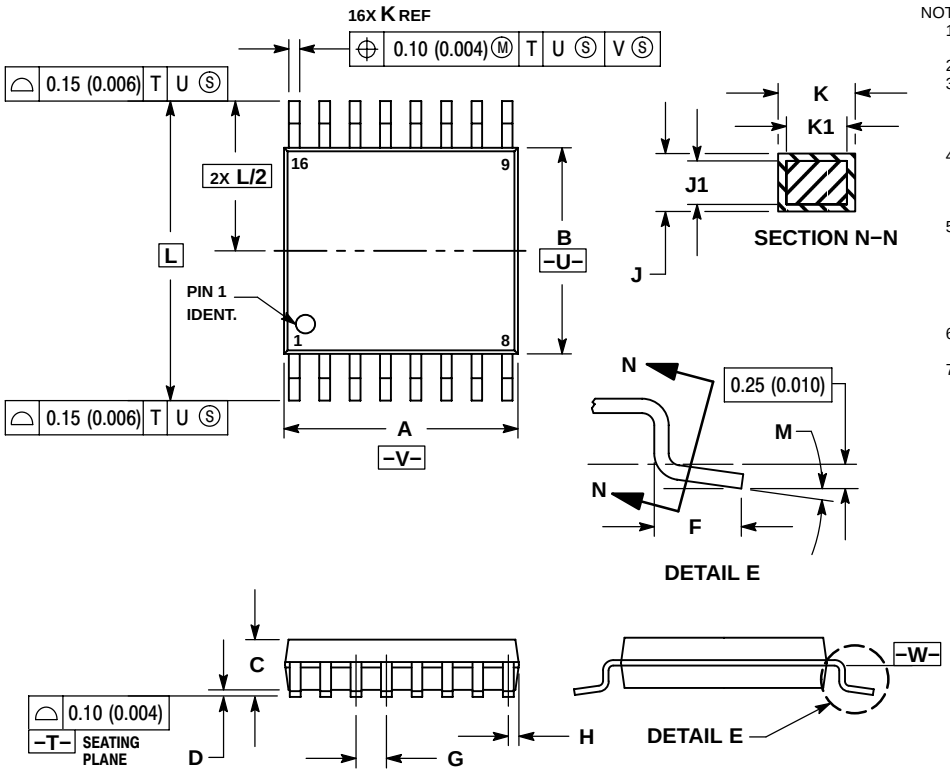



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

## PACKAGE DIMENSIONS

**SOEIAJ−16**
**M SUFFIX**
CASE 966−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |



### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
**Phone**: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
**Fax**: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada

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