

# MC74LVX139

## Dual 2-to-4 Decoder/ Demultiplexer

The MC74LVX139 is an advanced high speed CMOS 2-to-4 decoder/demultiplexer fabricated with silicon gate CMOS technology.

When the device is enabled ( $\bar{E}$  = low), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

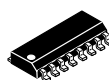
- High Speed:  $t_{PD} = 6.0$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise:  $V_{OLP} = 0.5$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Pb-Free Packages are Available\*



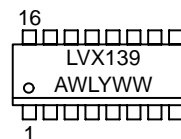
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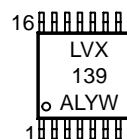
### MARKING DIAGRAMS



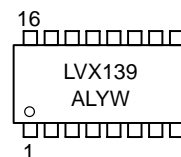
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
M SUFFIX  
CASE 966



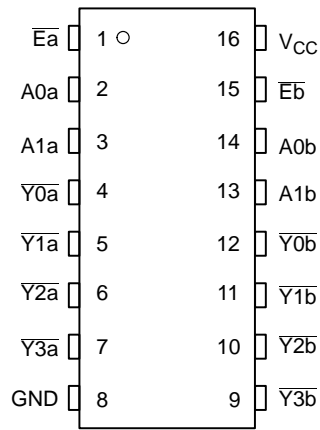
A = Assembly Location  
WL or L = Wafer Lot  
Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

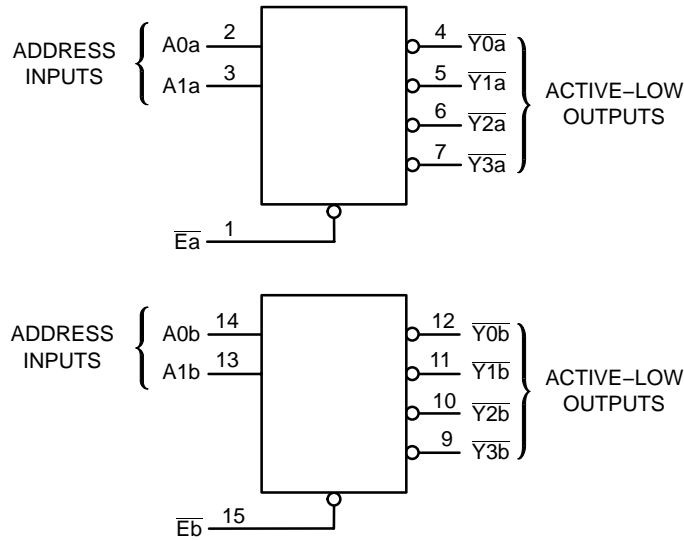
# MC74LVX139



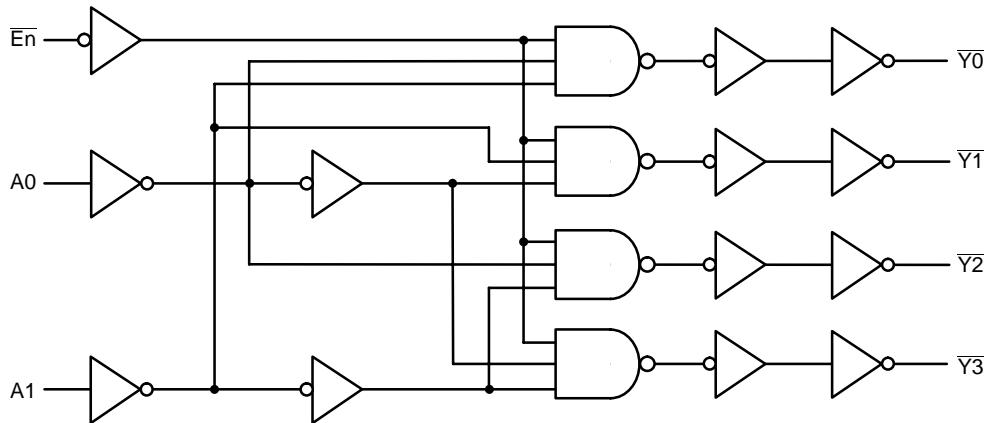
**FUNCTION TABLE**

E	Inputs		Outputs			
	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

**Figure 1. Pin Assignment**



**Figure 2. Logic Diagram**



**Figure 3. Expanded Logic Diagram**  
(1/2 of Device)

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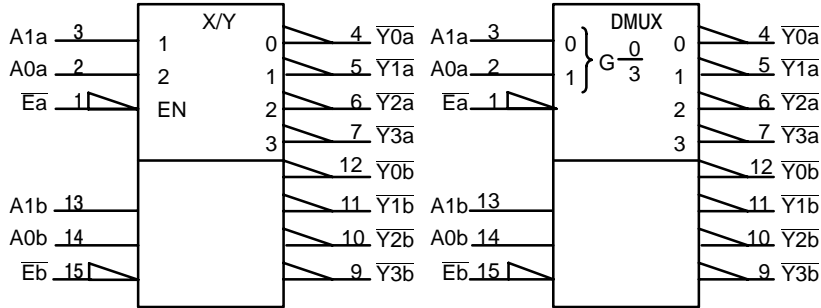


Figure 4. IEC Logic Diagram

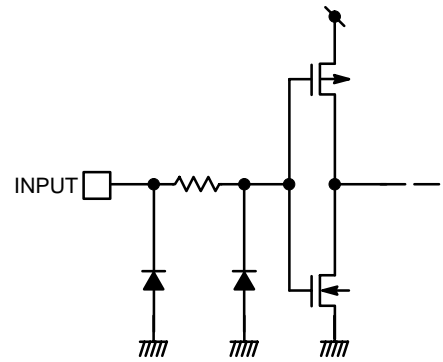


Figure 5. Input Equivalent Circuit

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Positive DC Supply Voltage	-0.5 to +7.0	V	
$V_{IN}$	Digital Input Voltage	-0.5 to +7.0	V	
$V_{OUT}$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V	
$I_{IK}$	Input Diode Current	-20	mA	
$I_{OK}$	Output Diode Current	$\pm 20$	mA	
$I_{OUT}$	DC Output Current, per Pin	$\pm 25$	mA	
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA	
$P_D$	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$	
$V_{ESD}$	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 >2000	V
$I_{LATCHUP}$	Latchup Performance	Above $V_{CC}$ and Below GND at 125 $^{\circ}C$ (Note 4)	$\pm 300$	mA
$\theta_{JA}$	Thermal Resistance, Junction-to-Ambient	SOIC Package TSSOP	143 164	$^{\circ}C/W$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	2.0	3.6	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature Range, all Package Types	-40	85	$^{\circ}C$
$t_r, t_f$	Input Rise or Fall Time			ns/V
		$V_{CC} = 5.0 V \pm 0.5 V$		

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## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0	0.75 V <sub>CC</sub>	-	-	0.75 V <sub>CC</sub>	-	V
			3.0	0.7 V <sub>CC</sub>	-	-	0.7 V <sub>CC</sub>	-	
			3.6	0.7 V <sub>CC</sub>	-	-	0.7 V <sub>CC</sub>	-	
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0	-	-	0.25 V <sub>CC</sub>	-	0.25 V <sub>CC</sub>	V
			3.0	-	-	0.3 V <sub>CC</sub>	-	0.3 V <sub>CC</sub>	
			3.6	-	-	0.3 V <sub>CC</sub>	-	0.3 V <sub>CC</sub>	
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	-	1.9	-	V
		I <sub>OH</sub> = -50 μA	3.0	2.9	3.0	-	2.9	-	
		I <sub>OH</sub> = -4 mA	3.0	2.58	3.0	-	2.48	-	
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 50 μA	2.0	-	0.0	0.1	-	0.1	V
		I <sub>OL</sub> = 50 μA	3.0	-	-	0.1	-	0.1	
		I <sub>OL</sub> = 4 mA	3.0	-	-	0.36	-	0.44	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 3.6	-	-	±0.1	-	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6	1.0	1.0	2.0	-	-	μA

## AC ELECTRICAL CHARACTERISTICS Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit	
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15 pF	-	8.5	15.0	1.0	17.8	ns	
		C <sub>L</sub> = 50 pF	-	11.0	16.5	1.0	18.0		
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15 pF	-	6.0	10.0	1.0	12.0		
		C <sub>L</sub> = 50 pF	-	8.5	13.0	1.0	15.0		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, E to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15 pF	-	8.0	13.0	1.0	15.5	ns	
		C <sub>L</sub> = 50 pF	-	10.0	16.5	1.0	18.0		
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15 pF	-	5.5	8.2	1.0	10.0		
		C <sub>L</sub> = 50 pF	-	7.5	13.0	1.0	15.0		
C <sub>IN</sub>	Maximum Input Capacitance		-	4	10	-	10	pF	
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	Typical @ 25°C, V <sub>CC</sub> = 3.3 V							pF
		26							

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/2 (per decoder). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

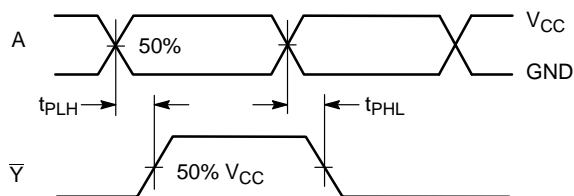


Figure 6. Switching Waveform

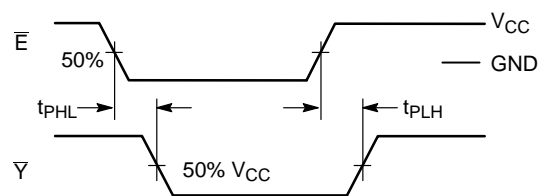
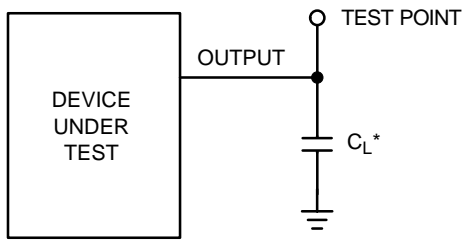


Figure 7. Switching Waveform

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\*Includes all probe and jig capacitance

Figure 8. Test Circuit

## ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX139DR2	SOIC-16	2500 Tape & Reel
MC74LVX139DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LVX139DTR2	TSSOP-16*	2500 Tape & Reel
MC74LVX139M	SOEIAJ-16	50 Units / Rail
MC74LVX139MG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC74LVX139MEL	SOEIAJ-16	2000 Tape & Reel
MC74LVX139MELG	SOEIAJ-16 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

Tape Size	B <sub>1</sub> Max	D	D <sub>1</sub>	E	F	K	P	P <sub>0</sub>	P <sub>2</sub>	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 -0.0 (0.059")	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")	+0.004 -0.0	1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

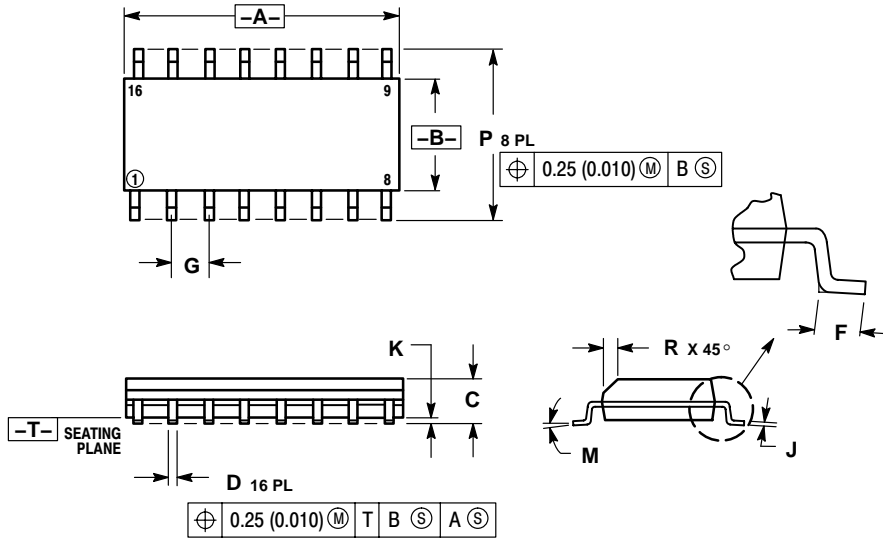
6. Metric Dimensions Govern-English are in parentheses for reference only.

7. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

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## PACKAGE DIMENSIONS

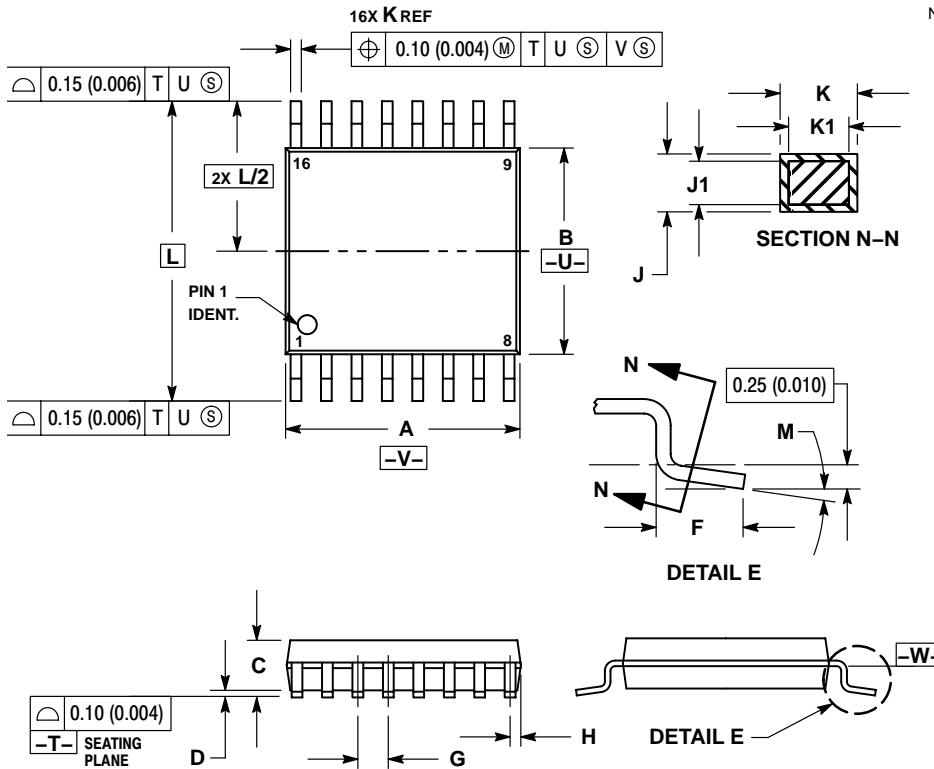
SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE A

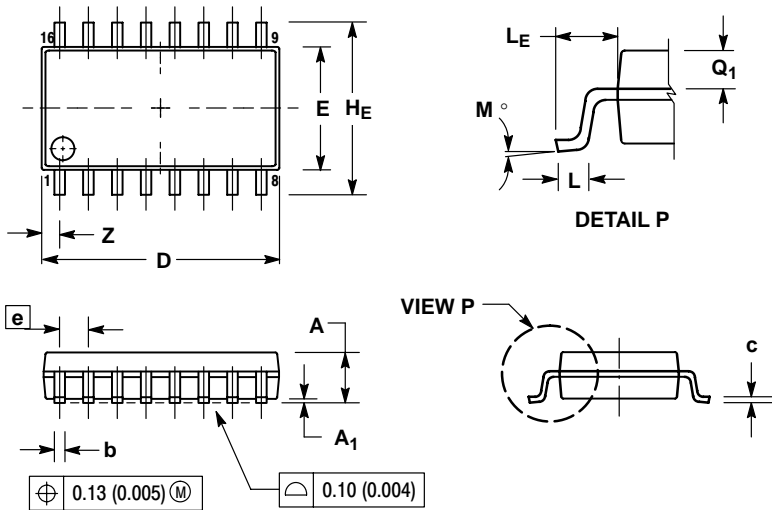


- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  - DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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SOEIAJ-16  
M SUFFIX  
CASE 966-01  
ISSUE O



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0° 10°		0° 10°	
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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