QUICKSWITCH® PRODUCTS 2.5V / 3.3V 32-BIT HIGH BANDWIDTH BUS SWITCH

IDTQS34XVH2245

FEATURES:

- **N channel FET switches with no parasitic diode to V_{CC}**
  - *Isolation under power-off conditions*
  - *No DC path to V_{CC} or GND*
  - *5V tolerant in OFF and ON state*
- **5V tolerant I/Os**
- **Flat R_{ON} characteristics over operating range**
- **Rail-to-rail switching 0 - 5V**
- **Bidirectional dataflow with near-zero delay: no added ground bounce**
- **Excellent R_{ON} matching between channels**
- **V_{CC} operation: 2.3V to 3.6V**
- **High bandwidth**
- **LVTTL-compatible control Inputs**
- **Undershoot Clamp Diodes on all switch and control Inputs**
- **Low I/O capacitance, 4pF typical**
- **25Ω resistors for low noise and line matching**
- **Available in 80-pin QVSOP package**

APPLICATIONS:

- **Hot-swapping**
- **Low distortion analog switch**
- **Replaces mechanical relay**
- **ATM 25/155 switching**

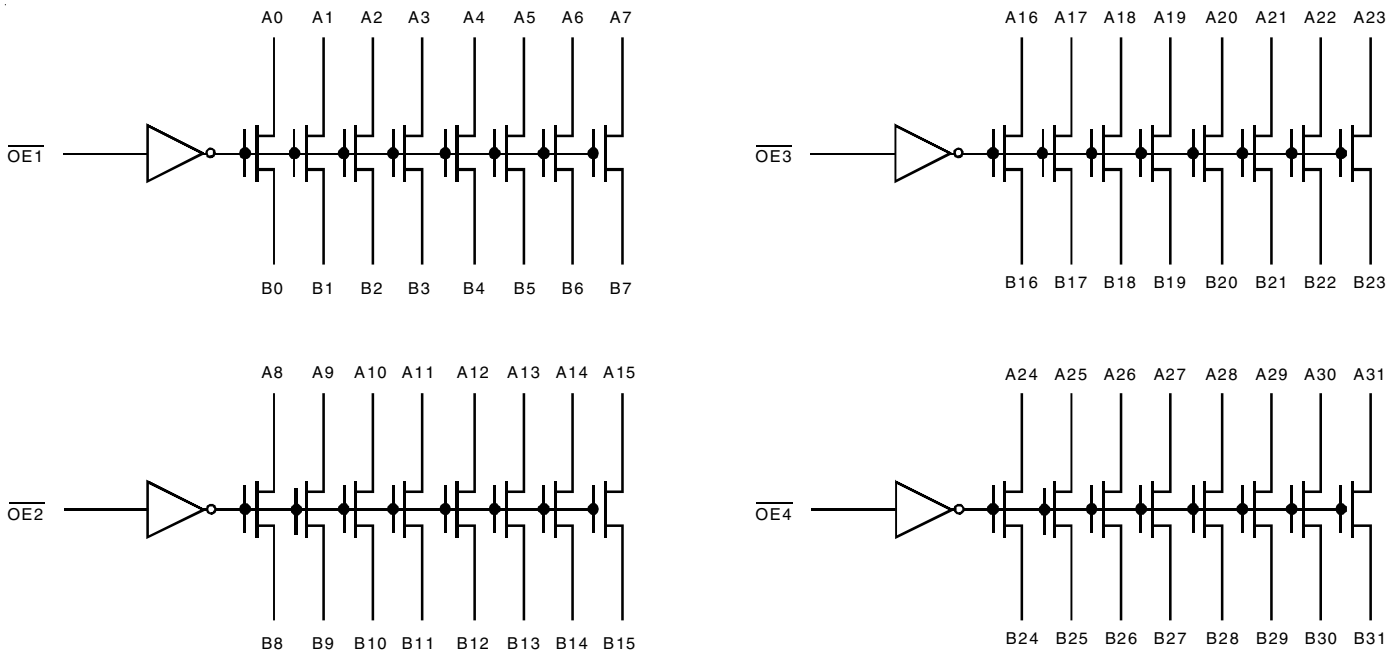
DESCRIPTION:

The QS34XVH2245 is a high bandwidth, 32-bit bus switch. The QS34XVH2245 with 25Ω resistance and 1.35ns propagation delay is ideal for line matching and low noise environments. The switches can be turned ON under the control of individual LVTTL-compatible Output Enable ($\overline{OEx}$) signals for bidirectional data flow with no added delay or ground bounce. In the ON state, the switches can pass signals up to 5V. In the OFF state, the switches offer very high impedance at the terminals.

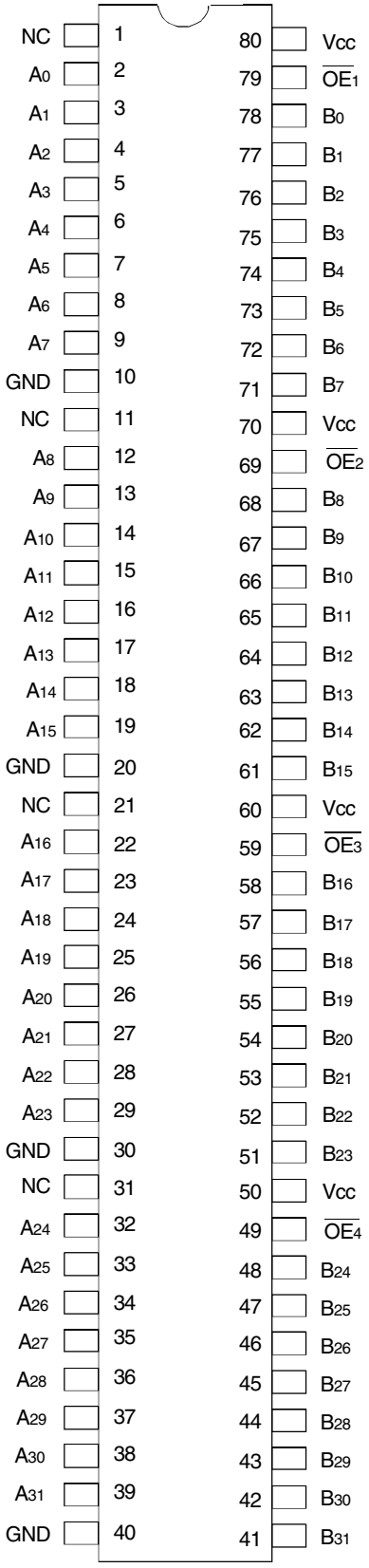
The combination of small propagation delay, high OFF impedance, and over-voltage tolerance makes the QS34XVH2245 ideal for high performance communications applications.

The QS34XVH2245 is characterized for operation from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	SupplyVoltage to Ground	–0.5 to +4.6	V
V_{TERM}(3)	DC Switch Voltage V_S	–0.5 to +5.5	V
V_{TERM}(3)	DC Input Voltage V_{IN}	–0.5 to +5.5	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	–3	V
I_{OUT}	DC Output Current (max. sink current/pin)	120	mA
T_{STG}	Storage Temperature	–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC} .

CAPACITANCE (T_A = +25°C, F = 1MHz, V_{IN} = 0V, V_{OUT} = 0V)

Symbol	Parameter(1)	Typ.	Max.	Unit
C_{IN}	Control Inputs	3	5	pF
$C_{I/O}$	Quickswitch Channels (Switch OFF)	4	6	pF
$C_{I/O}$	Quickswitch Channels (Switch ON)	8	12	pF

NOTE:
1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
$\overline{OEx}$	I	Output Enable
Ax	I/O	Bus A
Bx	I/O	Bus B

FUNCTION TABLE(1)

$\overline{OEx}$	Function
H	Disconnected
L	Connect (Ax = Bx)

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level

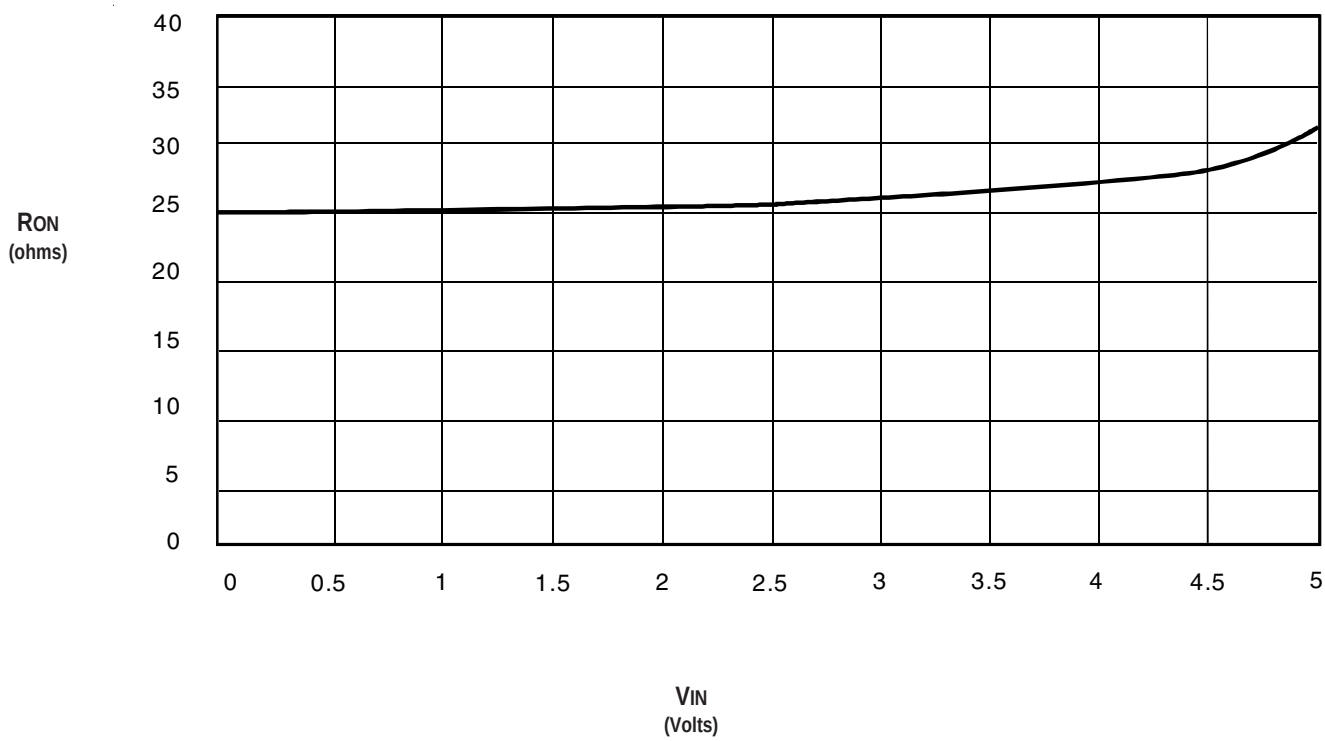
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions			Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		for Control Inputs	V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		for Control Inputs	V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IN}	Input Leakage Current (Control Inputs)	0V ≤ V_{IN} ≤ V_{CC}			—	—	±1	µA
I_{OZ}	Off-State Current (Hi-Z)	0V ≤ V_{OUT} ≤ 5V, Switches OFF			—	—	±1	µA
I_{OFF}	Data Input/Output Power Off Leakage	V_{IN} or V_{OUT} 0V to 5V, V_{CC} = 0V			—	—	±1	µA
R_{ON}	Switch ON Resistance	V_{CC} = 2.3V	V_{IN} = 0V	I_{ON} = 30mA	18	27	39	Ω
		Typical at V_{CC} = 2.5V	V_{IN} = 1.7V	I_{ON} = 15mA	18	28	41	
		V_{CC} = 3V	V_{IN} = 0V	I_{ON} = 30mA	18	25	38	
			V_{IN} = 2.4V	I_{ON} = 15mA	18	26	40	

NOTE:
1. Typical values are at V_{CC} = 3.3V and T_A = 25°C.

TYPICAL ON RESISTANCE vs V_{IN} AT V_{CC} = 3.3V

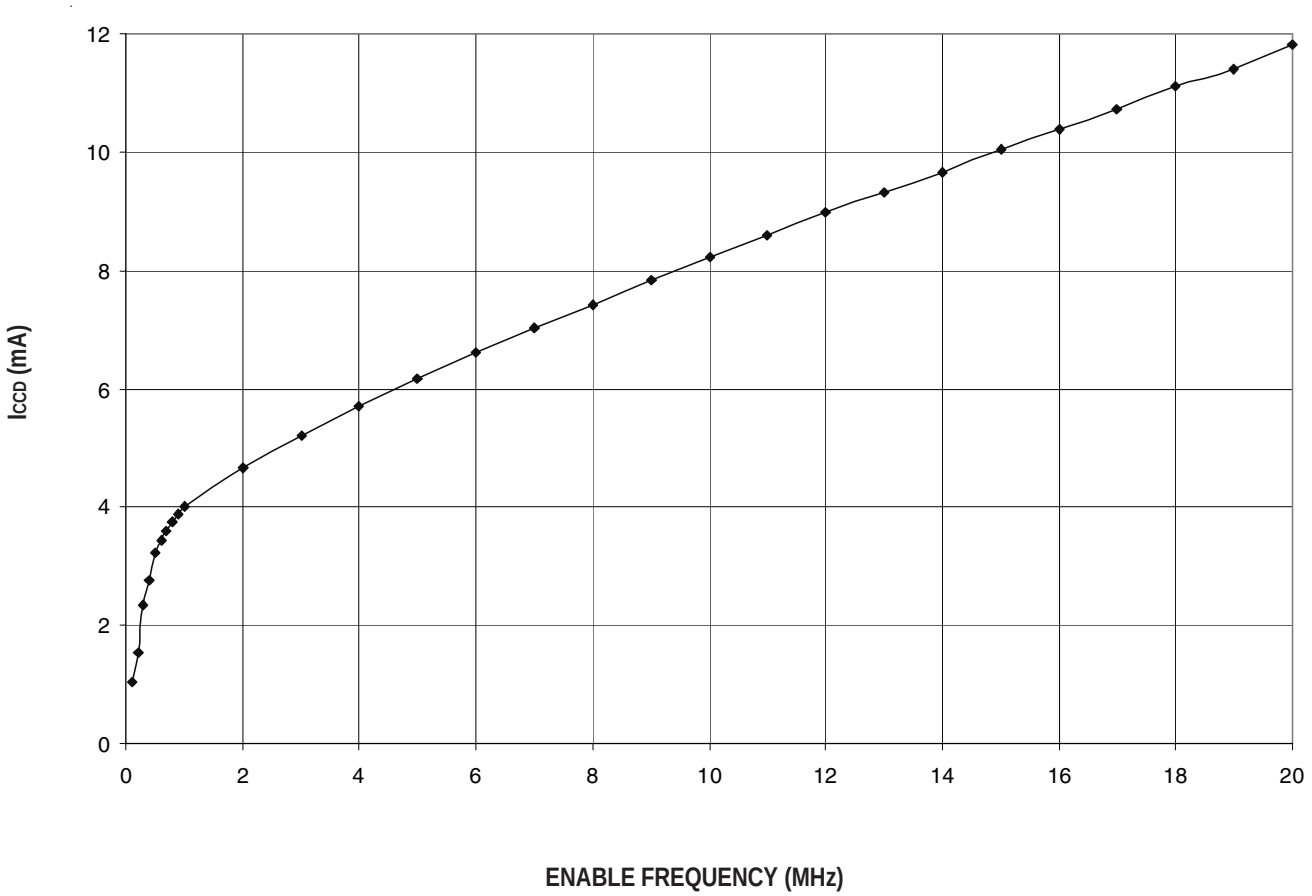


POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min.	Typ.	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	—	8	16	mA
ΔI_{CC}	Power Supply Current [2,3] per Input HIGH	V_{CC} = Max., V_{IN} = 3V, f = 0 per Control Input	—	—	30	µA
I_{CCD}	Dynamic Power Supply Current per Output Enable Control Input[4]	V_{CC} = 3.3V, A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle	See Typical I_{CCD} vs Enable Frequency graph below			

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per input driven at the specified level. A and B pins do not contribute to ΔIcc.
3. This parameter is guaranteed but not tested.
4. This parameter represents the current required to switch internal capacitance at the specified frequency. The A and B inputs do not contribute to the Dynamic Power Supply Current. This parameter is guaranteed but not production tested.

TYPICAL I_{CCD} vs ENABLE FREQUENCY CURVE AT V_{CC} = 3.3V



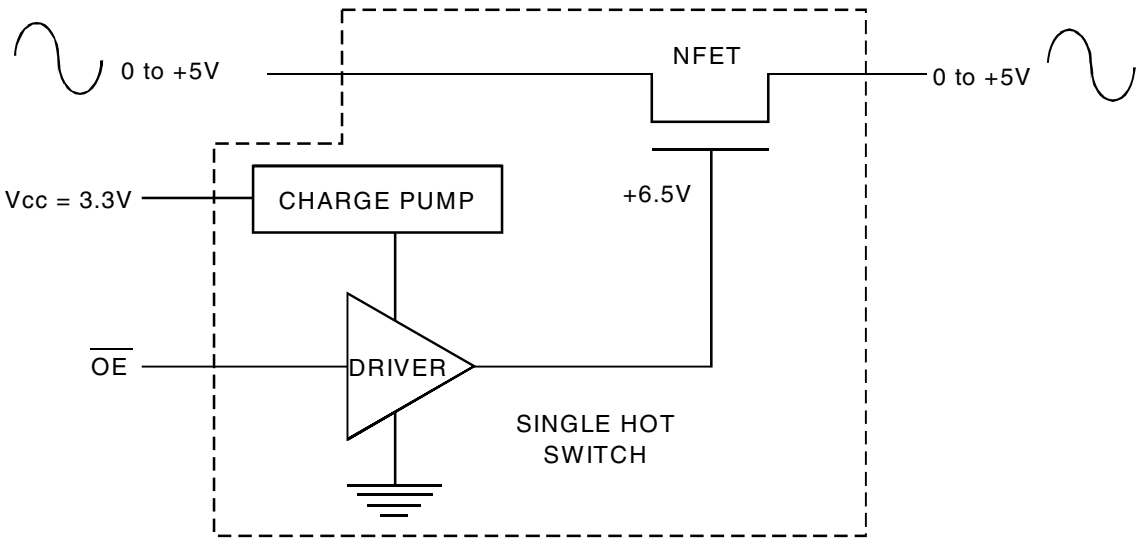
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C

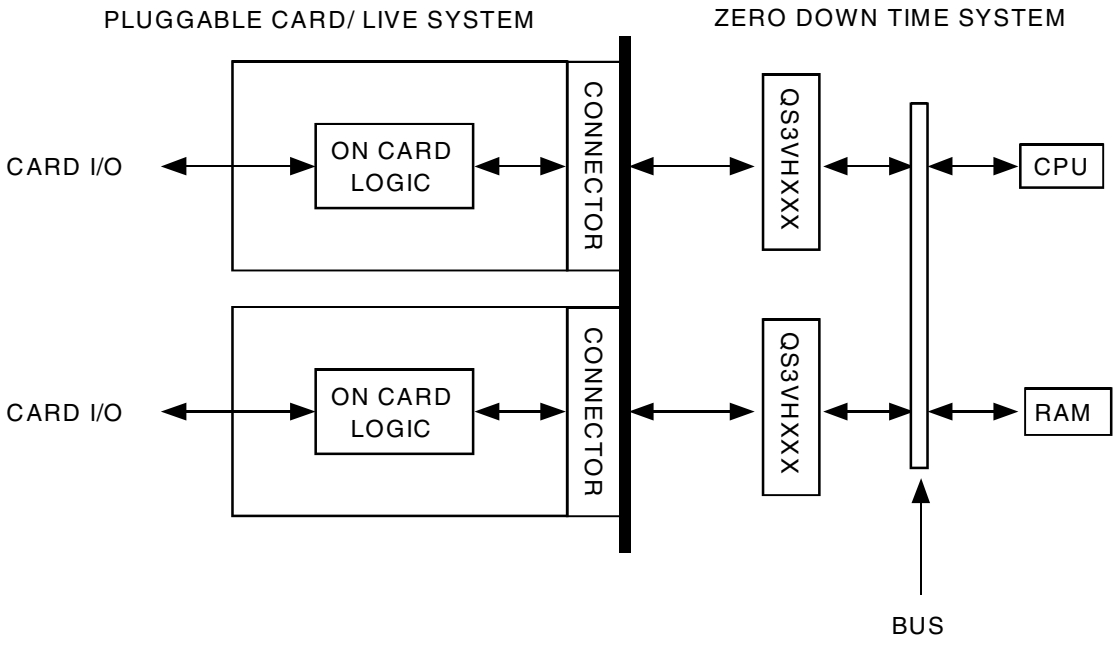
Symbol	Parameter	V_{CC} = 2.5 ± 0.2V (1)		V_{CC} = 3.3 ± 0.3V (1)		Unit
		Min. (4)	Max.	Min. (4)	Max.	
t_{PLH} t_{PHL}	Data Propagation Delay(2,3) Ax to/from Bx	—	0.9	—	1.35	ns
t_{PZL} t_{PZH}	Switch Turn-On Delay $\overline{OE}$x to Ax/Bx	1.5	9	1.5	8	ns
t_{PLZ} t_{PHZ}	Switch Turn-Off Delay $\overline{OE}$x to Ax/Bx	1.5	7.5	1.5	7.5	ns
$f_{\overline{OE}x}$	Operating Frequency - Enable(2,5)	—	10	—	20	MHz

NOTES:
1. See Test Conditions under TEST CIRCUITS AND WAVEFORMS.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 1.35ns at C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Minimums are guaranteed but not production tested.
5. Maximum toggle frequency for $\overline{OE}$x control input (pass voltage > V_{CC}, V_{IN} = 5V, $R_{LOAD} \geq 1M\Omega$, no C_{LOAD}).

SOME APPLICATIONS FOR HOTSWITCH PRODUCTS



Rail-to-Rail Switching

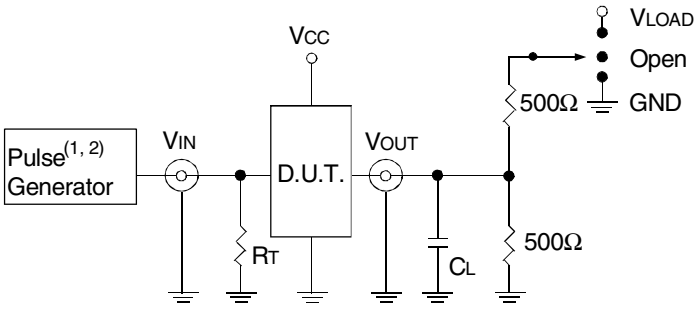


Hot-Swapping

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V ± 0.3V	$V_{CC}^{(2)}$= 2.5V ± 0.2V	Unit
V_{LOAD}	6	2 x Vcc	V
V_{IH}	3	Vcc	V
V_T	1.5	Vcc/2	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
C_L	50	30	pF



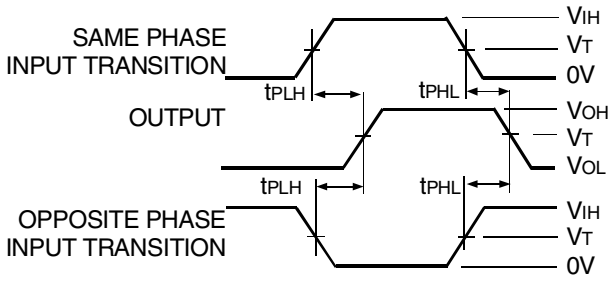
Test Circuits for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

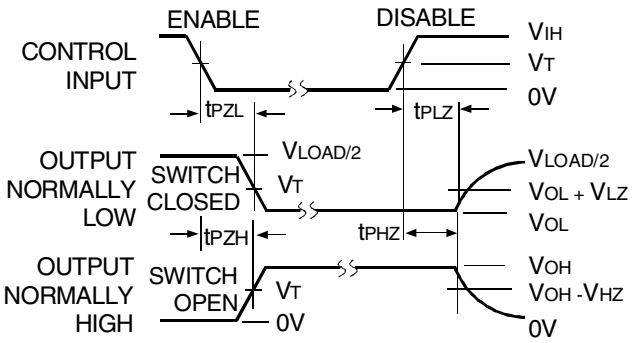
NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open



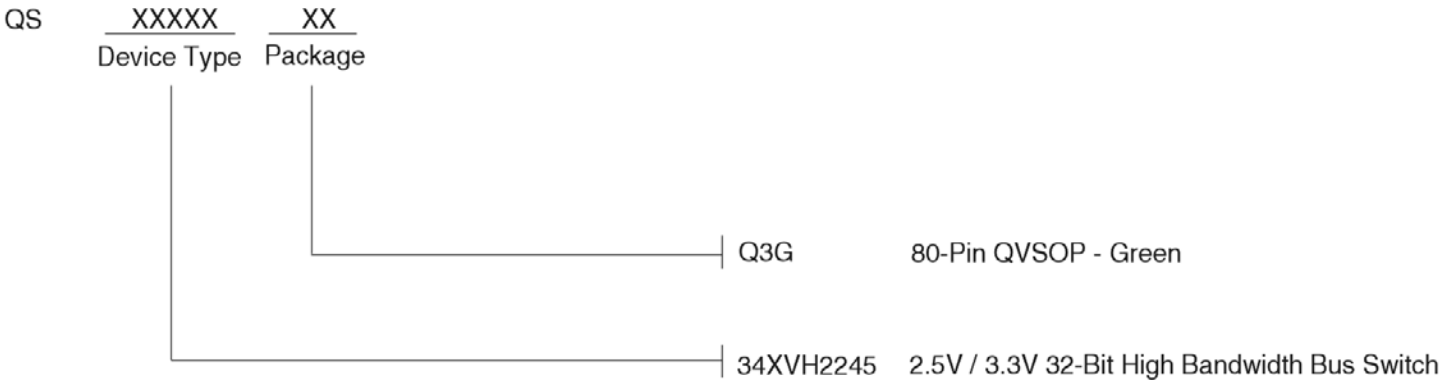
Propagation Delay



NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

ORDERING INFORMATION



Datasheet Document History

09/01/08	Pg. 4, 8	Revise I_{CCQ} Typ. and Max. Remove non green package version and updated the ordering information by removing the "IDT" notation.

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