

QUAD 2 CHANNEL MULTIPLEXER

- HIGH SPEED: $t_{PD} = 4.1 \text{ ns (TYP.)}$ at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A (MAX.)}$ at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 157
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.8V \text{ (MAX.)}$

DESCRIPTION

The 74VHC157 is an advanced high-speed CMOS QUAD 2-CHANNEL MULTIPLEXER fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It consists of four 2-input digital multiplexer with common select and strobe inputs. It is a non-inverting multiplexer. When the STROBE

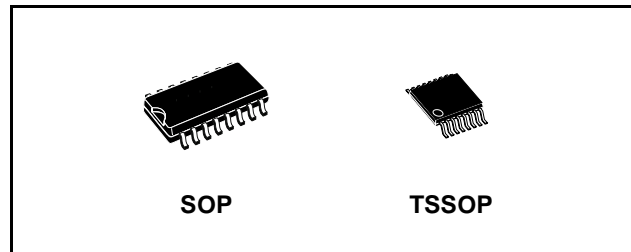


Table 1: Order Codes

PACKAGE	T & R
SOP	74VHC157MTR
TSSOP	74VHC157TTR

input is held high selection of data is inhibited and all the outputs become low. The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs. Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

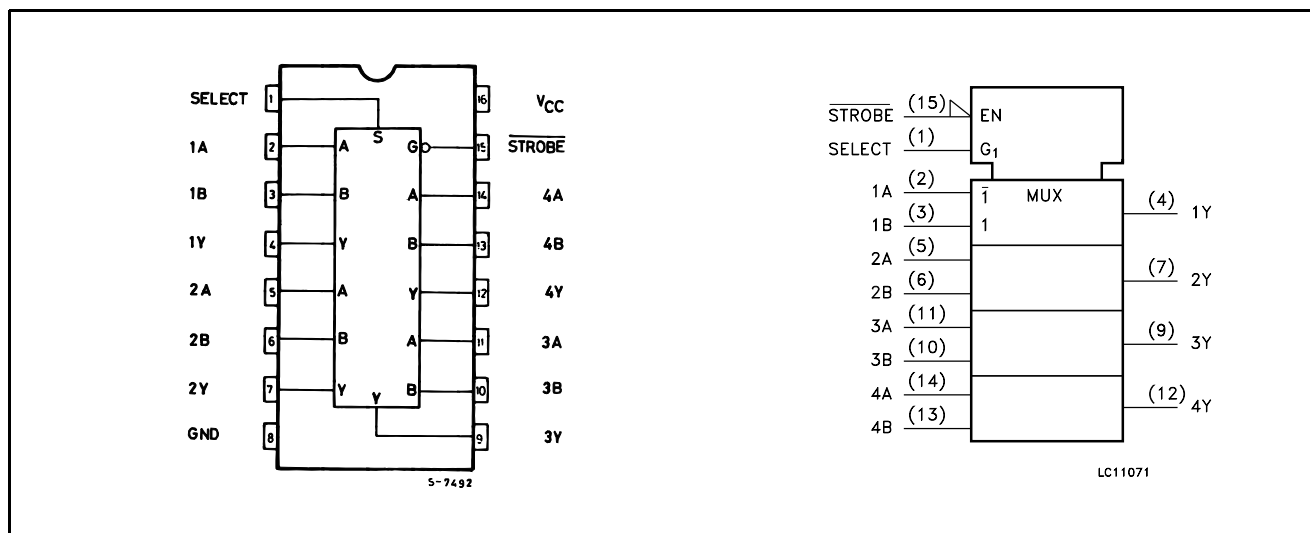


Figure 2: Input Equivalent Circuit

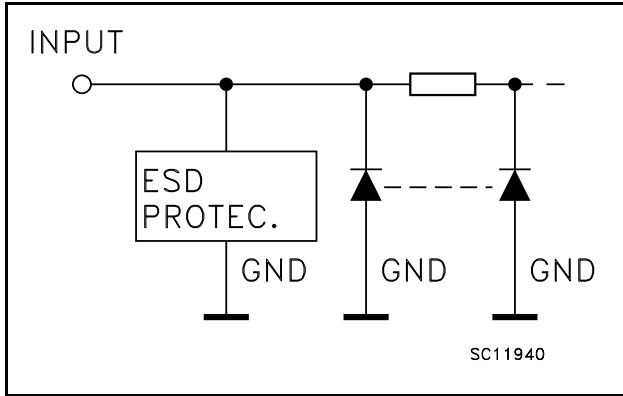


Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Inputs
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	Multiplexer Outputs
15	$\overline{\text{STROBE}}$	Strobe Input
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUTS				OUTPUT
$\overline{\text{STROBE}}$	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't care

Figure 3: Logic Diagram

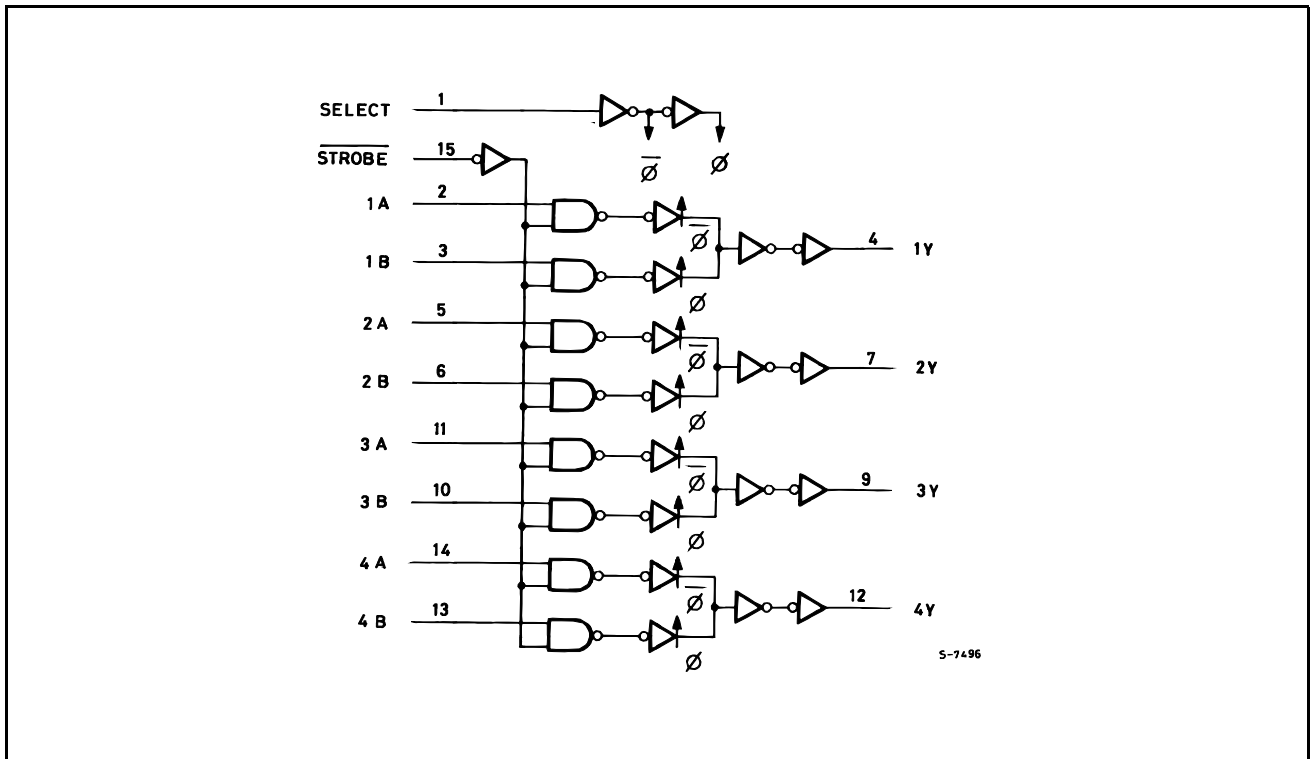


Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1) ($V_{CC} = 3.3 \pm 0.3V$) ($V_{CC} = 5.0 \pm 0.5V$)	0 to 100 0 to 20	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0 to 5.5		0.7V _{CC}			0.7V _{CC}		0.7V _{CC}		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0 to 5.5				0.3V _{CC}		0.3V _{CC}		0.3V _{CC}	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		4.5	I _O =-50 μA	4.4	4.5		4.4		4.4		
		3.0	I _O =-4 mA	2.58			2.48		2.4		
		4.5	I _O =-8 mA	3.94			3.8		3.7		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
		4.5	I _O =8 mA			0.36		0.44		0.55	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		40	μA

Table 7: AC Electrical Characteristics (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)	C _L (pF)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time A, B to Y	3.3 ^(*)	15		6.2	9.7	1.0	11.5	1.0	11.5	ns
		3.3 ^(*)	50		8.7	13.2	1.0	15.0	1.0	15.0	
		5.0 ^(**)	15		4.1	6.4	1.0	7.5	1.0	7.5	
		5.0 ^(**)	50		5.6	8.4	1.0	9.5	1.0	9.5	
t _{PLH} t _{PHL}	Propagation Delay Time SELECT to Y	3.3 ^(*)	15		8.4	13.2	1.0	15.5	1.0	15.5	ns
		3.3 ^(*)	50		10.9	16.7	1.0	19.0	1.0	19.0	
		5.0 ^(**)	15		5.3	8.1	1.0	9.5	1.0	9.5	
		5.0 ^(**)	50		6.8	10.1	1.0	11.5	1.0	11.5	
t _{PLH} t _{PHL}	Propagation Delay Time STROBE to Y	3.3 ^(*)	15		8.7	13.6	1.0	16.0	1.0	16.0	ns
		3.3 ^(*)	50		11.2	17.1	1.0	19.5	1.0	19.5	
		5.0 ^(**)	15		5.6	8.6	1.0	10.0	1.0	10.0	
		5.0 ^(**)	50		7.1	10.6	1.0	12.0	1.0	12.0	

(*) Voltage range is 3.3V ± 0.3V

(**) Voltage range is 5.0V ± 0.5V

Table 8: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value						Unit
				T _A = 25°C			-40 to 85°C		-55 to 125°C	
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
C _{IN}	Input Capacitance		6	10		10		10	pF	
C _{PD}	Power Dissipation Capacitance (note 1)		18						pF	

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/4 (per channel)

Table 9: Dynamic Switching Characteristics

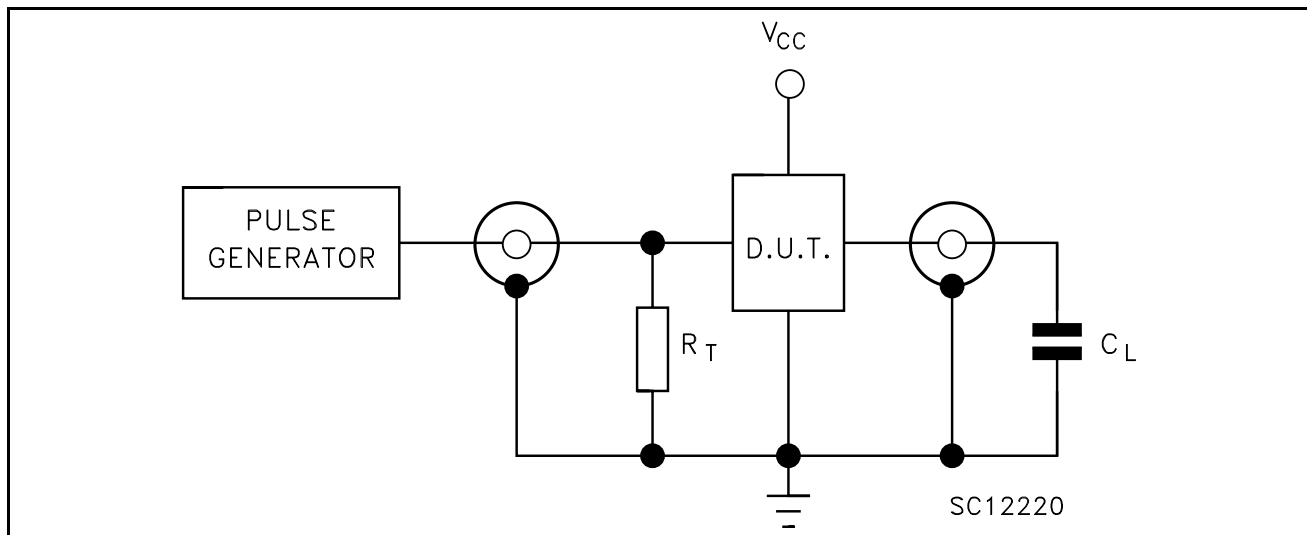
Symbol	Parameter	Test Condition		Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
		V _{CC} (V)		Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50 pF		0.3	0.8					V
V _{OLV}				-0.8	-0.3						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		3.5						V	
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				1.5				V	

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Figure 4: Test Circuit



C_L = 15/50pF or equivalent (includes jig and probe capacitance)
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 5: Waveform - Propagation Delays For Inverting Conditions

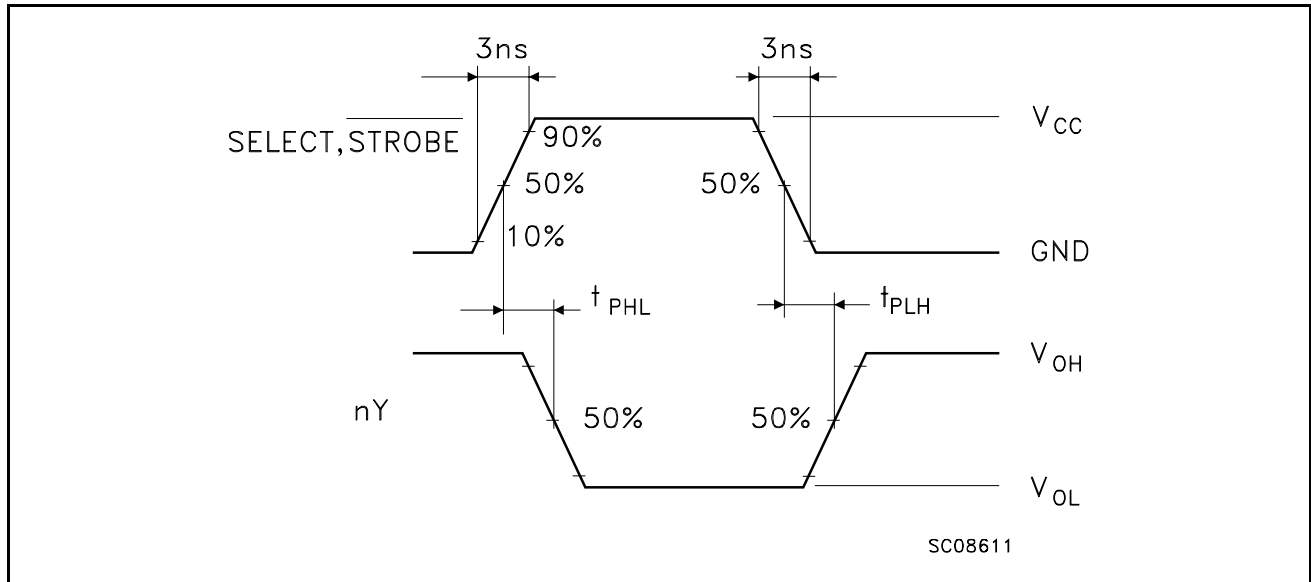
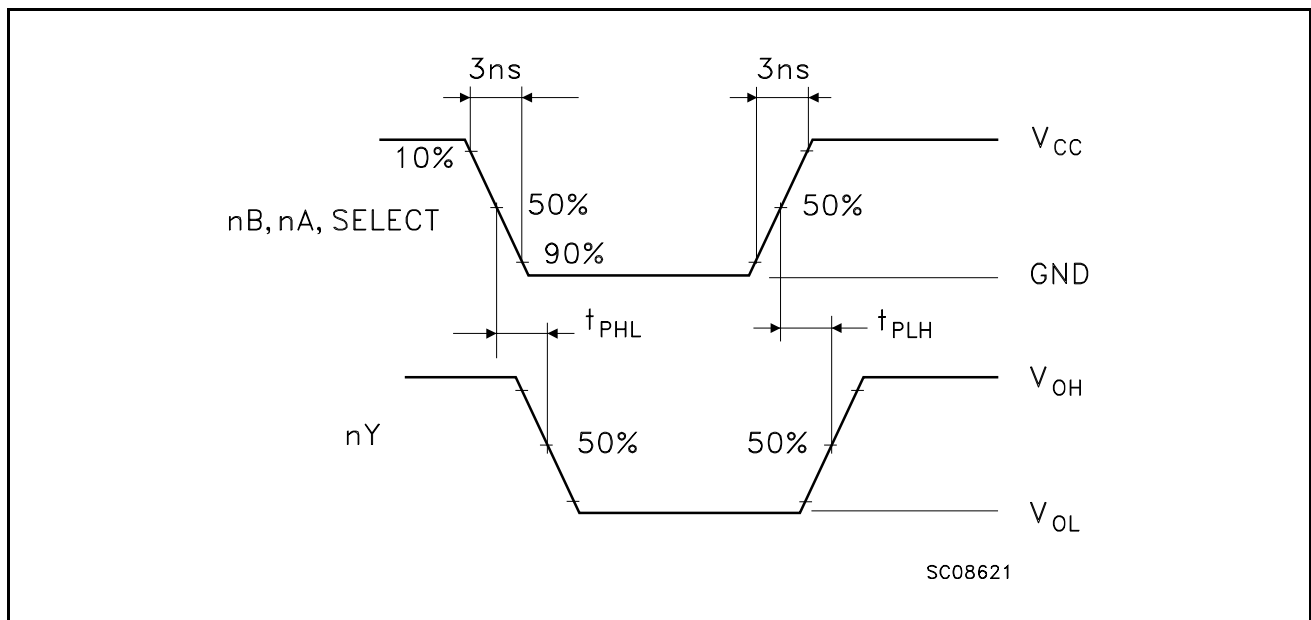
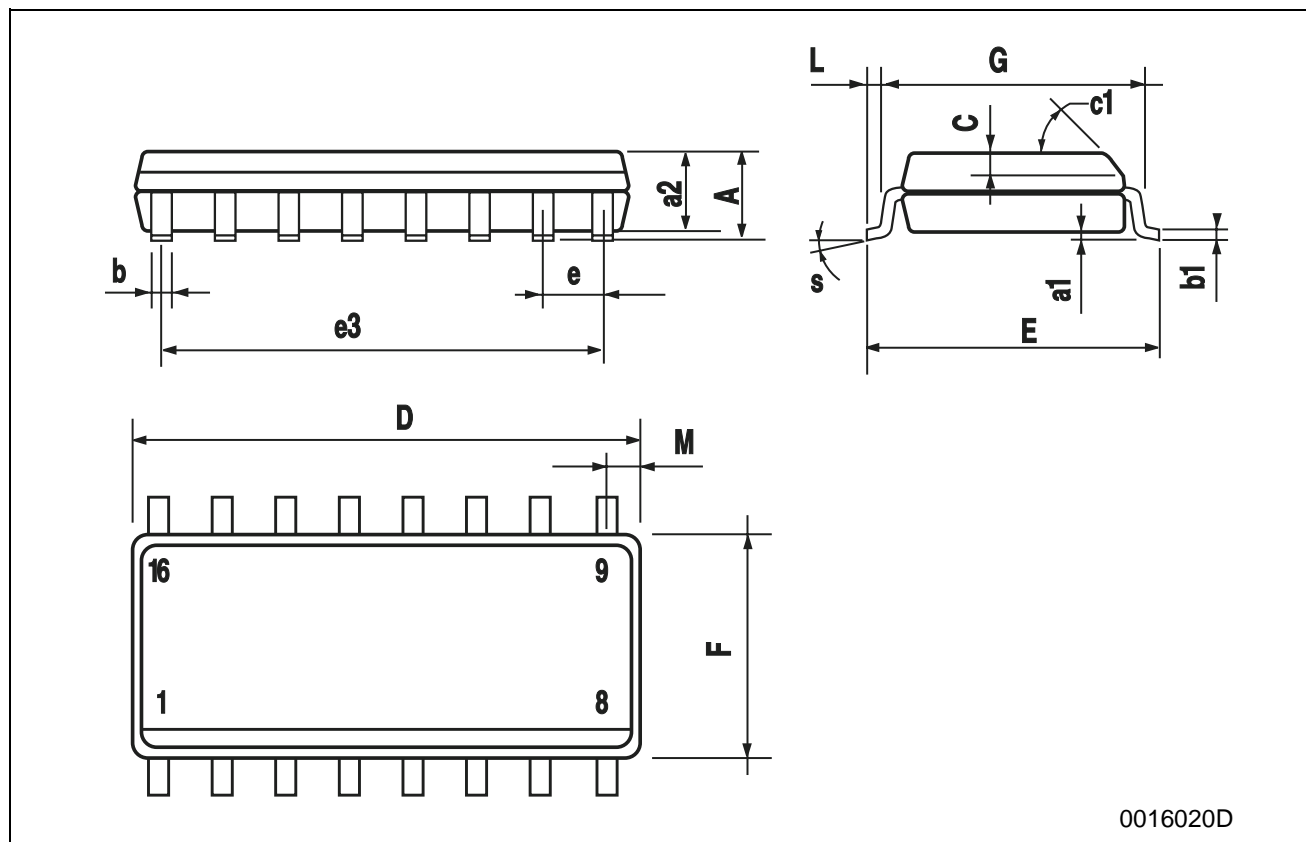


Figure 6: Waveform - Propagation Delays For Non-inverting Conditions



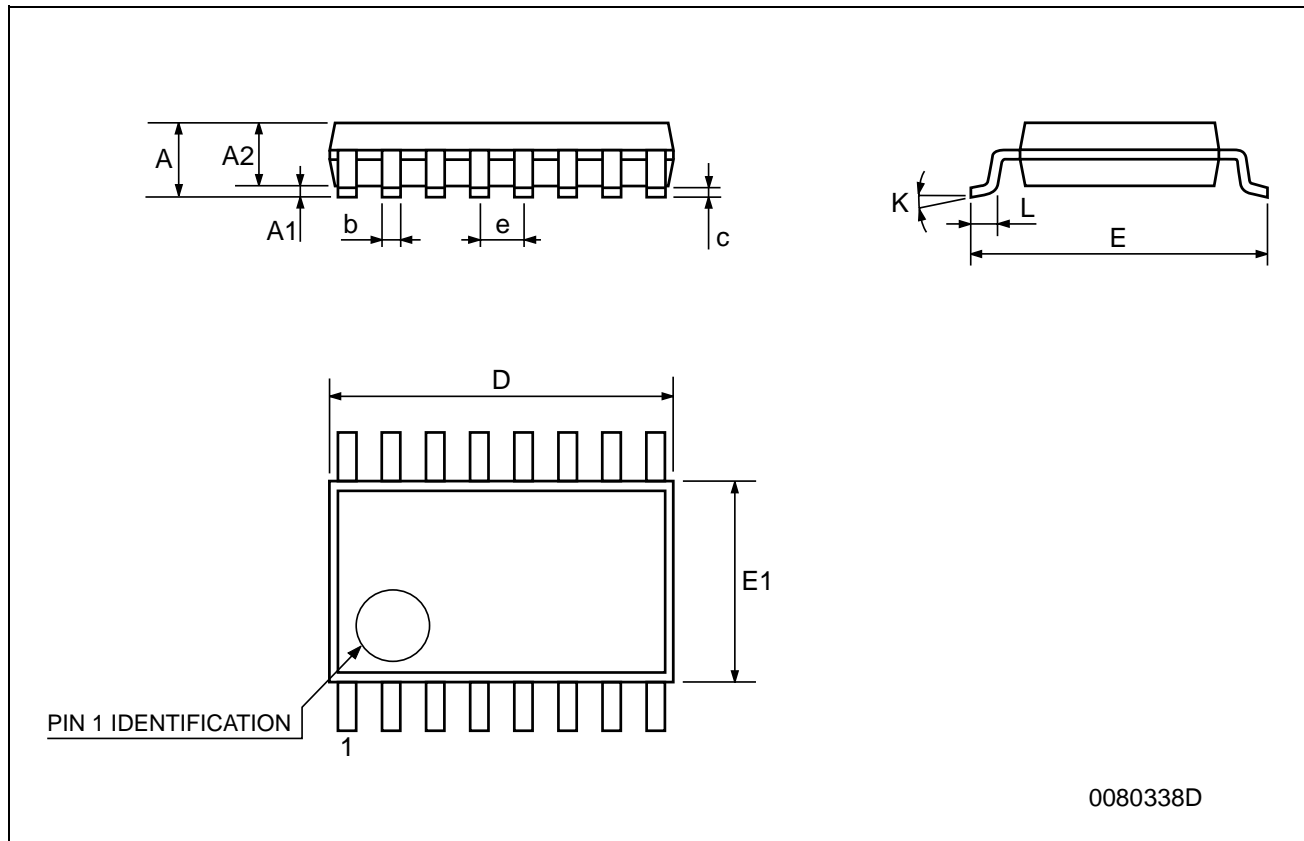
SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



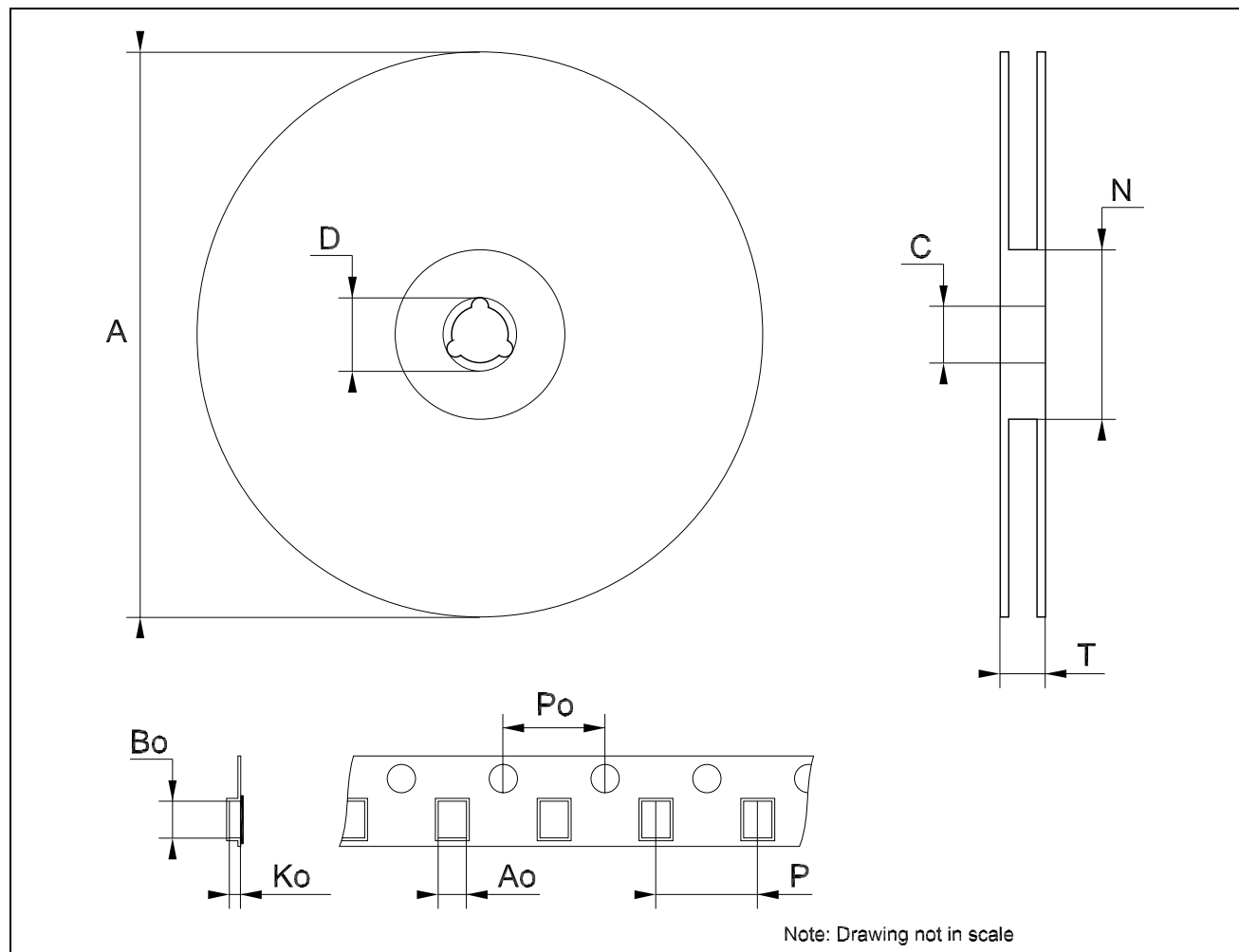
TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Tape & Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

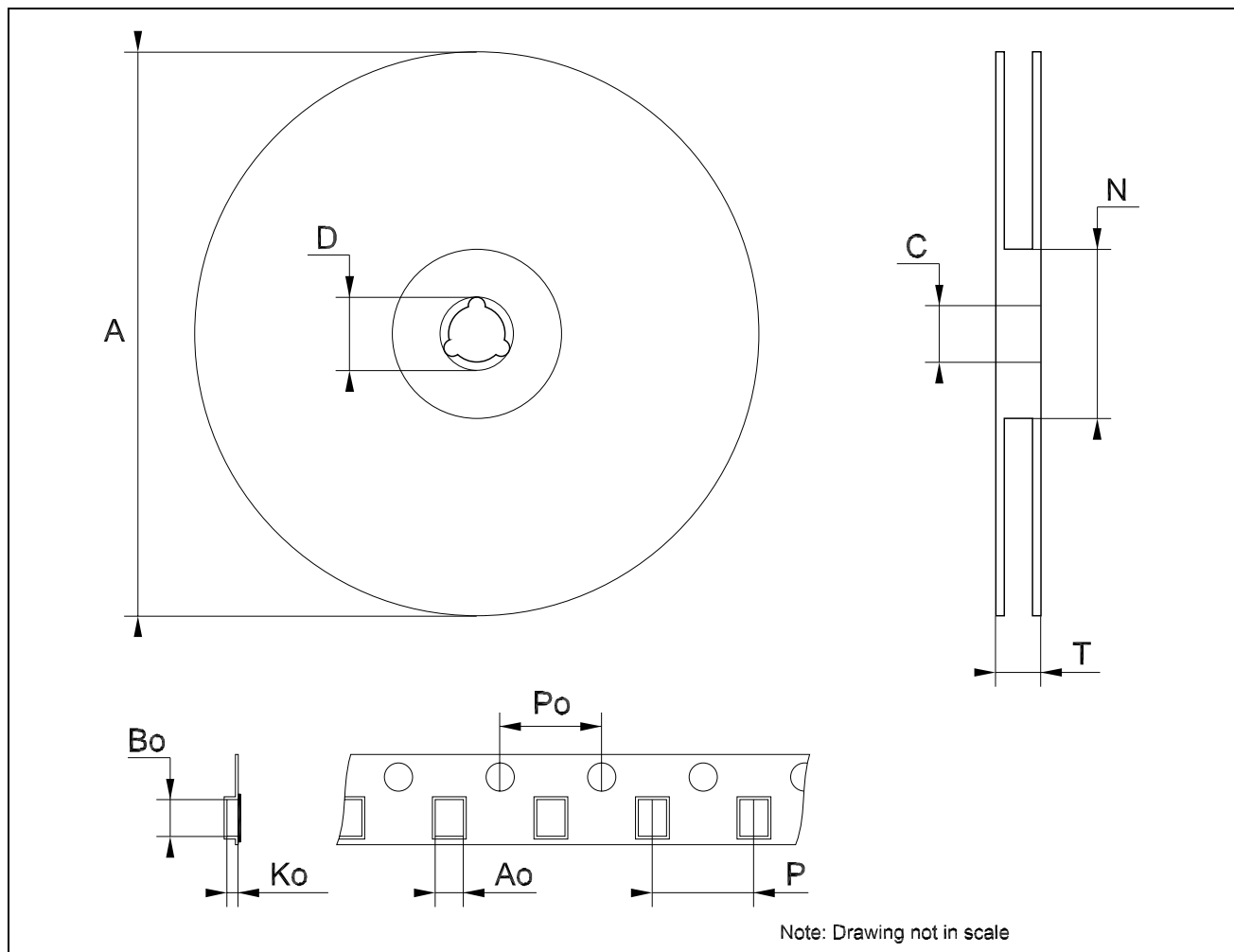


Table 10: Revision History

Date	Revision	Description of Changes
12-Nov-2004	4	Order Codes Revision - pag. 1.

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