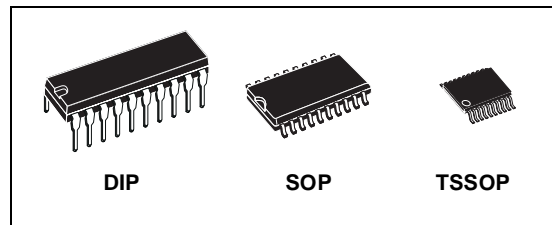




# 74ACT299

## 8 BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

- HIGH SPEED:  
 $f_{MAX} = 240\text{MHz}$  (TYP.) at  $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 8\mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS  
 $V_{IH} = 2\text{V}$  (MIN.),  $V_{IL} = 0.8\text{V}$  (MAX.)
- $50\Omega$  TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24\text{mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 299
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	74ACT299B	
SOP	74ACT299MTR	74ACT299MTR
TSSOP		74ACT299TTR

### DESCRIPTION

The 74ACT299 is an advanced high-speed CMOS 8-BIT PIPO SHIFT REGISTER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

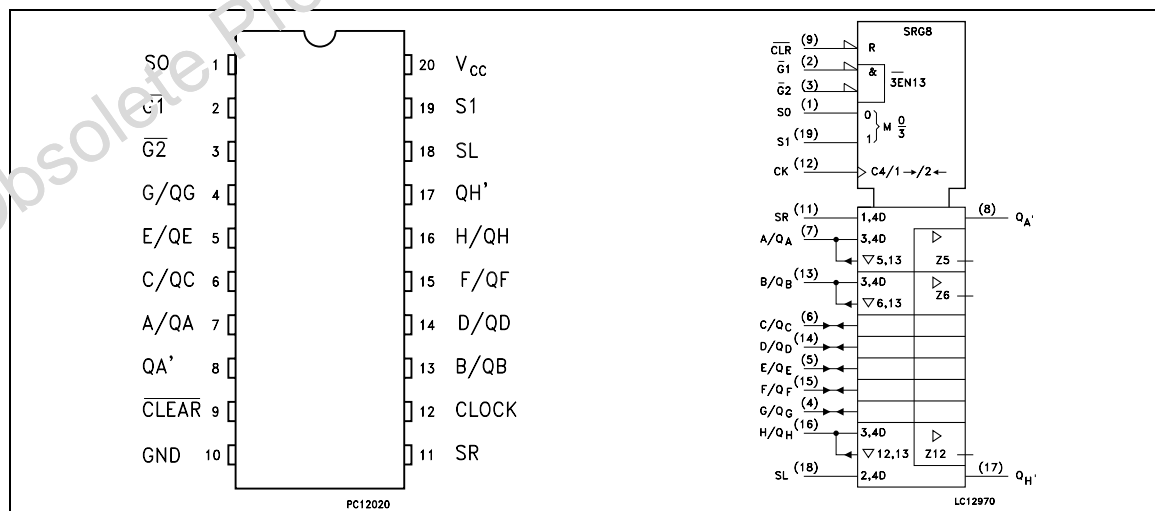
These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1) as shown in the Truth Table. When one or

both enable inputs, ( $\overline{G1}$ ,  $\overline{G2}$ ) are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected. Clear function is asynchronous to clock.

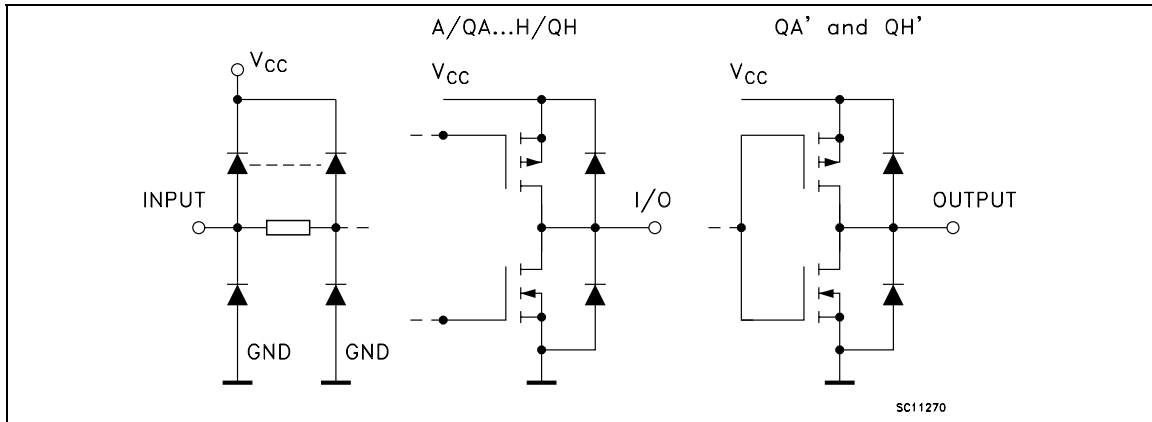
The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 19	S0, S1	Mode Select Inputs
2, 3	G1, G2	3-State Output Enable Inputs (Active LOW)
7, 13, 6, 14, 5, 15, 4, 16	A/QA to H/QH	Parallel Data Inputs or 3-State Parallel Outputs (Bus Driver)
8, 17	QA' to QH'	Serial Outputs (Standard Output)
9	CLEAR	Asynchronous Master Reset Input (Active LOW)
11	SR	Serial Data Shift Right Input
12	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
18	SL	Serial Data Shift Left Input
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

MODE	INPUTS						INPUTS/OUTPUTS				OUTPUTS	
	CLEAR	FUNCTION SELECTED		OUTPUT CONTROL		CLOCK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	G1*	G2*		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	┌	X	H	H	QGn	H	QGn
	H	L	H	L	L	┌	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	┌	H	X	QBn	H	QBn	H
	H	H	L	L	L	┌	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	┌	X	X	a	h	a	h

\* : When one or both controls are high, the eight input/output terminals are the high impedance state: however sequential operation or cleaning of the register is not affected.

Z : High Impedance

Qn0 : The level of An before the indicated steady state input conditions were established.

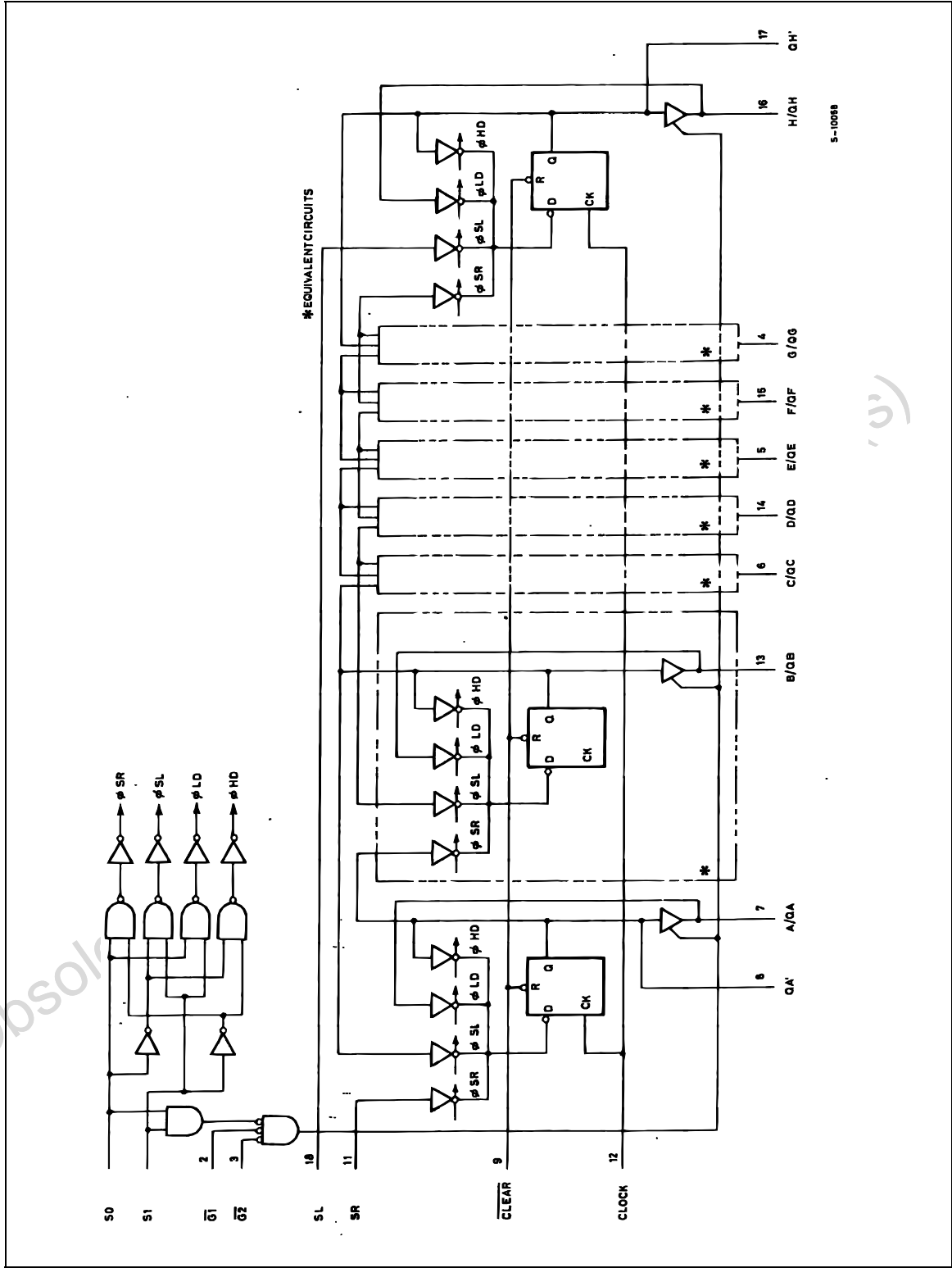
Qnn : The level of Qn before the most recent active transition indicated by OR

a, h : The level of the steadystate inputs A, H, respectively.

X : Don't Care



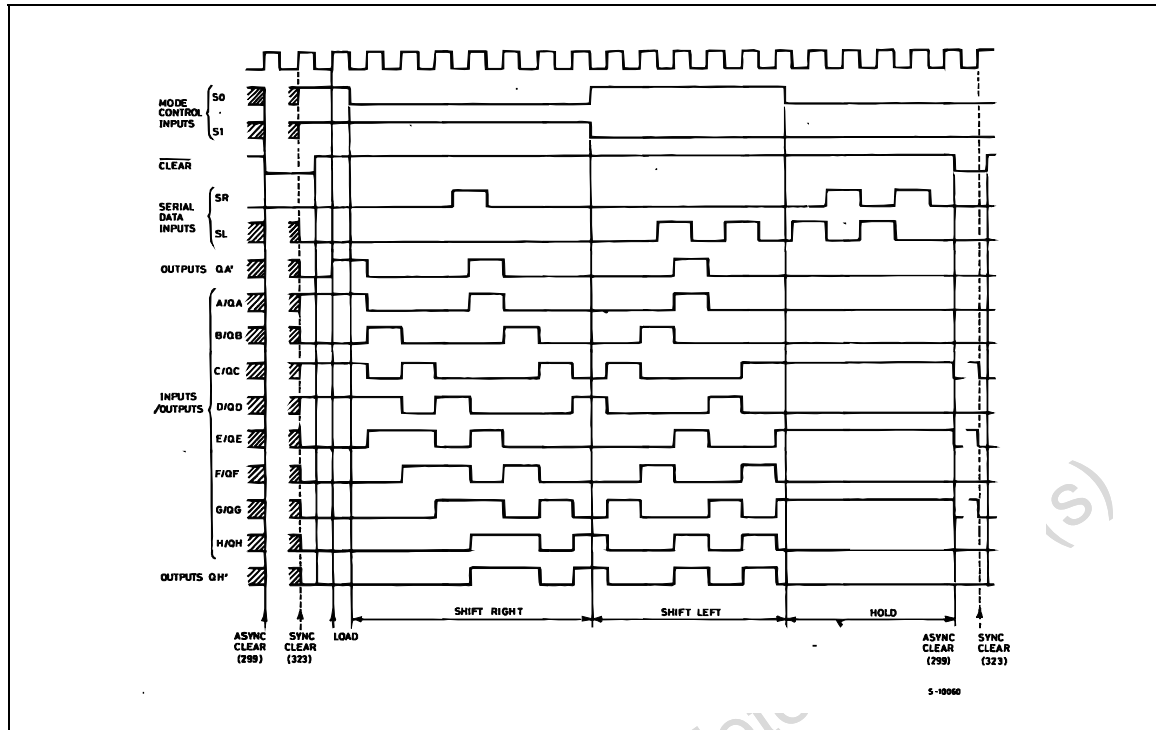
LOGIC DIAGRAM



Obsol



## TIMING CHART



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 400$	mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}\text{C}$
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to $5.5\text{V}$ (note 1)	8	ns/V

1)  $V_{IN}$  from 0.8V to 2.0V

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V	2.0	1.5		2.0		2.0		V
		5.5		2.0	1.5		2.0		2.0		
V <sub>IL</sub>	Low Level Input Voltage	4.5	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V		1.5	0.8		0.8		0.8	V
		5.5			1.5	0.8		0.8		0.8	
V <sub>OH</sub>	High Level Output Voltage	4.5	I <sub>O</sub> =-50 μA	4.4	4.49		4.4		4.4		V
		5.5	I <sub>O</sub> =-50 μA	5.4	5.49		5.4		5.4		
		4.5	I <sub>O</sub> =-24 mA	3.86			3.76		3.7		
		5.5	I <sub>O</sub> =-24 mA	4.86			4.76		4.7		
V <sub>OL</sub>	Low Level Output Voltage	4.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	V
		5.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
		5.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>OZ</sub>	High Impedance Output Leakage Current	5.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND			± 0.5		± 5		± 10	μA
I <sub>CCT</sub>	Max I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V		0.6			1.5		1.6	mA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			8		80		160	μA
I <sub>OLD</sub>	Dynamic Output Current (note 1, 2)	5.5	V <sub>OLD</sub> = 1.65 V max					75		50	mA
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF,  $R_L = 500$   $\Omega$ , Input  $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Condition	Value								Unit
			$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time CLOCK to $Q'_A$ $Q'_H$	5.0(*)		6.5	10.5	1.0	15.0	1.0	16.0	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time CLOCK to $Q_A$ - $Q_H$	5.0(*)		6.5	11.4	1.0	15.0	1.0	16.0	ns	
$t_{PHL}$	Propagation Delay Time CLEAR to $Q'_A$ $Q'_H$	5.0(*)		6.4	10.0	1.0	17.5	1.0	18.0	ns	
$t_{PHL}$	Propagation Delay Time CLEAR to $Q_A$ - $Q_H$	5.0(*)		6.6	10.5	1.0	17.5	1.0	18.0	ns	
$t_{PZL}$ $t_{PZH}$	Output Enable Time	5.0(*)		6.4	11.4	1.0	13.5	1.0	14.5	ns	
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time	5.0(*)		6.2	9.6	1.0	13.5	1.0	14.5	ns	
$t_W$	CLEAR Pulse Width, LOW	5.0(*)			5.0		5.0		5.0	ns	
$t_W$	CLOCK pulse Width	5.0(*)			5.0		5.0		5.0	ns	
$t_s$	Setup Time HIGH or LOW (S0 or S1 to CK)	5.0(*)			6.0		6.5		6.5	ns	
$t_h$	Hold Time HIGH or LOW (S0 or S1 to CK)	5.0(*)			0.0		0.0		0.0	ns	
$t_s$	Setup Time HIGH or LOW (SR or SL to CK)	5.0(*)			3.5		3.5		3.5	ns	
$t_h$	Hold Time HIGH or LOW (SR or SL to CK)	5.0(*)			2.0		2.0		2.0	ns	
$t_{REM}$	Recovery Time CLR to CK	5.0(*)			2.0		2.0		2.0	ns	
$f_{MAX}$	Maximum Clock Frequency	5.0(*)		80	240		80		80	MHz	

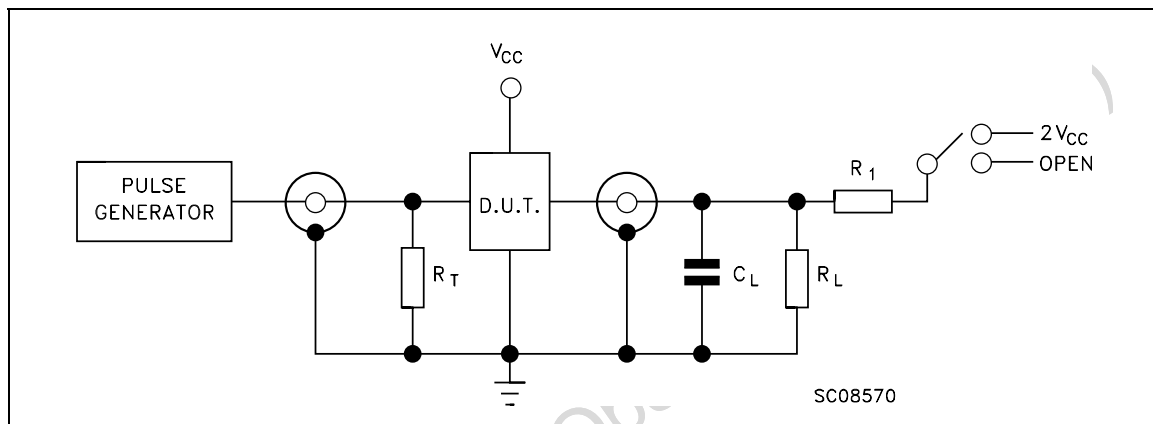
(\*) Voltage range is 5.0V  $\pm$  0.5V

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
				T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
		V <sub>CC</sub> (V)		Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	5.0			4	10		10		10	pF
C <sub>I/O</sub>	I/O Capacitance	5.0			13						pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	5.0	f <sub>IN</sub> = 10MHz		160						pF

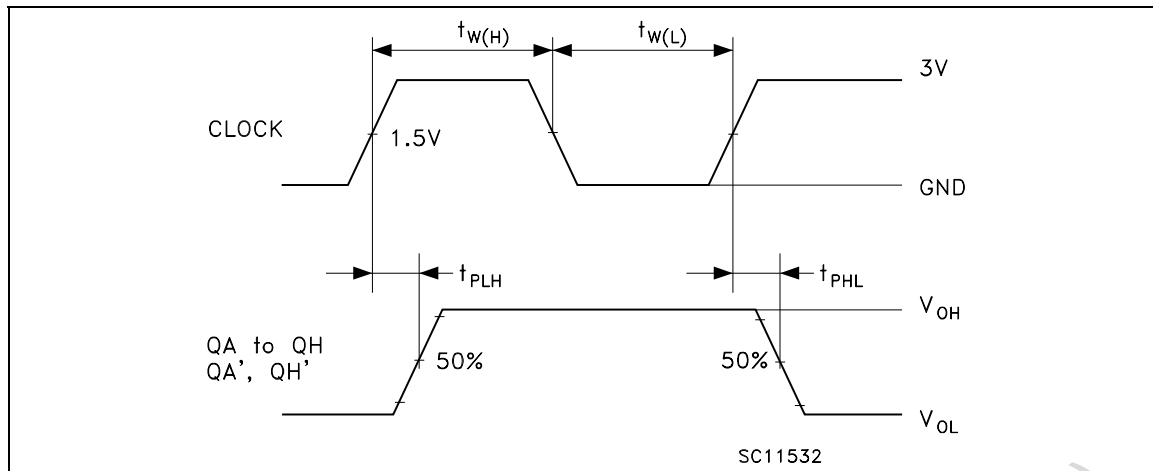
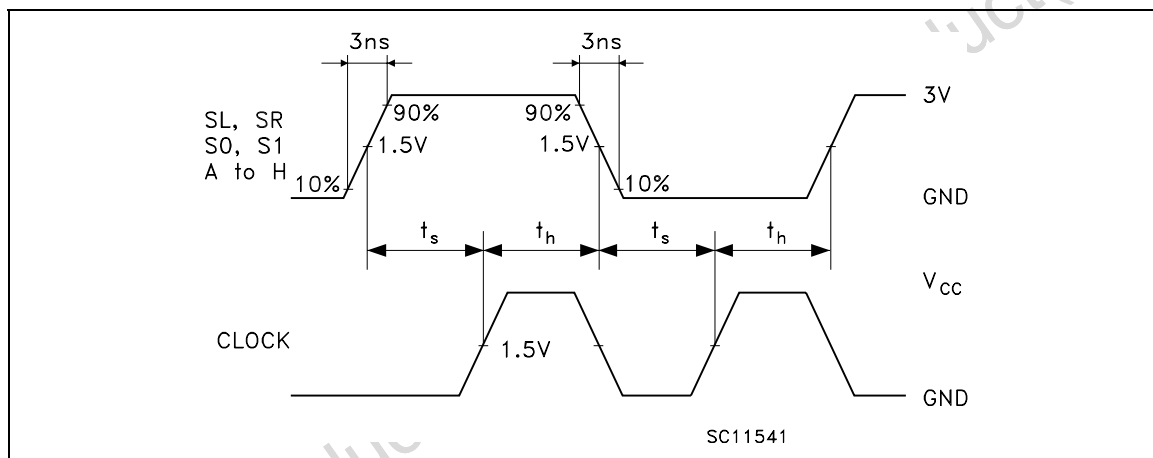
1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(oper)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC/n</sub> (per circuit)

## TEST CIRCUIT

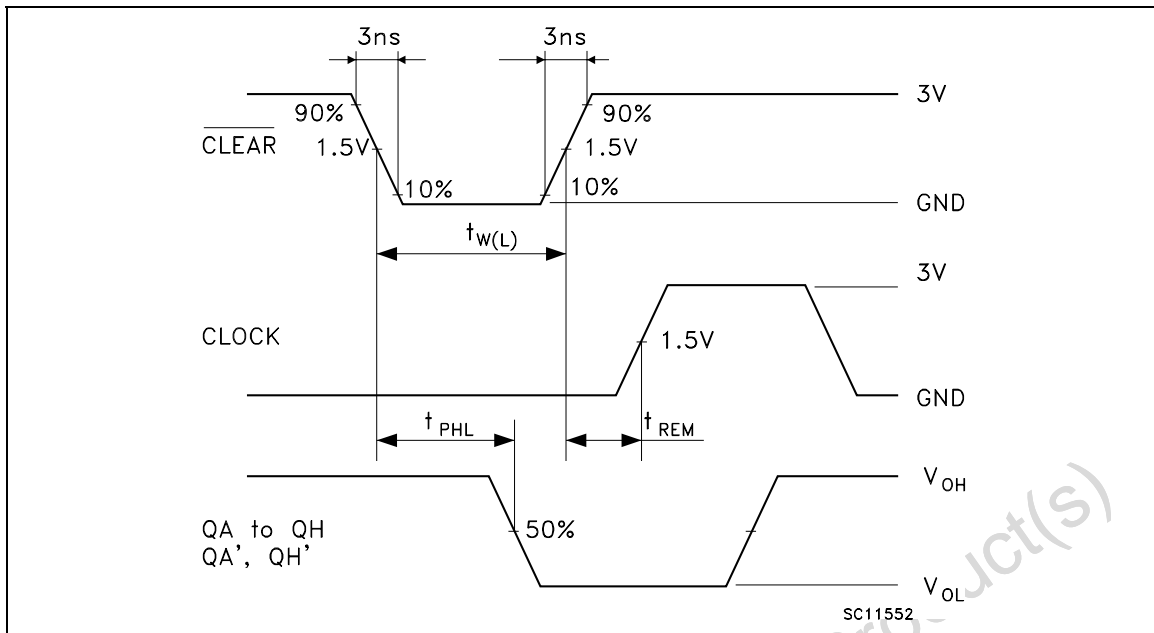
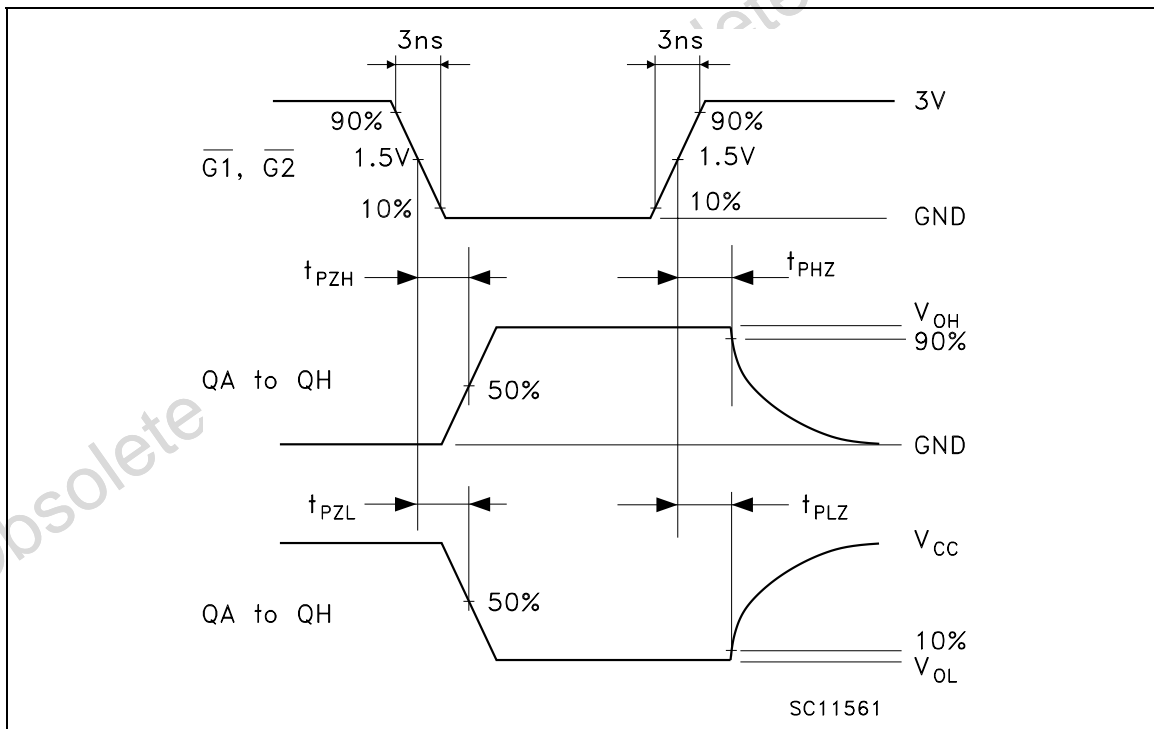


TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	2V <sub>CC</sub>
t <sub>PZH</sub> , t <sub>PHZ</sub>	Open

C<sub>L</sub> = 50pF or equivalent (includes jig and probe capacitance)  
R<sub>L</sub> = R<sub>1</sub> = 500Ω or equivalent  
R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

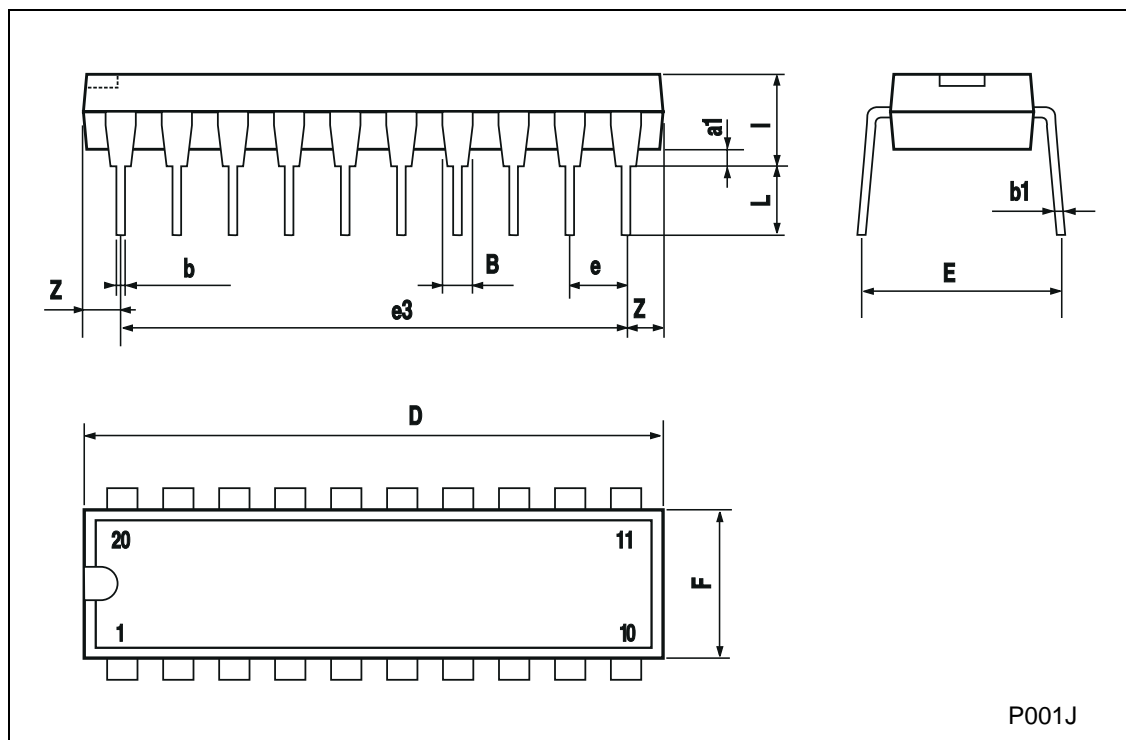
**WAVEFORM 1: PROPAGATION DELAYS** (f=1MHz; 50% duty cycle)**WAVEFORM 2: PROPAGATION DELAYS** (f=1MHz; 50% duty cycle)



**WAVEFORM 3: PROPAGATION DELAYS** (f=1MHz; 50% duty cycle)**WAVEFORM 4: PROPAGATION DELAYS** (f=1MHz; 50% duty cycle)

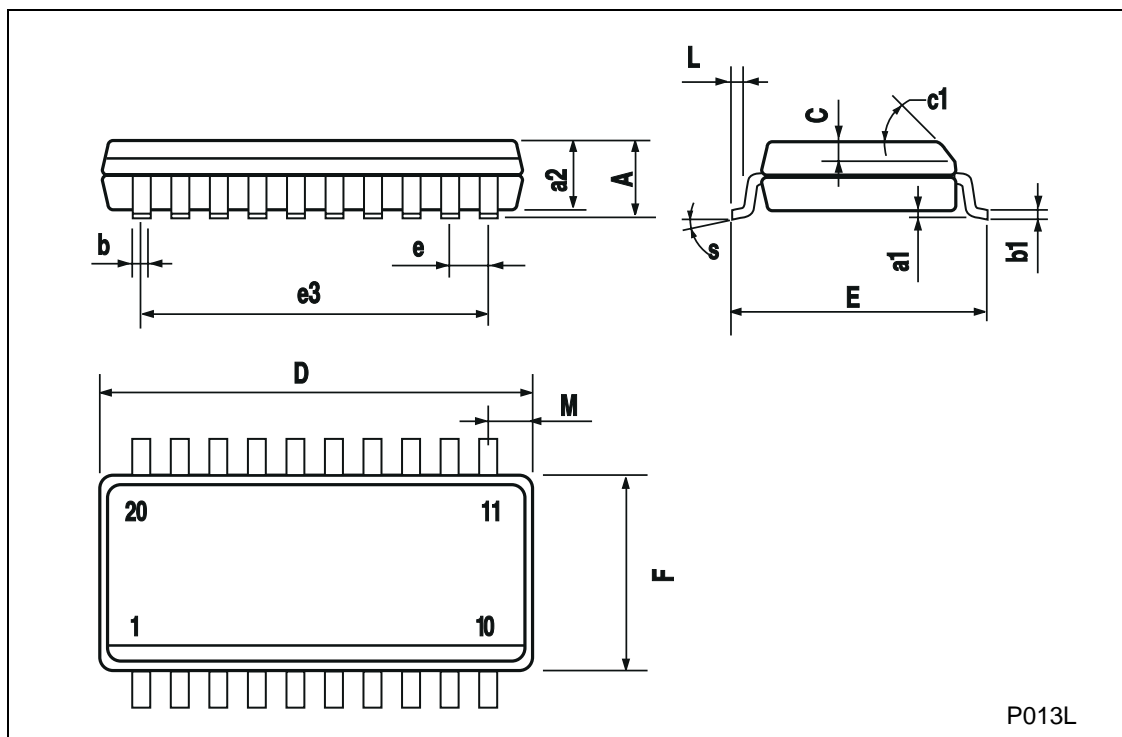
## Plastic DIP-20 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
l			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



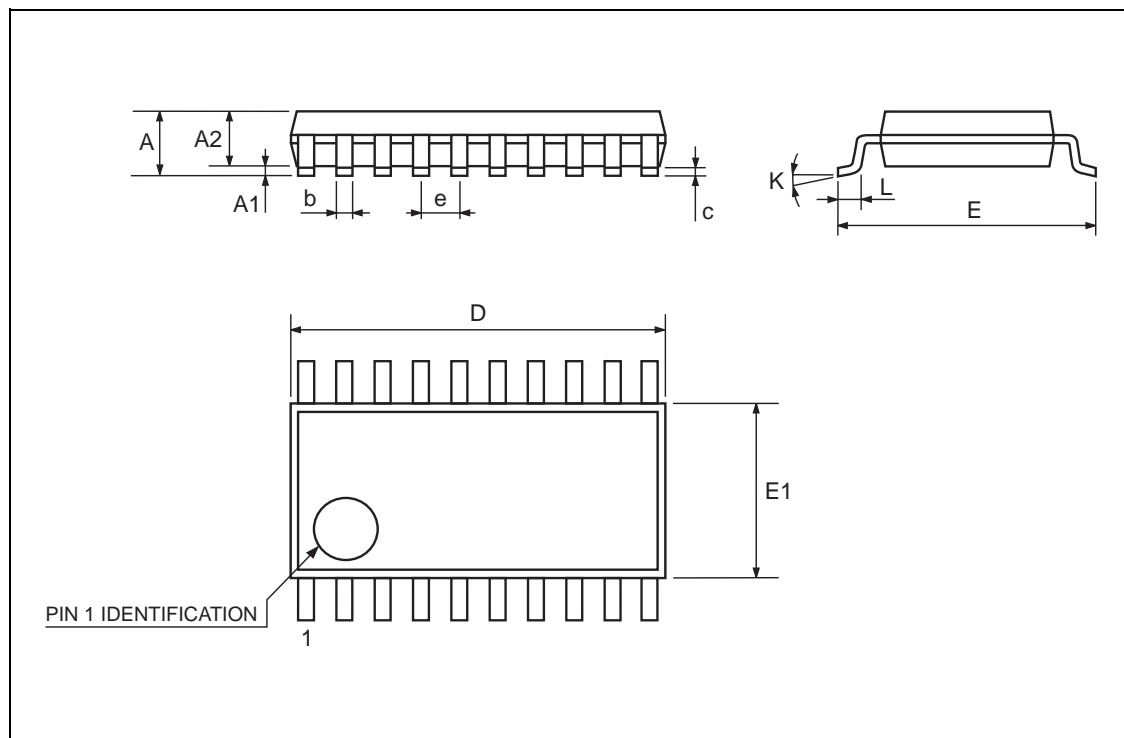
## SO-20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



## TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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