FAIRCHILD SEMICONDUCTOR™

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# DM74LS123
# Dual Retriggerable One-Shot with Clear and Complementary Outputs

## General Description

The DM74LS123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading edge or trailing edge triggering. Pin (A) is an active-LOW transition trigger input and pin (B) is an active-HIGH transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components. The clear input also serves as a trigger input when it is pulsed with a low level pulse transition (⌐‾|_). To obtain the best trouble free operation from this device please read the operating rules as well as the Fairchild Semiconductor one-shot application notes carefully and observe recommendations.

## Features

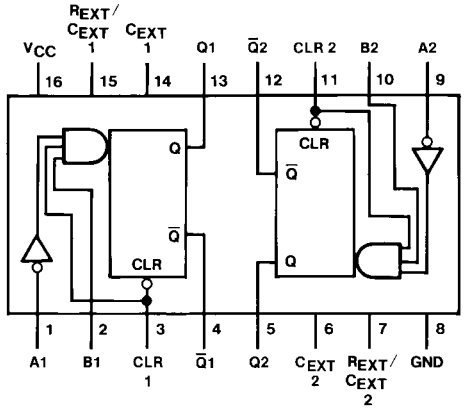
- DC triggered from active-HIGH transition or active-LOW transition inputs
- Retriggerable to 100% duty cycle
- Compensated for $V_{CC}$ and temperature variations
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74LS123M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74LS123SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74LS123N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




## Function Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| CLEAR | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⌐‾| | ⌐‾| |
| H | ↓ | H | ⌐‾| | ⌐‾| |
| ↑ | L | H | ⌐‾| | ⌐‾| |

H = HIGH Logic Level
L = LOW Logic Level
X = Can Be Either LOW or HIGH
↑ = Positive Going Transition
↓ = Negative Going Transition
⌐‾| = A Positive Pulse
⌐‾| = A Negative Pulse

## Functional Description

The basic output pulse width is determined by selection of an external resistor ($R_X$) and capacitor ($C_X$). Once triggered, the basic pulse width may be extended by retriggering the gated active-LOW transition or active-HIGH transition inputs or be reduced by use of the active-LOW or CLEAR input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

## Operating Rules

1. An external resistor ($R_X$) and an external capacitor ($C_X$) are required for proper operation. The value of $C_X$ may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for $C_X$ a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the DM74LS123 one-shot and should not be used. In general the use of the switching diode is not recommended with retriggerable operation.

   Furthermore, if a polarized timing capacitor is used on the DM74LS123 the negative terminal of the capacitor should be connected to the "$C_{EXT}$" pin of the device (Figure 1).

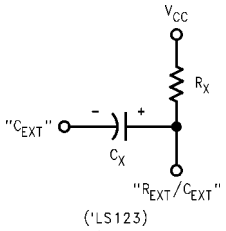



**FIGURE 1.**

3. For $C_X >> 1000$ pF the output pulse width ($t_W$) is defined as follows:

   $t_W = KR_X C_X$

   where [$R_X$ is in kΩ]

   [$C_X$ is in pF]

   [$t_W$ is in ns]

   K ≈ 0.37
4. The multiplicative factor K is plotted as a function of $C_X$ below for design considerations:

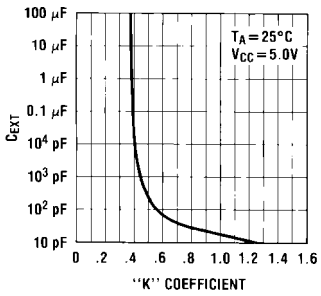



**FIGURE 2.**

5. For $C_X < 1000$ pF see Figure 3 for $t_W$ vs. $C_X$ family curves with $R_X$ as a parameter:

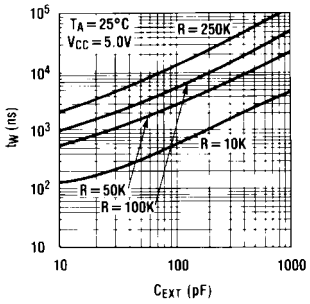



**FIGURE 3.**

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:

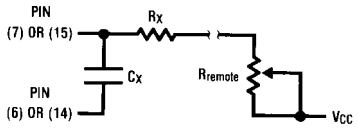



**FIGURE 4.**

**"$R_{remote}$" should be as close to the device pin as possible.**

7. The retriggerable pulse width is calculated as shown below:

   $T = t_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$

   The retriggered pulse width is equal to the pulse width plus a delay time period (Figure 5).

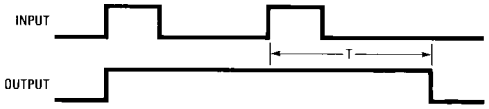



**FIGURE 5.**

## Operating Rules (Continued)

8. Output pulse width variation versus $V_{CC}$ and temperatures: Figure 6 depicts the relationship between pulse width variation versus $V_{CC}$, and Figure 7 depicts pulse width variation versus temperatures.

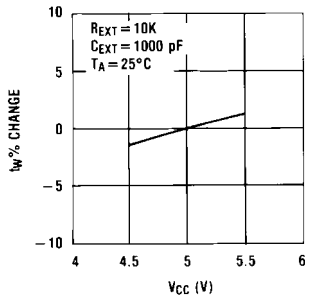



**FIGURE 6.**

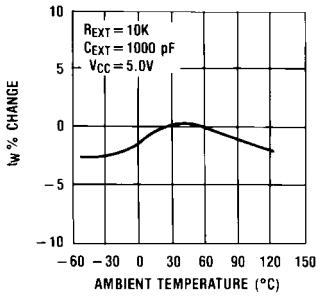



**FIGURE 7.**

9. Under any operating condition $C_X$ and $R_X$ must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from $C_X$ to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of $C_X$ in each cycle of its operation so that the output pulse width will be accurate.
10. The $C_{EXT}$ pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.
11. $V_{CC}$ and ground wiring should conform to good high-frequency standards and practices so that switching transients on the $V_{CC}$ and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from $V_{CC}$ to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the $V_{CC}$-pin as space permits.

**Note: For further detailed device characteristics and output performance please refer to the Fairchild Semiconductor one-shot application note AN-372.**

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature | −65°C to +150°C |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Nom | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | HIGH Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | | −0.4 | mA |
| $I_{OL}$ | LOW Level Output Current | | | | 8 | mA |
| $t_W$ | Pulse Width (Note 2) | A or B HIGH | 40 | | | ns |
| | | A or B LOW | 40 | | | |
| | | Clear LOW | 40 | | | |
| $R_{EXT}$ | External Timing Resistor | | 5 | | 260 | kΩ |
| $C_{EXT}$ | External Timing Capacitance | | No Restriction | | | µF |
| $C_{WIRE}$ | Wiring Capacitance at $R_{EXT}/C_{EXT}$ Terminal | | | | 50 | pF |
| $T_A$ | Free Air Operating Temperature | | 0 | | 70 | °C |

**Note 2:** $T_A = 25°C$ and $V_{CC} = 5V$.

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 3) | Max | Units |
|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | −1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max, $V_{IL}$ = Max, $V_{IH}$ = Min | 2.7 | 3.4 | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max, $V_{IL}$ = Max, $V_{IH}$ = Min | | 0.35 | 0.5 | V |
| | | $I_{OL}$ = 4 mA, $V_{CC}$ = Min | | 0.25 | 0.4 | |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 7V | | | 0.1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7V | | | 20 | µA |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 4) | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (Note 5)(Note 6)(Note 7) | | 12 | 20 | mA |

**Note 3:** All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

**Note 4:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 5:** Quiescent $I_{CC}$ is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs OPEN, $C_{EXT}$ = 0.02 µF, and $R_{EXT}$ = 25 kΩ.

**Note 6:** $I_{CC}$ is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs OPEN, $C_{EXT}$ = 0.02 µF, and $R_{EXT}$ = 25 kΩ.

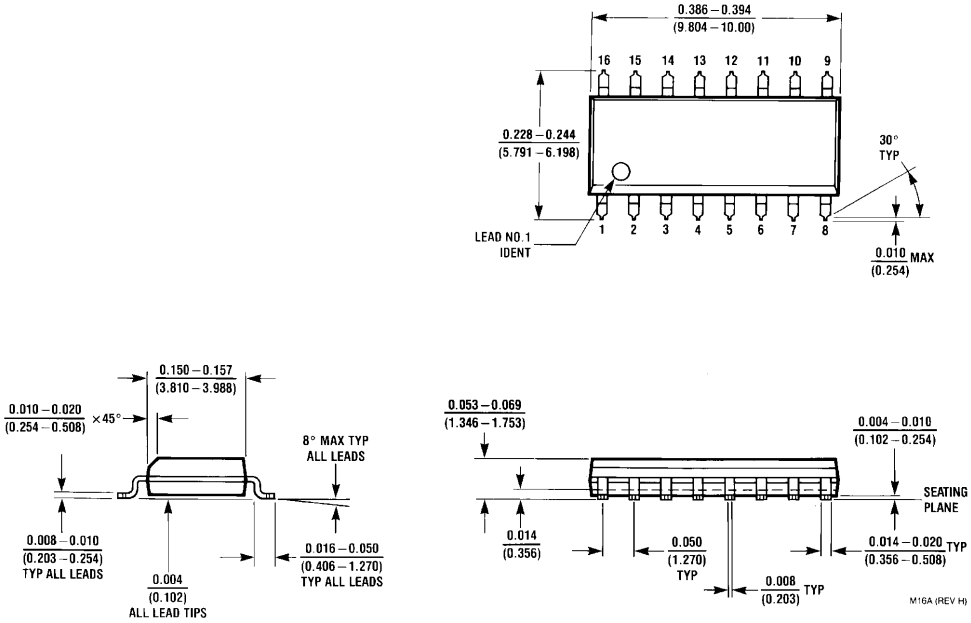
**Note 7:** With all outputs OPEN and 4.5V applied to all data and clear inputs, $I_{CC}$ is measured after a momentary ground, then 4.5V is applied to the clock.

## Switching Characteristics

at $V_{CC}$ = 5V and $T_A$ = 25°C

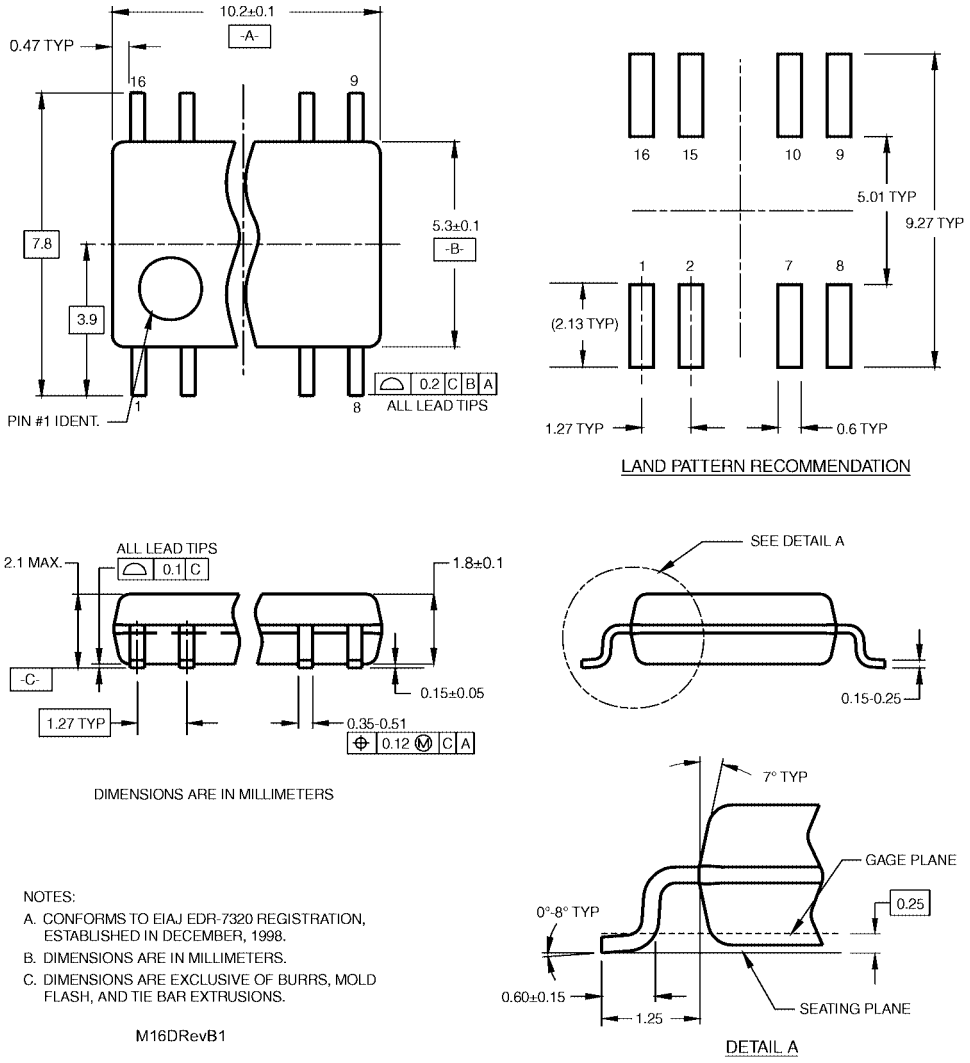
| Symbol | Parameters | From (Input) To (Output) | $R_L$ = 2 kΩ | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 15pF, $C_{EXT}$ = 0 pF, $R_{EXT}$ = 5 kΩ | | $C_L$ = 15pF, $C_{EXT}$ = 1000 pF, $R_{EXT}$ = 10 kΩ | | |
| | | | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | A to Q | | 33 | | | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | B to Q | | 44 | | | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | A to $\overline{Q}$ | | 45 | | | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | B to $\overline{Q}$ | | 56 | | | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Clear to $\overline{Q}$ | | 45 | | | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Q | | 27 | | | ns |
| $t_{WQ(Min)}$ | Minimum Width of Pulse at Output Q | A or B to Q | | 200 | | | ns |
| $t_{W(out)}$ | Output Pulse Width | A or B to Q | | | 4 | 5 | µs |

## Physical Dimensions inches (millimeters) unless otherwise noted




**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow**
**Package Number M16A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

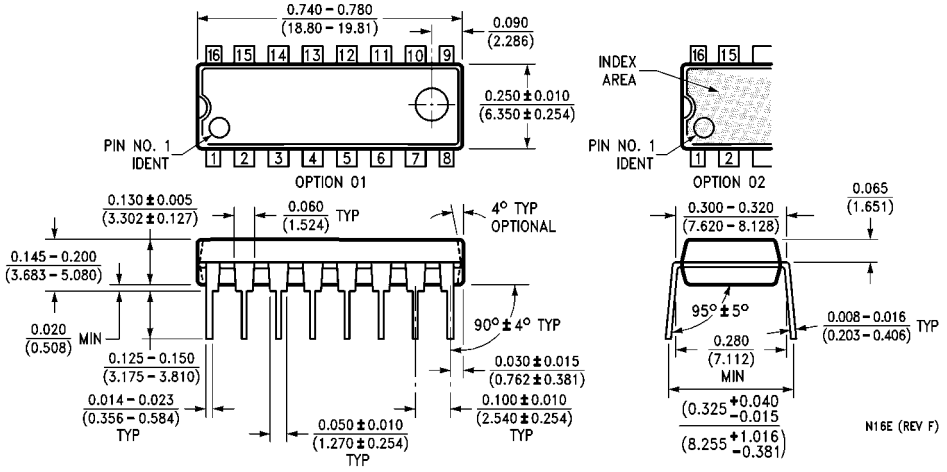
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N16E**



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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