General-purpose CMOS Logic IC Series (BU4S,BU4000B Series)

High Voltage CMOS Logic ICs <Function Logic>

BU4015B,BU4015BF,BU4021B,BU4021BF,
BU4094BC,BU4094BCF,BU4094BCFV,BU4538B,BU4028B

No.09050EAT04

●Description

BU4015B series ICs are 4-stage static shift registers, each consisting of 2 circuits. The D flip-flops of each stage share a common reset input, enabling asynchronous reset at any time.
BU4021B series ICs are 8-bit static shift registers configured with 8 register cells, each of which has parallel input. Control of the parallel/serial input (P/S) enables serial input/output with clock synchronization and well as parallel input/serial output conversions.
BU4094BC series ICs are shift/store registers, each consisting of an 8-bit shift register and an 8-bit latch. Output can be held in the data transfer mode because the data read into the shift register can be latched by the asynchronous strobe input,
The BU4538B IC is a monostable multivibrator that can be reset and retriggered from either edge of an input pulse. A wide range of accurate output pulse widths is available because the output pulse width and accuracy are determined by the external timing constants Cx an Rx.
The BU4028B IC is a decoder which converts BCD signals into decimal signals. Of the 10 outputs (Q0 ~ Q9), those corresponding to the input codes A-D are set to “H”, while the others are set to “L”.

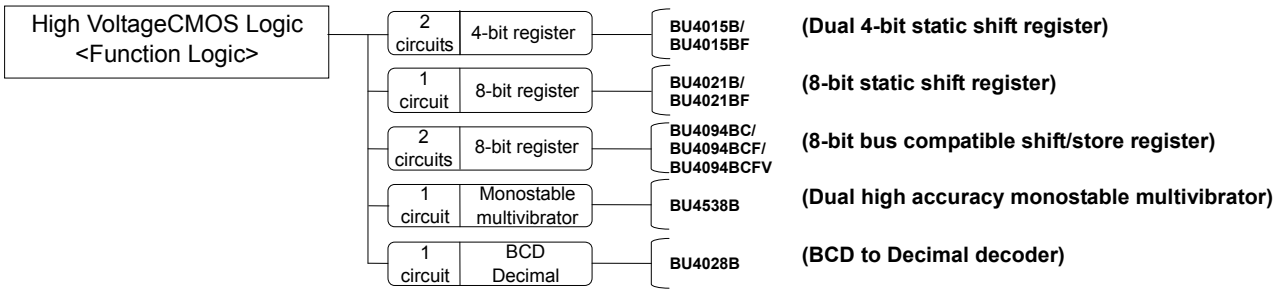
●Features

1) Low power consumption
2) Wide operating supply voltage range
3) High impedance
4) High fan out
5) L-TTL2 and LS-TTL1 inputs can be driven directly.

●Applications

BU4015B: serial / parallel data conversion and ring counter.
BU4021B: control circuits, timing circuits and as a general purpose register requiring high degree of noise tolerance.
BU4094BC: series/parallel data conversion and data receivers.
BU4538B: can obtain the output pulse amplitude with improved accuracy by external capacity and resistance.
BU4028B: code conversion, address decoding, memory selection control, demultiplexing or readout and decoding, etc.

●Lineup



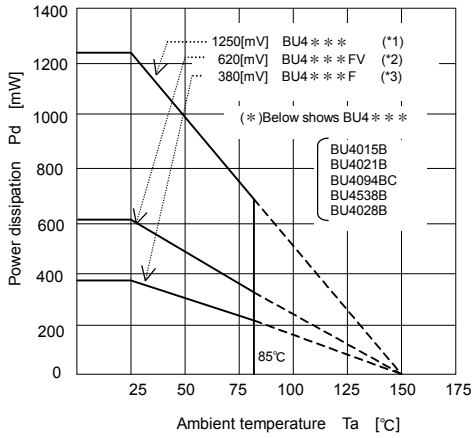
●Absolute Maximum Ratings

Parameter	Symbol	Limit					Unit
		BU4015B	BU4021B	BU4094BC	BU4538B	BU4028B	
Power Supply Voltage	VDD	-0.3 to 18					V
Supply Current	Iin	±10					mA
Operating Temperature	Topr	-40 to 85					℃
Storage Temperature	Tstg	-55 to 150					℃
Input Voltage	VIN	-0.3 to VDD+0.3					V
Maximum Junction Temperature	Tjmax	150					℃

●Recommended Operating Conditions

Parameter	Symbol	Limit					Unit
		BU4015B	BU4021B	BU4094BC	BU4538B	BU4028B	
Operating Power Supply	VDD	3 to 16 (3 to 18V @BU4094BC)					V
Input Voltage	VIN	0 to VDD					V

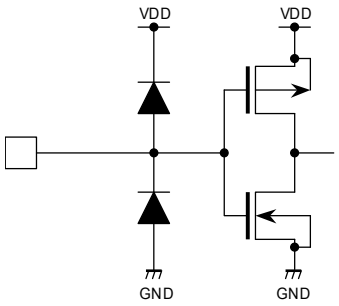
●Thermal Derating Curve



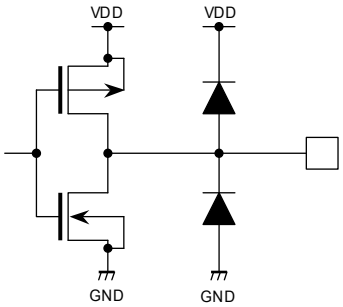
(*1)	(*2)	(*3)	Unit
10.0	5.0	3.1	mW/℃

When used at Ta=25℃ or higher the value above is reduced per 1℃. Power Dissipation is measured by using the sample mounted on a 70mm×70mm×1.6mm FR4 glass-epoxy PCB (cupper area is less than 3%)

●Input / Output Equivalent Circuits



＜Input＞



＜Output＞

●Electrical Characteristics(BU4015B)

DC Characteristics (Unless otherwise noted VSS=0[V],Ta=25[℃])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Input 'H' voltage	VIH	3.5	—	—	V	5	—	—
		7.0	—	—		10		
		11.0	—	—		15		
Input 'L' voltage	VIL	—	—	1.5	V	5	—	—
		—	—	3.0		10		
		—	—	4.0		15		
Input 'H' current	IIH	—	—	0.3	μA	15	VIH=15[V]	—
Input 'L' current	IIL	—	—	-0.3	μA	15	VIL=0[V]	—
Output 'H' voltage	VOH	4.95	—	—	V	5	IO=0[mA]	1
		9.95	—	—		10		
		14.95	—	—		15		
Output 'L' voltage	VOL	—	—	0.05	V	5	IO=0[mA]	2
		—	—	0.05		10		
		—	—	0.05		15		
Output 'H' current	IOH	-0.16	—	—	mA	5	VOH=4.6[V]	1
		-0.4	—	—		5	VOH=9.5[V]	
		-1.2	—	—		15	VOH=13.5[V]	
Output 'L' current	IOL	0.44	—	—	mA	5	VOL=0.4[V]	2
		1.1	—	—		10	VOL=0.5[V]	
		3.0	—	—		15	VOL=1.5[V]	
Static supply current	IDD	—	—	20	μA	5	VI=VSS or GND	—
		—	—	40		10		
		—	—	80		15		

Switching Characteristics (Unless otherwise noted VSS=0[V],Ta=25[℃],CL=50[pF])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Output rising time	tTLH	—	180	—	ns	5	—	—
		—	90	—		10		
		—	65	—		15		
Output falling time	TTHL	—	100	—	ns	5	—	—
		—	50	—		10		
		—	40	—		15		
Propagation delay time CLOCK, D→Q	tPLH tPHL	—	310	—	ns	5	—	3・4
		—	125	—		10		
		—	90	—		15		
Propagation delay time RESET→Q	tPLH tPHL	—	460	—	ns	5	—	5・6
		—	180	—		10		
		—	120	—		15		
Set up time	Tsu	—	100	—	ns	5	—	7・8
		—	50	—		10		
		—	40	—		15		
Minimum clock pulse width	tW(CLK)	—	185	—	ns	5	—	9
		—	85	—		10		
		—	55	—		15		
Minimum reset pulse width	tW(RST)	—	200	—	ns	5	—	10
		—	80	—		10		
		—	60	—		15		
Maximum clock frequency	f (CLK) Max.	—	20	—	MHz	5	—	—
		—	6.0	—		10		
		—	7.5	—		15		
Maximum clock rising/falling time	tr(CLK) tf(CLK)	—	100	—	μs	5	—	—
		—	40	—		10		
		—	15	—		15		
Input capacitance	CIN	—	5	—	pF	—	—	—

●Electrical Characteristics(BU4021B)

DC Characteristics (Unless otherwise noted VSS=0[V],Ta=25[°C])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Input 'H' voltage	VIH	3.5	—	—	V	5	—	—
		7.0	—	—		10		
		11.0	—	—		15		
Input 'L' voltage	VIL	—	—	1.5	V	5	—	—
		—	—	3.0		10		
		—	—	4.0		15		
Input 'H' current	IIH	—	—	0.3	μA	15	VIH=15[V]	—
Input 'L' current	IIL	—	—	-0.3	μA	15	VIL=0[V]	—
Output 'H' voltage	VOH	4.95	—	—	V	5	IO=0[mA]	11
		9.95	—	—		10		
		14.95	—	—		15		
Output 'L' voltage	VOL	—	—	0.05	V	5	IO=0[mA]	12
		—	—	0.05		10		
		—	—	0.05		15		
Output 'H' current	IOH	-0.16	—	—	mA	5	VOH=4.6[V]	11
		-0.4	—	—		5	VOH=9.5[V]	
		-1.2	—	—		15	VOH=13.5[V]	
Output 'L' current	IOL	0.44	—	—	mA	5	VOL=0.4[V]	12
		1.1	—	—		10	VOL=0.5[V]	
		3.0	—	—		15	VOL=1.5[V]	
Static supply current	IDD	—	—	20	μA	5	VI=VDD or GND	—
		—	—	40		10		
		—	—	80		15		

Switching Characteristics (Unless otherwise noted VSS=0[V],Ta=25[°C],CL=50[pF])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Output rising time	tTLH	—	180	—	ns	5	—	—
		—	90	—		10		
		—	65	—		15		
Output falling time	tTHL	—	100	—	ns	5	—	—
		—	50	—		10		
		—	40	—		15		
"L" to "H" Propagation delay time CLOCK→Q P/S→Q	tPLH	—	400	—	ns	5	—	13・15
		—	170	—		10		
		—	115	—		15		
"H" to "L" Propagation delay time CLOCK→Q P/S→Q	tPHL	—	400	—	ns	5	—	14・16
		—	170	—		10		
		—	115	—		15		
Set up time	tsu	—	150	—	ns	5	—	17
		—	50	—		10		
		—	30	—		15		
Minimum clock pulse width	tW(CLK)	—	150	—	ns	5	—	19
		—	75	—		10		
		—	40	—		15		
Maximum clock frequency	f (CLK) Max.	—	3.0	—	MHz	5	—	—
		—	6.0	—		10		
		—	8.0	—		15		
Maximum clock rising/falling time	tr(CLK) tf(CLK)	—	—	15	μs	5	—	—
		—	—	5.0		10		
		—	—	4.0		15		
Minimum P/S Control pulse width	tw(P/S)	—	150	—	ns	5	—	20
		—	75	—		10		
		—	40	—		15		
Input capacitance	CIN	—	5	—	pF	—	—	—

●Electrical Characteristics(BU4094BC)

DC Characteristics (Unless otherwise noted VSS=0[V],Ta=25[℃])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Input 'H' voltage	VIH	3.5	—	—	V	5	—	—
		7.0	—	—		10		
		11.0	—	—		15		
Input 'L' voltage	VIL	—	—	1.5	V	5	—	—
		—	—	3.0		10		
		—	—	4.0		15		
Input 'H' current	IIH	—	—	0.3	μA	15	VIH=15[V]	—
Input 'L' current	IIL	—	—	-0.3	μA	15	VIL=0[V]	—
Output 'H' voltage	VOH	4.95	—	—	V	5	IO=0[mA]	21
		9.95	—	—		10		
		14.95	—	—		15		
Output 'L' voltage	VOL	—	—	0.05	V	5	IO=0[mA]	22
		—	—	0.05		10		
		—	—	0.05		15		
Output 'H' current	IOH	-0.44	—	—	mA	5	VOH=4.6[V]	21
		-1.1	—	—		5	VOH=9.5[V]	
		-3.0	—	—		15	VOH=13.5[V]	
Output 'L' current	IOL	0.44	—	—	mA	5	VOL=0.4[V]	22
		1.1	—	—		10	VOL=0.5[V]	
		3.0	—	—		15	VOL=1.5[V]	
Static supply current	IDD	—	—	5	μA	5	VI=VDD or GND	—
		—	—	10		10		
		—	—	20		15		

Switching Characteristics (Unless otherwise noted VSS=0[V],Ta=25[℃],CL=50[pF])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Output rising time	tTLH	—	100	200	ns	5	—	—
		—	50	100		10		
		—	40	80		15		
Output falling time	tTHL	—	100	200	ns	5	—	—
		—	50	100		10		
		—	40	80		15		
Propagation delay time CLOCK→QS	tPLH tPHL	—	350	600	ns	5	—	23
		—	125	250		10		
		—	95	190		15		
Propagation delay time CLOCK→Q'S	tPLH tPHL	—	230	460	ns	5	—	24
		—	110	220		10		
		—	75	150		15		
Propagation delay time CLOCK→QN	tPLH tPHL	—	420	840	ns	5	—	25
		—	195	390		10		
		—	135	270		15		
Propagation delay time STROBE→QN	tPLH tPHL	—	290	580	ns	5	—	26
		—	145	290		10		
		—	100	200		15		
3state Propagation delay time Output Enable→QN	tPHZ tPZH	—	140	280	ns	5	RL=1[kΩ]	27
		—	75	150		10		
		—	55	110		15		
3 state Propagation delay time Output Enable→QN	tPLZ tPZL	—	140	280	ns	5	RL=1[kΩ]	28
		—	75	150		10		
		—	55	110		15		
Minimum set up time DATA→CLOCK	tsu	—	20	125	ns	5	—	29
		—	8	55		10		
		—	6	35		15		
Minimum hold time CLOCK →DATA	tH	—	10	40	ns	5	—	30
		—	10	20		10		
		—	5	15		15		
Minimum clock pulse width	tW(CLK)	—	100	200	ns	5	—	31
		—	50	100		10		
		—	40	80		15		
Maximum clock rising/falling time	tr(CL) tf(CL)	NO Limit			μs	5	—	—
						10		
						15		
Maximum clock frequency	f CL	1.25	2.5	—	MHz	—	—	—
		2.5	5	—		—		
		3.0	12.5	—		—		
Minimum strobe pulse width	TwH	—	100	200	ns	—	—	—
		—	40	80		—		
		—	35	70		—		
Input capacitance	CIN	—	5	—	pF	—	—	—

●**Electrical Characteristics(BU4538B)**

DC Characteristics (Unless otherwise noted VSS=0[V],Ta=25[℃])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Input 'H' voltage	VIH	3.5	—	—	V	5	—	—
		7.0	—	—		10		
		11.0	—	—		15		
Input 'L' voltage	VIL	—	—	1.5	V	5	—	—
		—	—	3.0		10		
		—	—	4.0		15		
Input 'H' current	IIH	—	—	0.3	μA	15	VIH=15[V]	—
Input 'L' current	IIL	—	—	-0.3	μA	15	VIL=0[V]	—
Output 'H' voltage	VOH	4.95	—	—	V	5	IO=0[mA]	—
		9.95	—	—		10		
		14.95	—	—		15		
Output 'L' voltage	VOL	—	—	0.05	V	5	IO=0[mA]	—
		—	—	0.05		10		
		—	—	0.05		15		
Output 'H' current	IOH	-0.16	—	—	mA	5	VOH=4.6[V]	—
		-0.4	—	—		5	VOH=9.5[V]	
		-1.2	—	—		15	VOH=13.5[V]	
Output 'L' current	IOL	0.44	—	—	mA	5	VOL=0.4[V]	—
		1.1	—	—		10	VOL=0.5[V]	
		3.0	—	—		15	VOL=1.5[V]	
Static supply current	IDD	—	—	20	μA	5	VI=VDD or GND	—
		—	—	40		10		
		—	—	80		15		

Switching Characteristics (Unless otherwise noted VSS=0[V],Ta=25[℃],CL=50[pF])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Output rising time	tTLH	—	100	—	ns	5	—	—
		—	50	—		10		
		—	40	—		15		
Output falling time	tTHL	—	100	—	ns	5	—	—
		—	50	—		10		
		—	40	—		15		
Propagation delay time A,B→Q,$\overline{Q}$	tPLH tPHL	—	300	—	ns	5	—	32・33
		—	150	—		10		
		—	100	—		15		
Propagation delay time CD→Q,$\overline{Q}$	tPLH tPHL	—	250	—	ns	5	—	34・35
		—	125	—		10		
		—	95	—		15		
Minimum input pulse width	tWIN	—	50	—	ns	5	—	36
		—	30	—		10		
		—	25	—		15		
Output pulse width 1	tWOUT1	185	200	215	μs	5	CX=2000[pF] RX=100[kΩ]	38
		185	200	215		10		
		185	200	215		15		
Output pulse width 2	tWOUT2	8.8	9.4	10.0	ms	5	CX=0.1[uF] RX=100[kΩ]	39
		8.8	9.4	10.0		10		
		8.8	9.4	10.0		15		
Minimum trigger time	trr	—	0	—	ns	5	—	—
		—	0	—		10		
		—	0	—		15		
Input capacitance	CIN	—	5	—	pF	—	—	—

●**Electrical Characteristics(BU4028B)**

DC Characteristics (Unless otherwise noted VSS=0[V],Ta=25[℃])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Input 'H' voltage	VIH	3.5	—	—	V	5	—	—
		7.0	—	—		10		
		11.0	—	—		15		
Input 'L' voltage	VIL	—	—	1.5	V	5	—	—
		—	—	3.0		10		
		—	—	4.0		15		
Input 'H' current	IIH	—	—	0.3	μA	15	VIH=15[V]	—
Input 'L' current	IIL	—	—	-0.3	μA	15	VIL=0[V]	—
Output 'H' voltage	VOH	4.95	—	—	V	5	IO=0[mA]	40
		9.95	—	—		10		
		14.95	—	—		15		
Output 'L' voltage	VOL	—	—	0.05	V	5	IO=0[mA]	41
		—	—	0.05		10		
		—	—	0.05		15		
Output 'H' current	IOH	-0.16	—	—	mA	5	VOH=4.6[V]	40
		-0.4	—	—		5	VOH=9.5[V]	
		-1.2	—	—		15	VOH=13.5[V]	
Output 'L' current	IOL	0.44	—	—	mA	5	VOL=0.4[V]	41
		1.1	—	—		10	VOL=0.5[V]	
		3.0	—	—		15	VOL=1.5[V]	
Static supply current	IDD	—	—	1	μA	5	VI=VDD or GND	—
		—	—	2		10		
		—	—	4		15		

Switching Characteristics (Unless otherwise noted VSS=0[V],Ta=25[℃],CL=50[pF])

Parameter	Symbol	Limits			Unit		Condition	Fig.No
		Min	Typ	Max		VDD[V]		
Output rising time	tTLH	—	180	—	ns	5	—	42
		—	90	—		10		
		—	65	—		15		
Output falling time	tTHL	—	100	—	ns	5	—	43
		—	50	—		10		
		—	40	—		15		
"L" to "H" Propagation delay time	tPLH	—	300	—	ns	5	—	44
		—	130	—		10		
		—	90	—		15		
"H" to "L" Propagation delay time	tPHL	—	300	—	ns	5	—	45
		—	130	—		10		
		—	90	—		15		
Input capacitance	CIN	—	5	—	pF	—	—	—

●Electrical Characteristics Curves(BU4015B)

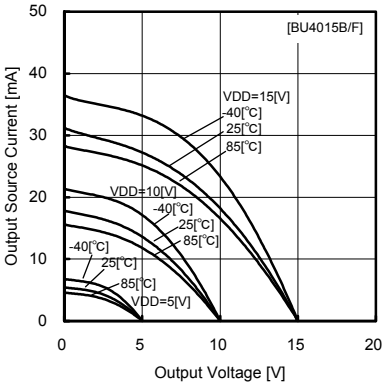


Fig.1 Output source current－voltage

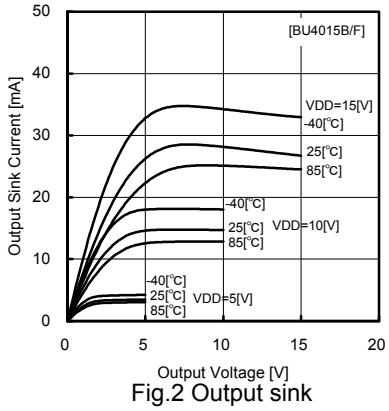


Fig.2 Output sink current－voltage

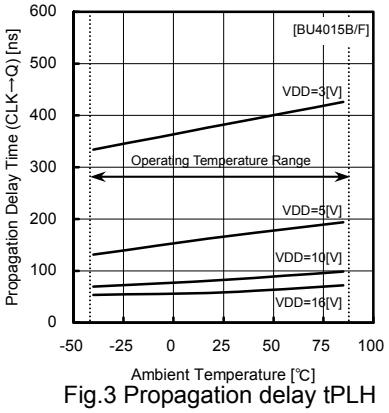


Fig.3 Propagation delay tPLH CLK→Q

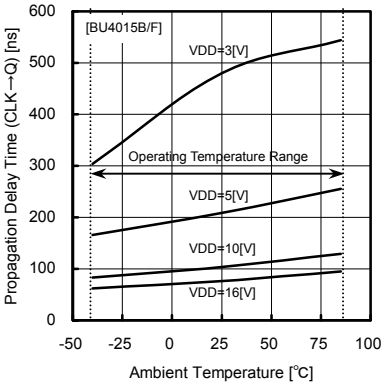


Fig.4 Propagation delay tPHL CLK→Q

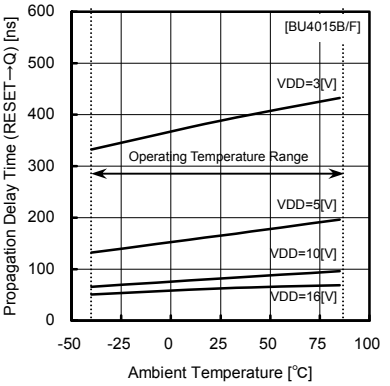


Fig.5 Propagation delay tPLH RESET→Q

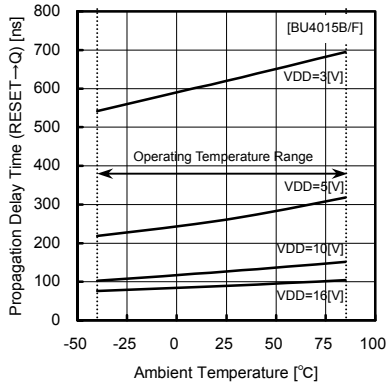


Fig.6 Propagation delay tPHL RESET→Q

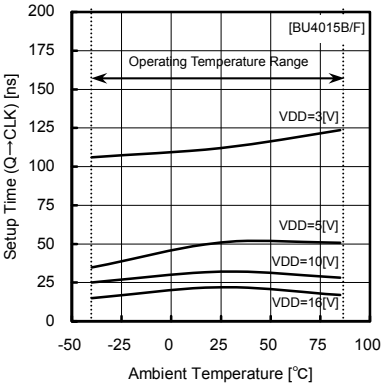


Fig.7Set up time tsu Q→CLK

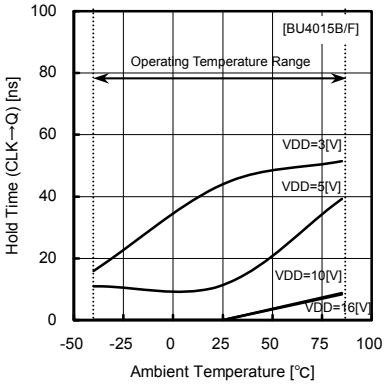


Fig.8 Hold time th CLK→Q

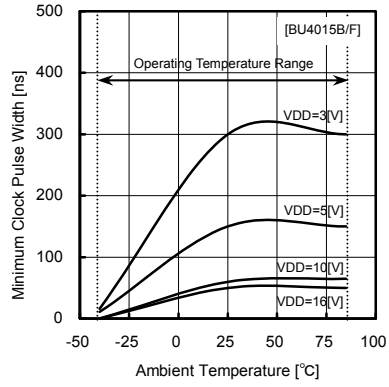


Fig.9 Minimum CLK pulse width

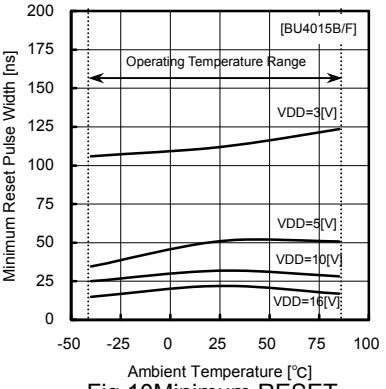
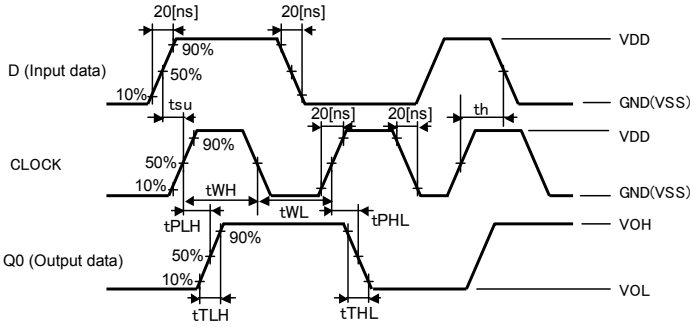


Fig.10Minimum RESET pulse width

○Switching characteristics



●Electrical Characteristics Curves(BU4021B)

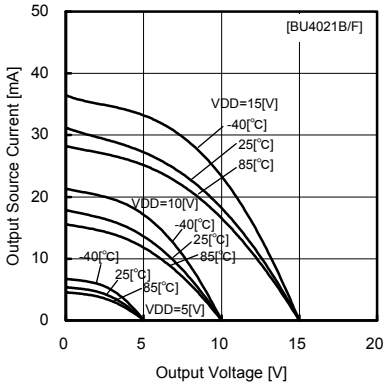


Fig.11 Output source current－voltage

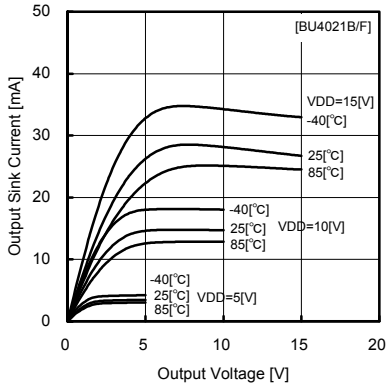


Fig.12 Output sink current－voltage

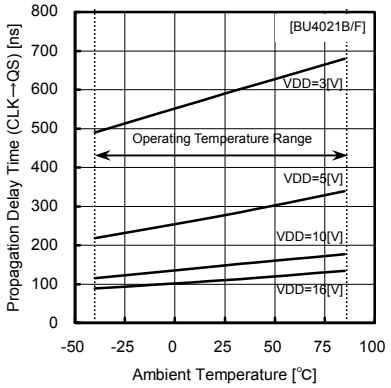


Fig.13 Propagation delay tPLH CLK→QS

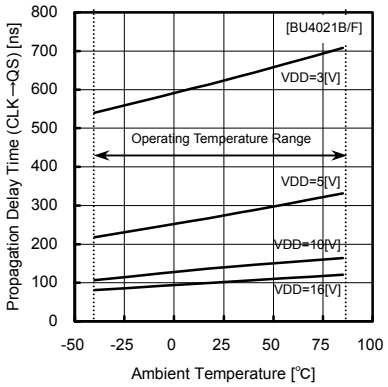


Fig.14 Propagation delay tPHL CLK→QS

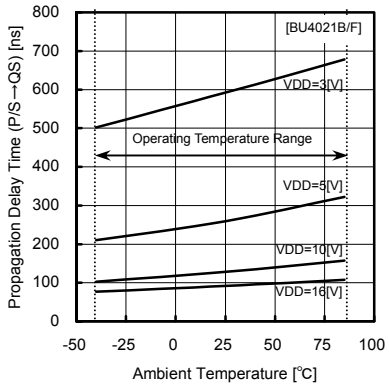


Fig.15 Propagation delay tPLH P/S→QS

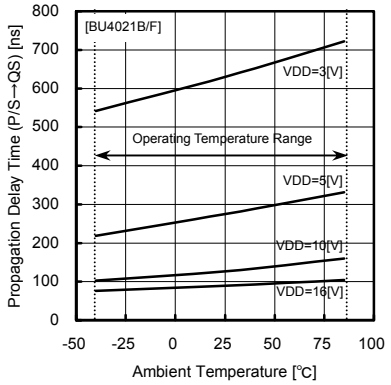


Fig.16 Propagation delay tPHL P/S→QS

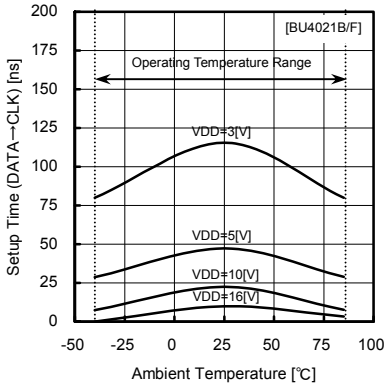


Fig.17 Set up time tsu Q→CLK

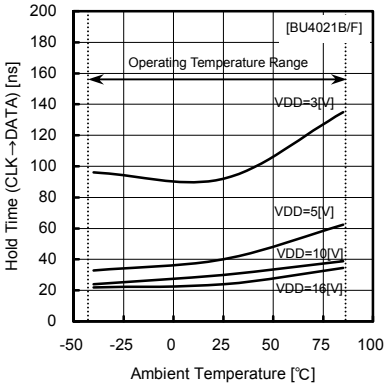


Fig.18 Hold time th CLK→Q

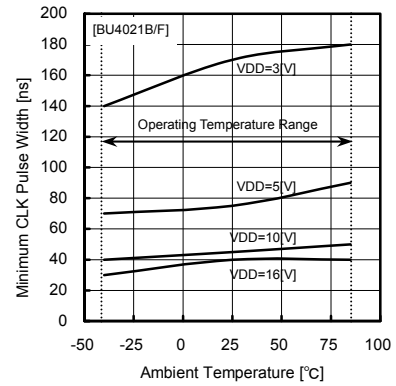


Fig.19 Minimum CLK pulse width

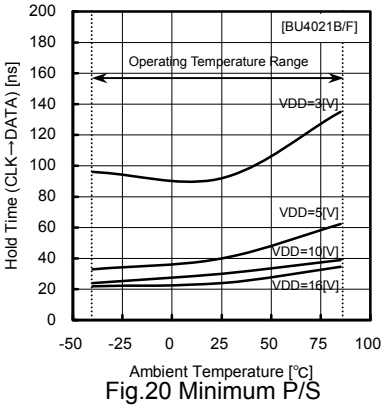
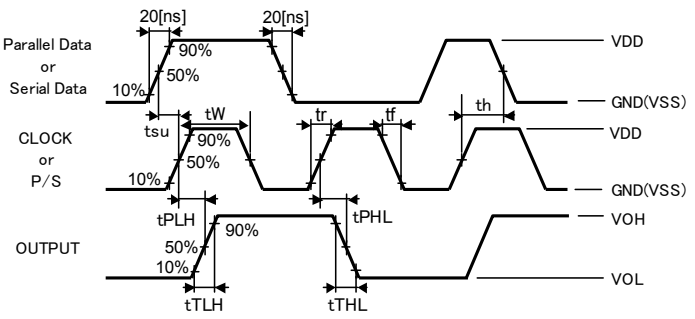


Fig.20 Minimum P/S pulse width

○Switching characteristics



●Electrical Characteristics Curves(BU4094BC)

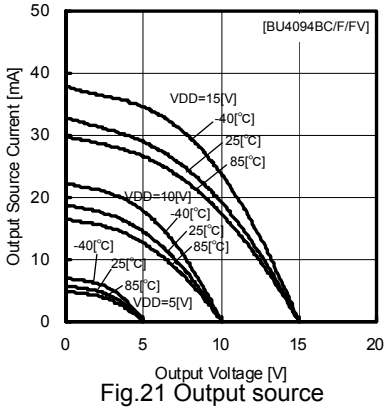


Fig.21 Output source current－voltage

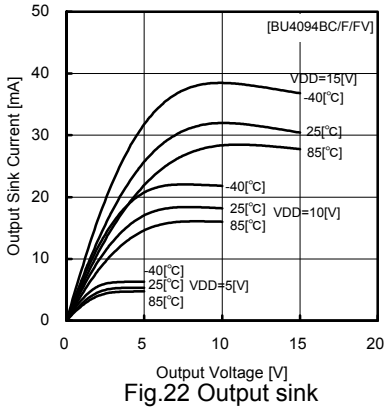


Fig.22 Output sink current－voltage

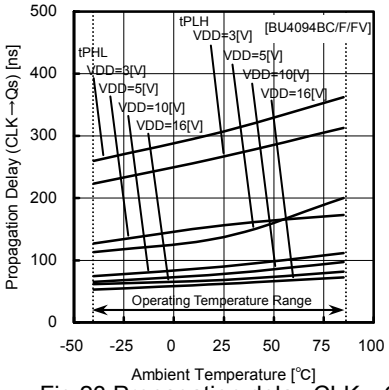


Fig.23 Propagation delay CLK→QS

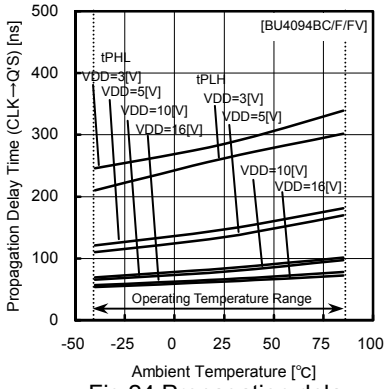


Fig.24 Propagation delay CLK→Q'S

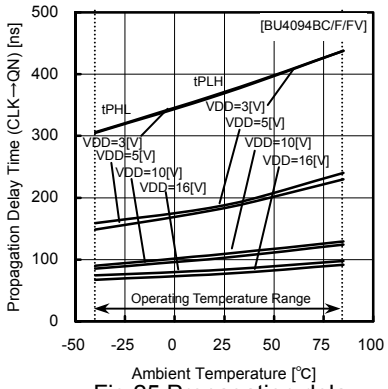


Fig.25 Propagation delay CLK→QN

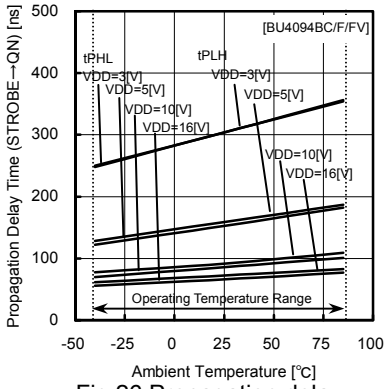


Fig.26 Propagation delay STROBE→QN

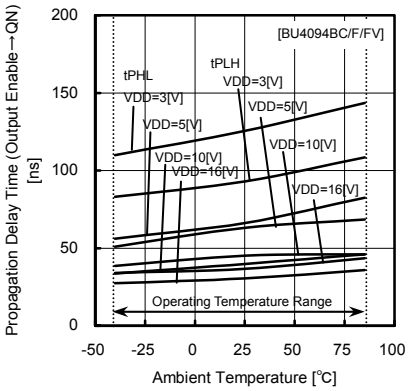


Fig.27 Propagation delay tPHZ Output Enable→QN

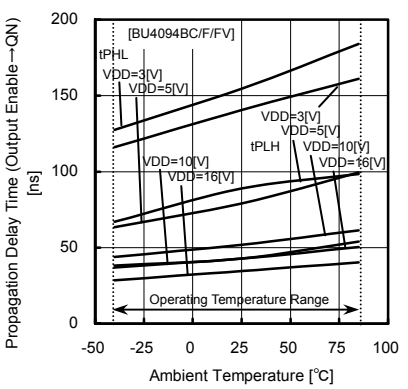


Fig.28 Propagation delay tPLZ Output Enable→QN

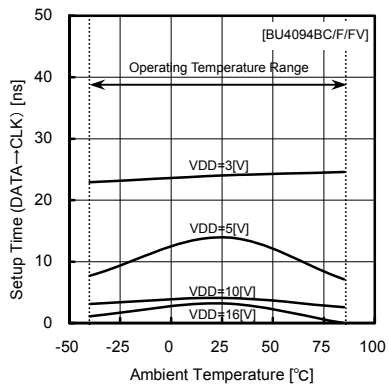


Fig.29 Set up time tsu DATA→CLK

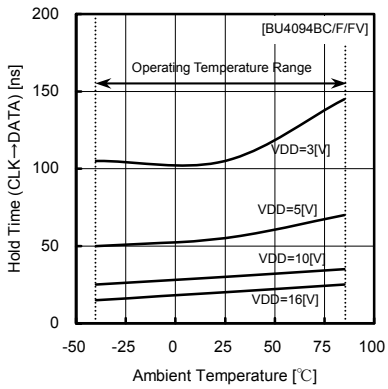


Fig.30 Hold time tH CLK→DATA

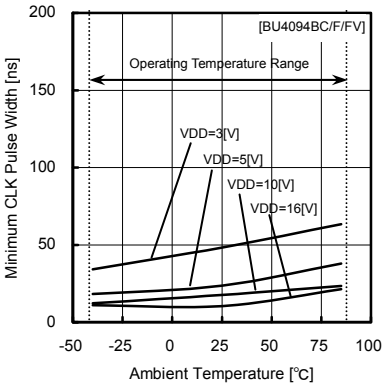


Fig.31 Minimum CLK pulse width tW(CLK)

○Switching characteristics are stated on page 14.

●Electrical Characteristics Curves(BU4538B)

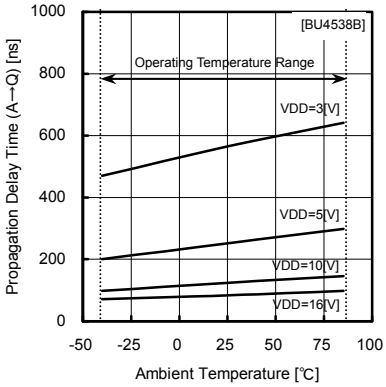


Fig.32 Propagation delay tPLH
A→Q

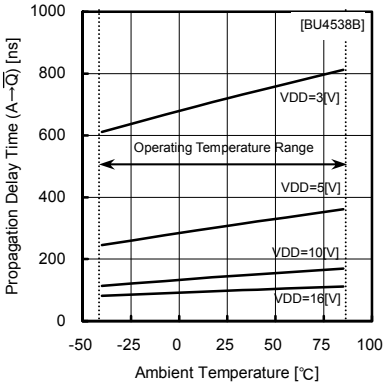


Fig.33 Propagation delay tPHL
A→$\overline{Q}$

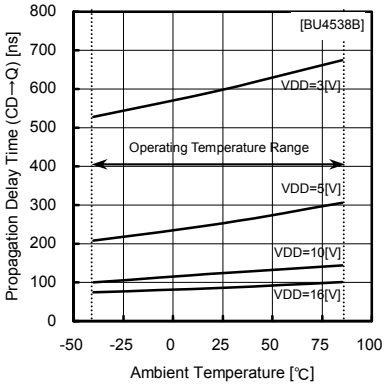


Fig.34 Propagation delay tPHL
CD→Q

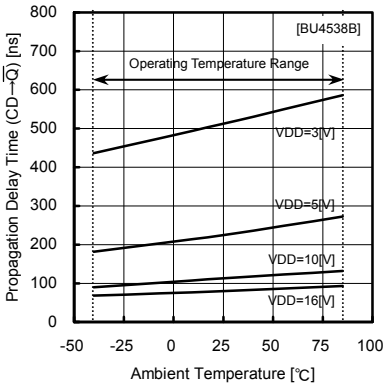


Fig.35 Propagation delay tPLH
CD→$\overline{Q}$

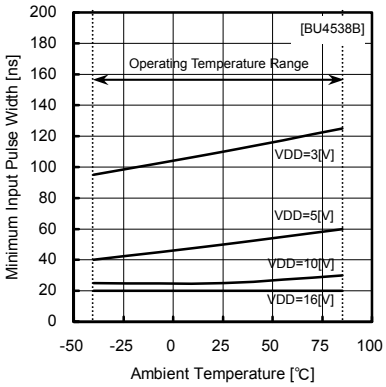


Fig.36 Minimum input pulse width
tWIN

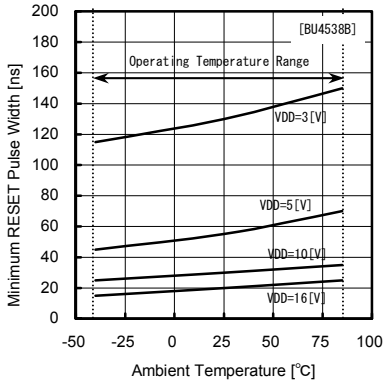


Fig.37 Minimum RESET pulse width
tRESET

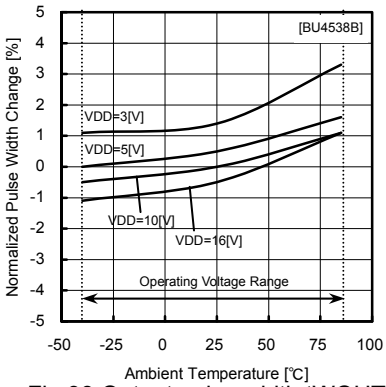


Fig.38 Output pulse width tWOUT1
(CX=2000[pF],RX=100[kΩ])

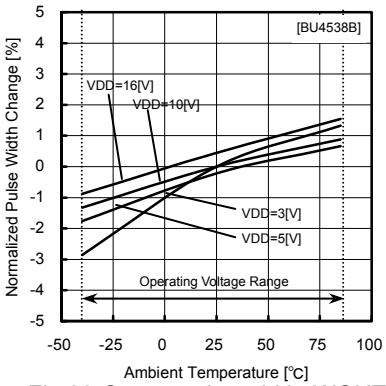
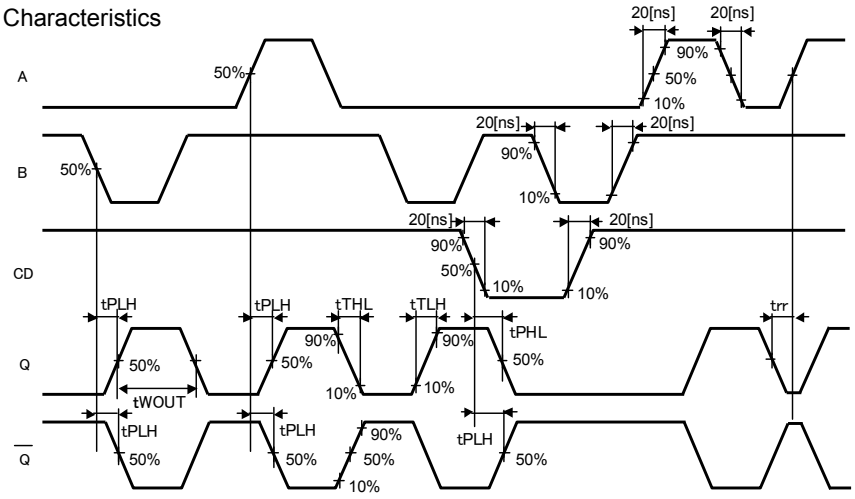


Fig.39 Output pulse width tWOUT2
(CX=0.1[μF],RX=100[kΩ])

○ Switching Characteristics



●Reference data(BU4028B)

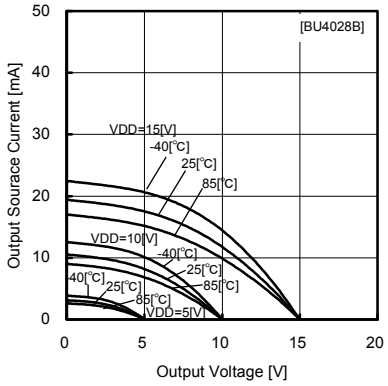


Fig.40 Output source current－voltage

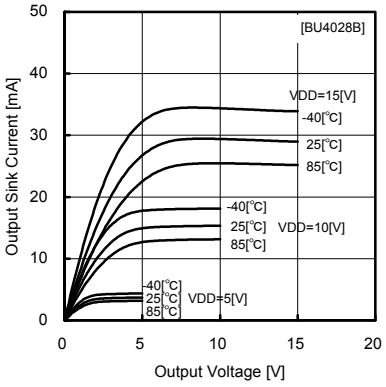


Fig.41 Output sink current－voltage

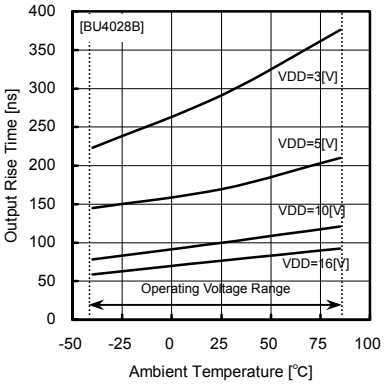


Fig.42 Propagation delay tTLH

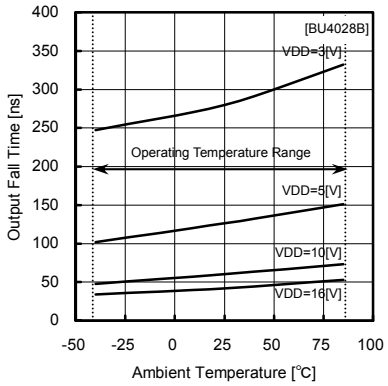


Fig.43 Propagation delay tTHL

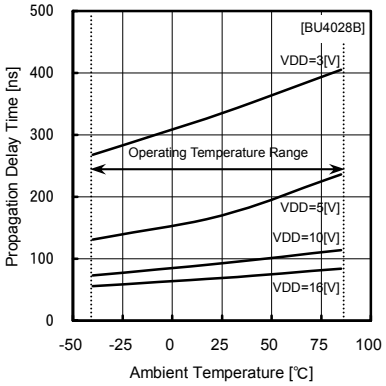


Fig.44 Propagation delay tPLH

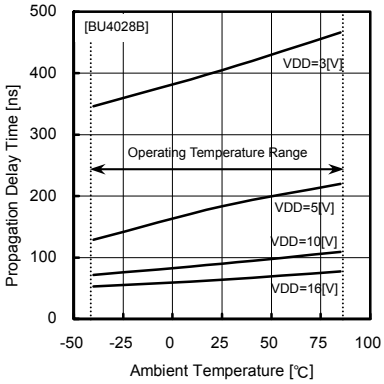


Fig.45 Propagation delay tPHL

(*) Switching characteristics is shown in P15.

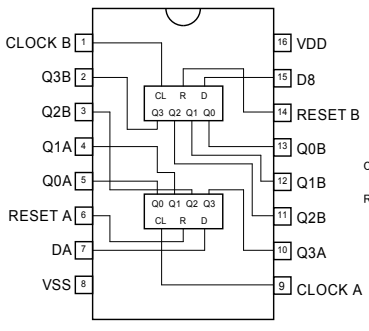
●Description of BU4015B series model

Function：Dual 4-bit static shift register

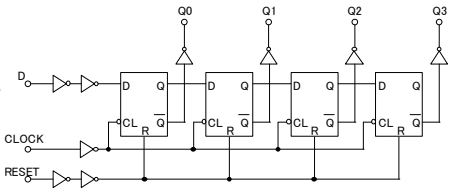
1) Description of operation

Dual 4-bit static shift register of BU4015B is configured with 2 independent serial input/parallel output registers of the same 4-state. Each register is provided with an independent clock and reset input having one series data input. Register state is the D type master/slave flip-flop. Data is shifted to the next stage during the rise time of the clock. Each register can be cleared by addition of “H” level to reset.

PIN arrangement



Block diagram



Truth table

CLOCK	D	RESET	Q0	Q1	Q2	Q3
↓	L	L	L	Q0	Q1	Q2
↓	H	L	H	Q0	Q1	Q2
↓	X	L	L	No Change		
X	X	H	L	L	L	L

X：Don't Care

PIN description

PIN No.	Symbol	I/O	Function
1	CLOCKB	I	Clock input (CHB)
2	Q3B	O	Output 3 (CHB)
3	Q2A	O	Output 2 (CHA)
4	Q1A	O	Output 1 (CHB)
5	Q0A	O	Output 0 (CHA)
6	RESETA	I	Reset input (CHA)
7	DA	I	Data input (CHA)
8	VSS	—	Power supply(-)
9	CLOCKA	I	Clock input (CHA)
10	Q3A	O	Output 3 (CHA)
11	Q2B	O	Output 2 (CHB)
12	Q1B	O	Output 1 (CHB)
13	Q0B	O	Output 0 (CHB)
14	RESETB	I	Reset input (CHB)
15	DB	I	Data input (CHB)
16	VDD	—	Power supply(+)

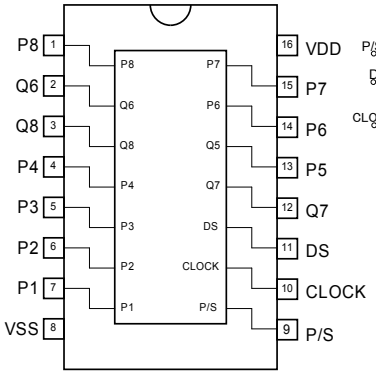
●Description of BU4021B series model

Function: 8-stage static shift register

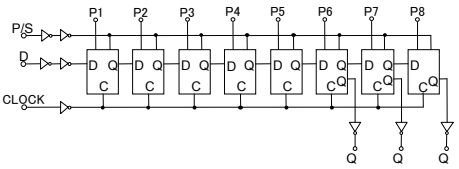
1) Description of operation

BU4021B is an 8-bit static shift register capable of parallel input/series output and series input/series output. In parallel operation, DS (data) being asynchronous with the clock is inputted into each F/F and obtained at output.
In series operation, DS (data) is triggered by clock.
When P/S input level is “H”, parallel operation is effective, and when P/S input level is “L”, series operation is effective.

PIN arrangement



Block diagram



PIN description

PIN No.	Symbol	I/O	Function
1	P8	I	Parallel data input 8
2	Q6	O	Output 6
3	Q8	O	Output 8
4	P4	I	Parallel data input 4
5	P3	I	Parallel data input 3
6	P2	I	Parallel data input 2
7	P1	I	Parallel data input 1
8	VSS	—	Power supply(-)
9	P/S	I	Parallel/Serial
10	CLOCK	I	Clock input
11	DS	I	Serial data input
12	Q7	O	Output 7
13	P5	I	Parallel data input 5
14	P6	I	Parallel data input 6
15	P7	I	Parallel data input 7
16	VDD	—	Power supply (+)

Truth table

CLOCK	D	RESET	Q0	Q1	Q2	Q3
↑	L	L	L	Q0	Q1	Q2
↑	H	L	H	Q0	Q1	Q2
↓	X	L	No Change			
X	X	H	L	L	L	L

X : Don't Care

CLOCK	DS	P/S	Dm	Qm*
↑	X	H	L	L
↑	X	H	H	H

X : Don't Care
*:Q6,Q7,Q8: outside

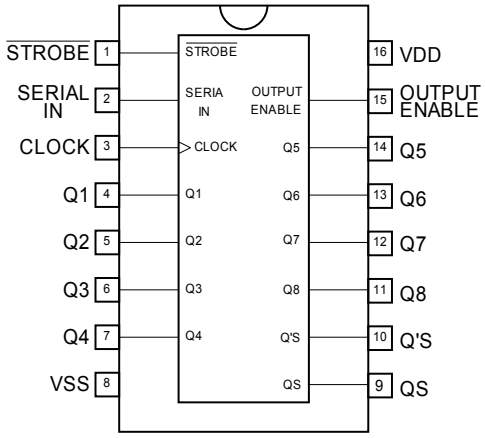
●Description of BU4094BC series model

Function: Dual 4-bit static shift register

1) Description of operation

BU4094BC is an 8-stage shift/store register provided in each stage with a data latch with 3-state output. Data read into shift register is read into the latch during the fall time of asynchronous STROBE input, and in the data transfer mode, output can be held. Data is passed through the latch and outputted when the STROBE is in “H” level. Because the parallel output becomes high impedance when the OUTPUT ENABLE terminal is set to “L” level by 3-state, the parallel output can be connected directly with the 8-bit pass line.

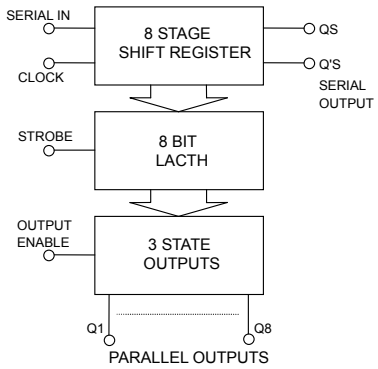
PIN arrangement



PIN description

PIN No.	Symbol	I/O	Function
1	STROBE	I	Latch input
2	SERIALIN	I	Data input
3	CLOCK	I	Clock input
4	Q1	O	Parallel data input Q1
5	Q2	O	Parallel data input Q2
6	Q3	O	Parallel data input Q3
7	Q4	O	Parallel data input Q4
8	VSS	—	Power supply(-)
9	QS	O	Serial data output QS
10	Q’S	O	Serial data output Q’S
11	Q8	O	Parallel data output Q8
12	Q7	O	Parallel data output Q7
13	Q6	O	Parallel data output Q6
14	Q5	O	Parallel data output Q5
15	ENABLE	I	Output enable
16	VDD	—	Power supply (+)

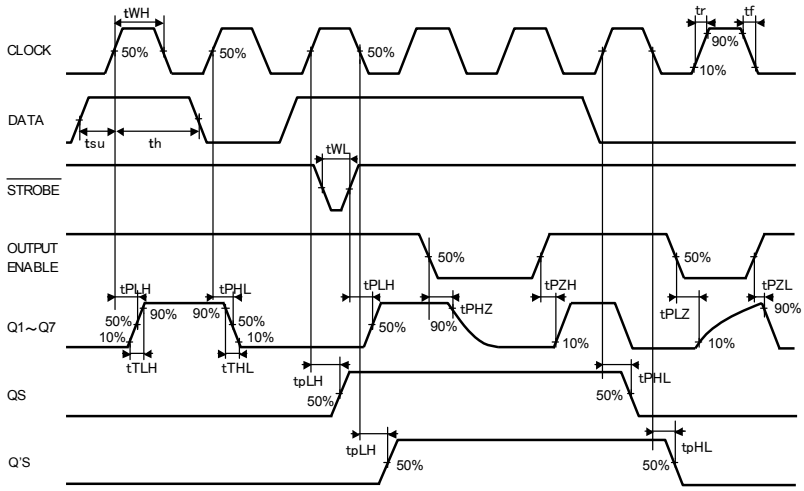
Block diagram



Truth table

CLOCK	OUTPUT ENABLE	$\overline{\text{STROBE}}$	SERIAL IN	Parallel Output		Serial Output	
				Q1	Qn	Qs	Q's
↑	H	H	L	L	Qn-1	Q7	NC
↑	H	H	H	H	Qn-1	Q7	NC
↑	H	L	X	NC	NC	Q7	NC
↑	L	X	X	Z	Z	Q7	NC
↓	H	X	X	NC	NC	NC	Qs
↓	H	H	X	Z	Z	NC	Qs

○ Switching characteristics



●Description of BU4538B series model

Function: Dual high accuracy monostable multivibrator

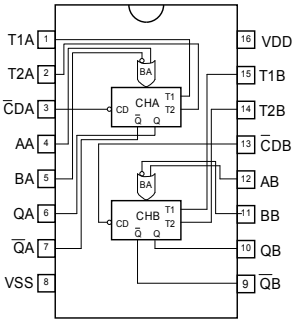
1) Description of operation

BU4538B is a re-triggerable monostable multi vibrator. Triggering is possible from either edge of the rise time and fall time of input pulse. Output pulse setting is determined by the time constant (Rx · Cx) of external Rx and Cx.

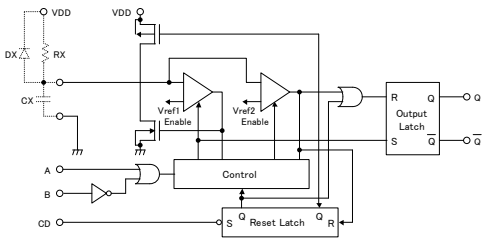
Recommended output pulse amplitude is 200[μs]~1[s].

(Cautions on use: In case of system power down, etc., electric charge accumulated in the capacity Cx is discharged to the VDD terminal through protective diode of 2 pins of 14 pins. When the electric current due to accumulated electric charge exceeds 10[mA], IC may be destructed. When a large capacity Cx is used, electric current flowing into the IC can be restricted by inserting the diode Dx.)

PIN arrangement



Block diagram



Truth table

INPUT			OUTPUT	
A	B	CD	Q	$\overline{Q}$
↑	H	H	⌐	⌐
↑	L	H	L	H
H	↓	H	L	H
L	↓	H	⌐	⌐
X	H	L	L	H

X:Don't Care

PIN description

PIN No.	Symbol	I/O	Function
1	T1A	—	Passive component connection pin 1(CHA)
2	T2A	—	Passive component connection pin 2(CHA)
3	CDA	I	Reset input (CHA)
4	AA	I	Input A(CHA)
5	BA	I	Input B(CHA)
6	QA	O	Output Q(CHA)
7	QAB	O	Output QB(CHA)
8	VSS	—	Power supply(-)
9	QBB	O	Output QB(CHB)
10	QB	O	Output Q(CHB)
11	BB	I	Input B(CHB)
12	AB	I	Input A(CHB)
13	CCB	I	Reset input (CHB)
14	T2B	—	Passive component connection pin 1(CHB)
15	T1B	—	Passive component connection pin 2(CHB)
16	VDD	—	Power supply (+)

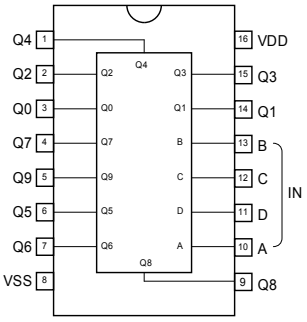
●Description of BU4028B series model

Function: BCD to decimal decoder

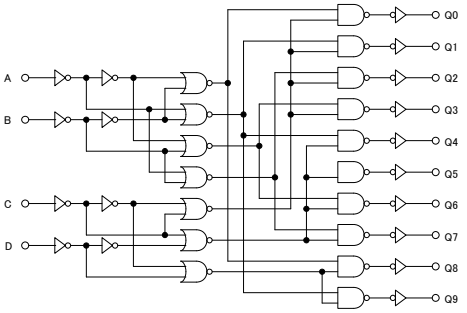
1) Description of operation

BU4028B is a decoder to convert BCD signals into decimal signals. Out of 10 outputs of Q0~Q9, output applicable for the input code of A~D becomes “H” level and all other outputs become “L” level. When the input of D is made to be inhibit input by using 3 inputs of A~C, this product can be used as a 1-OF-8 decoder.

PIN arrangement



Block diagram



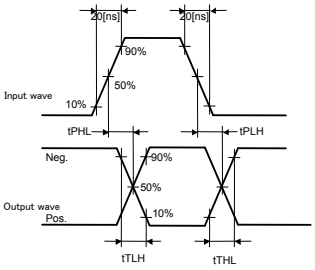
PIN description

PIN No.	Symbol	I/O	Function
1	Q4	O	Output 4
2	Q2	O	Output 2
3	Q0	O	Output 0
4	Q7	O	Output 7
5	Q9	O	Output 9
6	Q5	O	Output 5
7	Q6	O	Output 6
8	VSS	—	Power supply(-)
9	Q8	O	Output 8
10	A	I	Input A
11	D	I	Input D
12	C	I	Input C
13	B	I	Input B
14	Q1	O	Output 1
15	Q3	O	Output 3
16	VDD	—	Power supply (+)

Truth table

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
L	L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	H	L	L	L	L	L	L	L	L	H	L
L	L	H	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	L	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	H	L	L	L	L	L
L	H	H	L	L	L	L	H	L	L	L	L	L	L
L	H	H	H	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L	L
H	L	L	H	H	L	L	L	L	L	L	L	L	L
H	L	H	L	L	L	L	L	L	L	L	L	L	L
H	L	H	H	L	L	L	L	L	L	L	L	L	L
H	H	L	L	L	L	L	L	L	L	L	L	L	L
H	H	L	H	L	L	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	L	L	L	L	L	L	L	L	L	L

Switching characteristics



●Notes for use

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
2. Connecting the power supply connector backward
   Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.
3. Power supply lines
   Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.
4. GND voltage
   The potential of GND pin must be minimum potential in all operating conditions.
5. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
6. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
7. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
8. Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.
9. Ground Wiring Pattern
   When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
10. Unused input terminals
    Connect all unused input terminals to VDD or VSS in order to prevent excessive current or oscillation
    Insertion of a resistor (100kΩ approx.) is also recommended

●**Ordering part number**

B	U	4	0	1	5	B	F	V	-	E	2

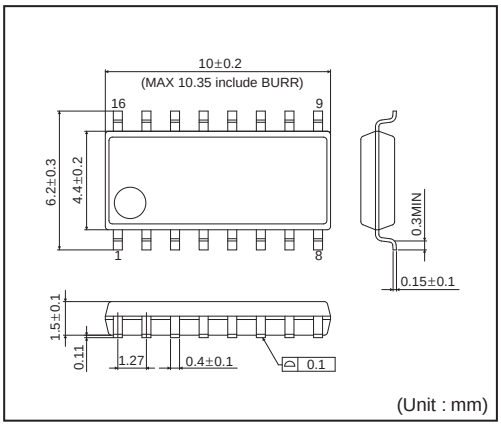
Part No.

Part No.
4015B 4538B
4021B 4028B
4094BC

Package
None: DIP16
F : SOP16
FV : SSOP-B16

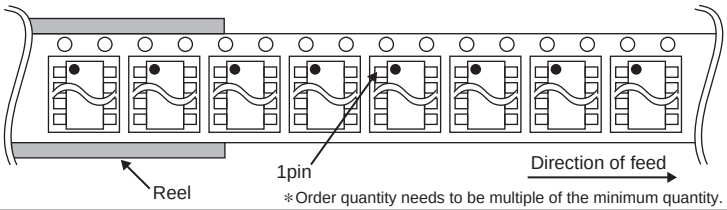
Packaging and forming specification
E2: Embossed tape and reel
None:Tray,Tube

SOP16



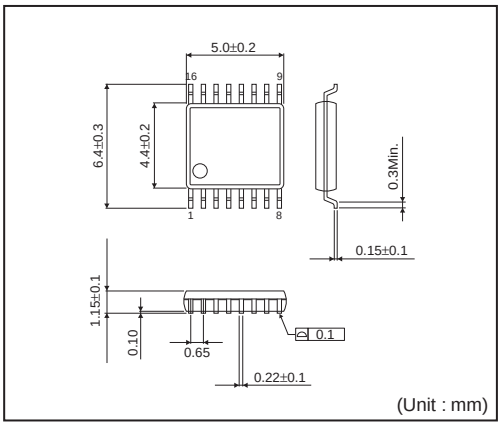
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



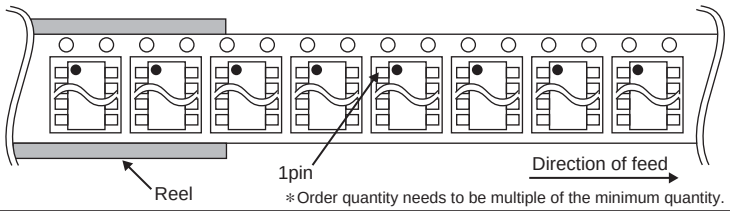
∗Order quantity needs to be multiple of the minimum quantity.

SSOP-B16



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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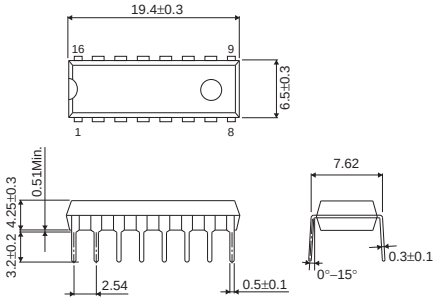
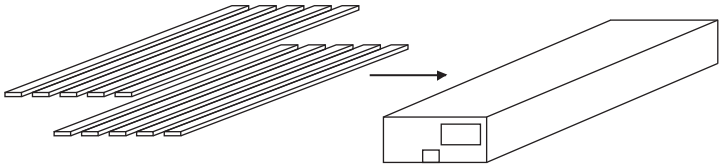
DIP16



(Unit : mm)

<Tape and Reel information>

Container	Tube
Quantity	1000pcs
Direction of feed	Direction of products is fixed in a container tube



∗Order quantity needs to be multiple of the minimum quantity.

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