

74LV123

Dual retriggerable monostable multivibrator with reset

Rev. 05 — 8 November 2007

Product data sheet

1. General description

The 74LV123 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC123; 74HCT123. It is a dual retriggerable monostable multivibrator which uses three methods to control the output pulse width:

1. The basic pulse time is programmed by the selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). These are normally connected as shown in [Figure 9](#).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\bar{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period ($nQ = \text{HIGH}$, $n\bar{Q} = \text{LOW}$) can be made as long as desired (see [Figure 12](#)).
3. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input $n\bar{RD}$, which also inhibits the triggering (see [Figure 13](#)).

Schmitt-trigger action in the $n\bar{A}$ and nB inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features

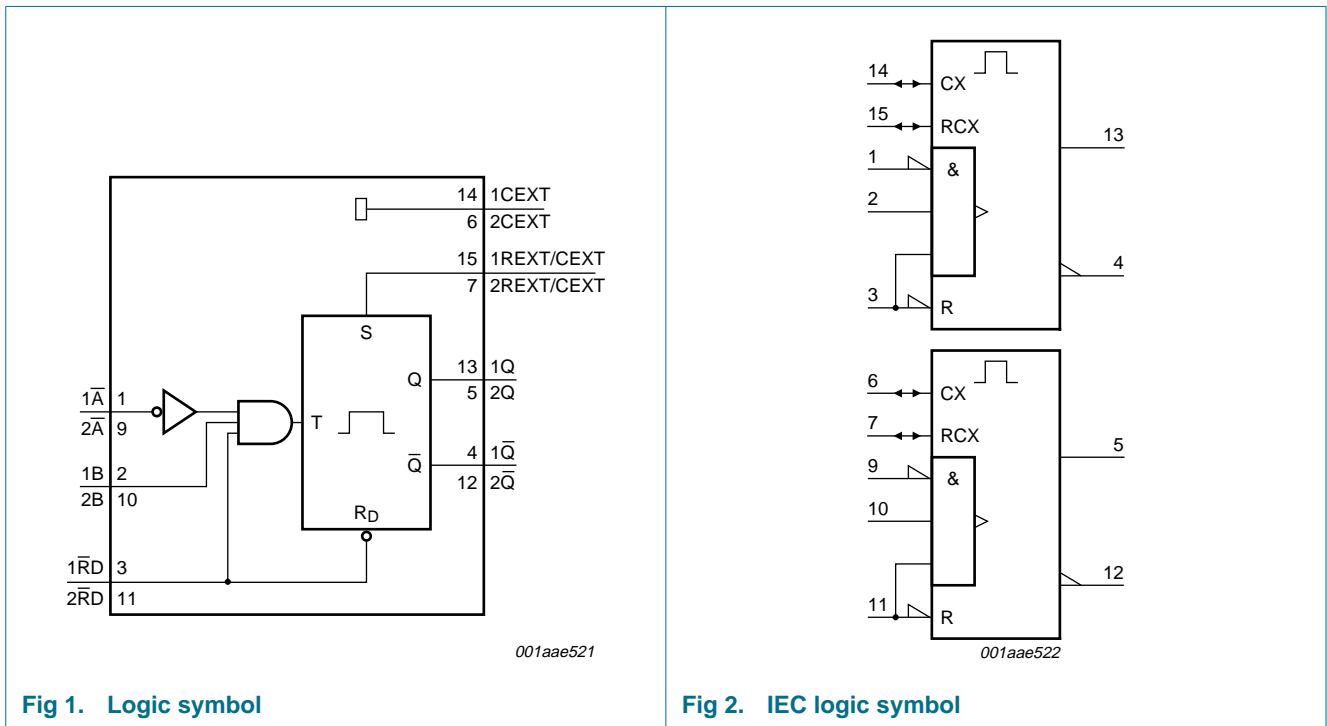
- Optimized for low-voltage applications: 1.0 V to 5.5 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical output ground bounce: < 0.8 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulses
- Schmitt-trigger action on all inputs except for the reset input

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74LV123N | -40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74LV123D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74LV123DB | -40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74LV123PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74LV123BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

4. Functional diagram



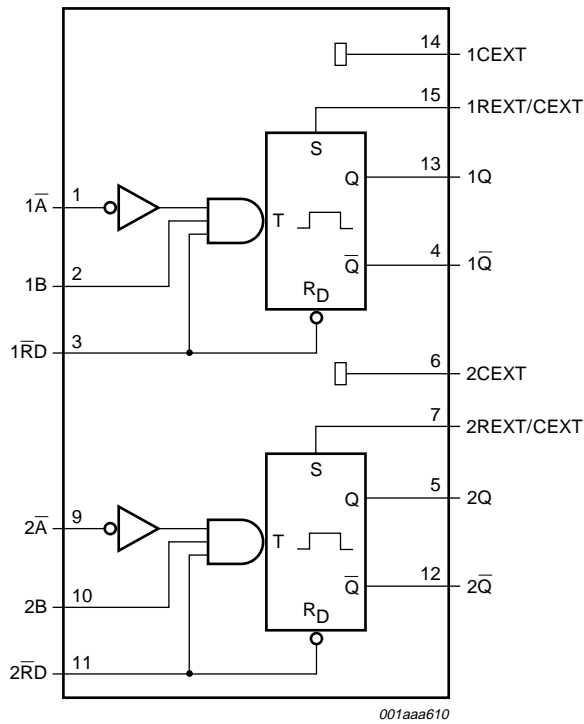


Fig 3. Functional diagram

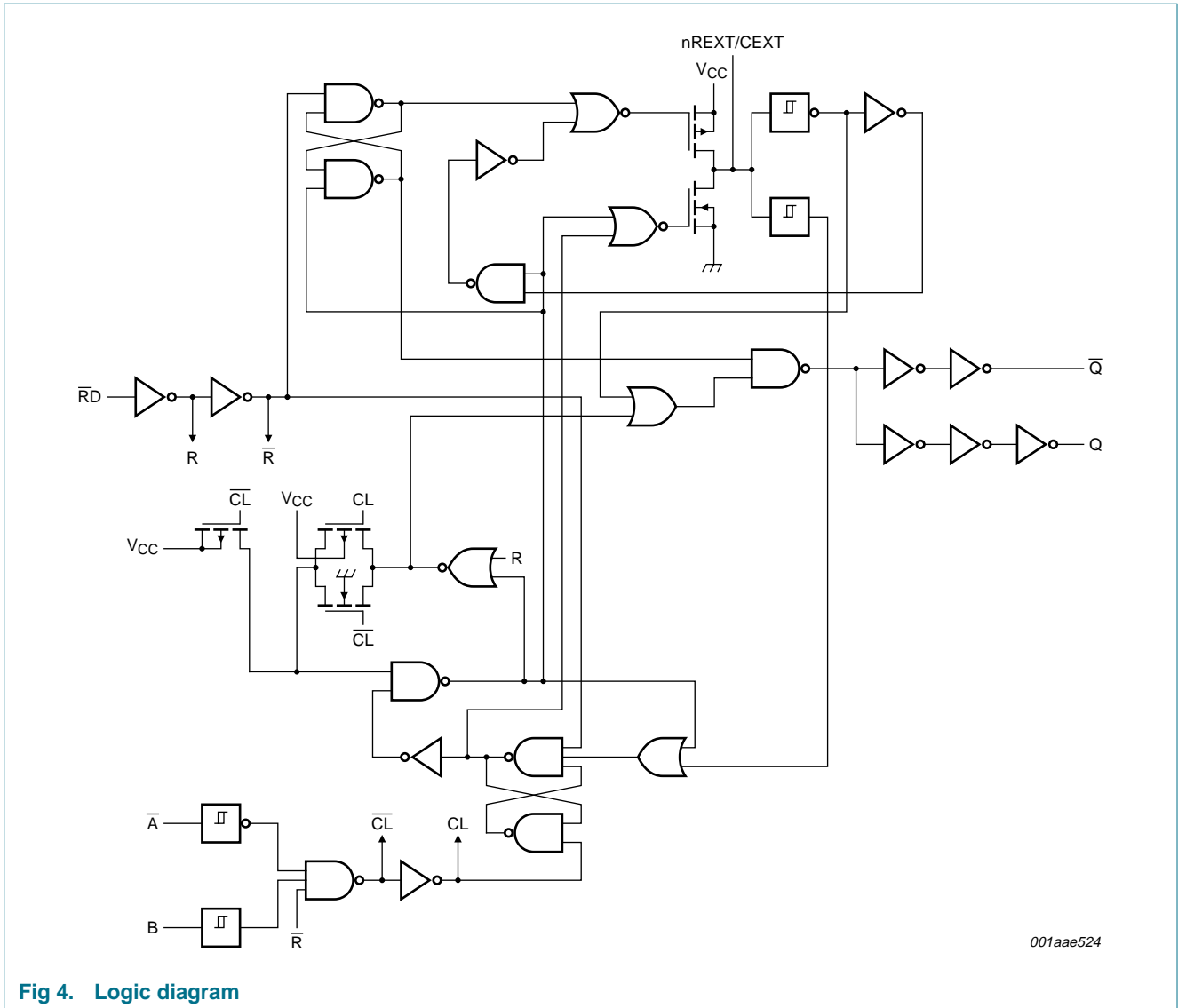
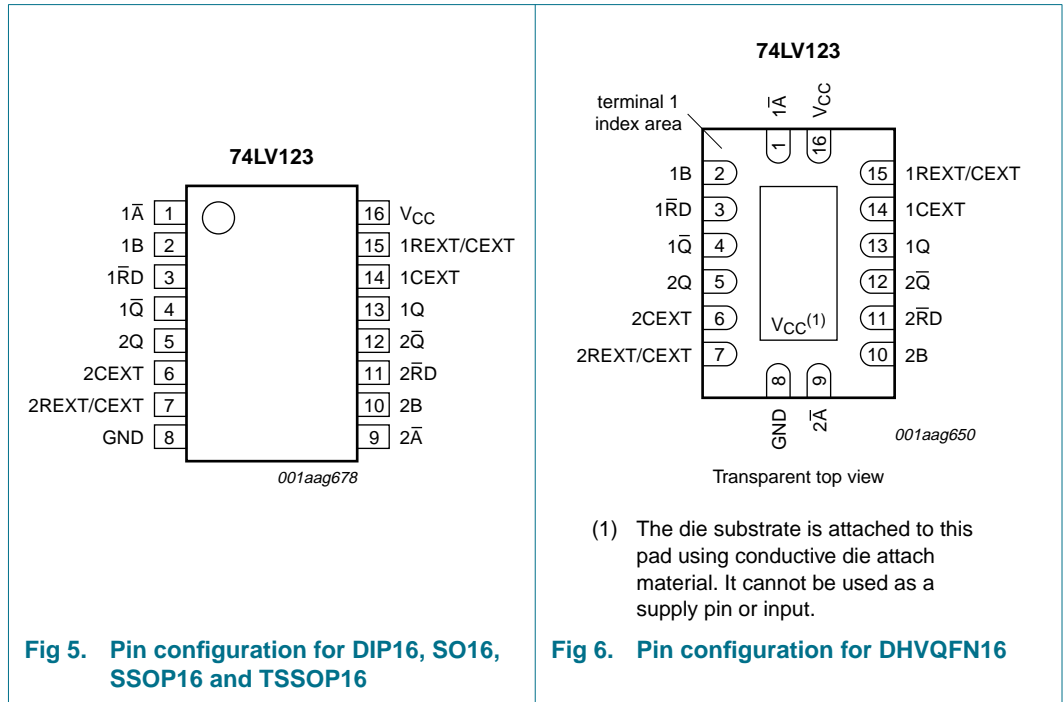


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning









5.2 Pin description

Table 2. Pin description


| Symbol | Pin | Description |
|-----------------|-----|--|
| 1 \bar{A} | 1 | negative-edge triggered input 1 |
| 1B | 2 | positive-edge triggered input 1 |
| 1 \bar{RD} | 3 | direct reset LOW and positive-edge triggered input 1 |
| 1 \bar{Q} | 4 | active LOW output 1 |
| 2Q | 5 | active HIGH output 2 |
| 2CEXT | 6 | external capacitor connection 2 |
| 2REXT/CEXT | 7 | external resistor and capacitor connection 2 |
| GND | 8 | ground (0 V) |
| 2 \bar{A} | 9 | negative-edge triggered input 2 |
| 2B | 10 | positive-edge triggered input 2 |
| 2 \bar{RD} | 11 | direct reset LOW and positive-edge triggered input 2 |
| 2 \bar{Q} | 12 | active LOW output 2 |
| 1Q | 13 | active HIGH output 1 |
| 1CEXT | 14 | external capacitor connection 1 |
| 1REXT/CEXT | 15 | external resistor and capacitor connection 1 |
| V _{CC} | 16 | supply voltage |


6. Functional description

Table 3. Function table^[1]

| Input | | | Output | |
|-------|----|----|---|---|
| nRD | nA | nB | nQ | nQ |
| L | X | X | L | H |
| X | H | X | L ^[2] | H ^[2] |
| X | X | L | L ^[2] | H ^[2] |
| H | L | ↑ |  |  |
| H | ↓ | H |  |  |
| ↑ | L | H |  |  |

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH transition;
 ↓ = HIGH-to-LOW transition;

 = one HIGH level output pulse

 = one LOW level output pulse

- [2] If the monostable multivibrator was triggered before this condition was established, the pulse will continue as programmed.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|-------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | [1] - | ±20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | [1] - | ±50 | mA |
| I_O | output current | except for pins nREXT/CEXT; $V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$ | [1] - | ±25 | mA |
| I_{CC} | supply current | | - | +50 | mA |
| I_{GND} | ground current | | - | -50 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ | | | |
| | | DIP16 package | [2] - | 750 | mW |
| | | SO16 package | [3] - | 500 | mW |
| | | SSOP16 package | [4] - | 500 | mW |
| | | TSSOP16 package | [4] - | 500 | mW |
| | | DHVQFN16 package | [5] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|---|---------|-----|----------|------|
| V_{CC} | supply voltage | | [1] 1.0 | 3.3 | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | in free air | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate [2] | $V_{CC} = 1.0\text{ V}$ to 2.0 V | - | - | 500 | ns/V |
| | | $V_{CC} = 2.0\text{ V}$ to 2.7 V | - | - | 200 | ns/V |
| | | $V_{CC} = 2.7\text{ V}$ to 3.6 V | - | - | 100 | ns/V |
| | | $V_{CC} = 3.6\text{ V}$ to 5.5 V | - | - | 50 | ns/V |

[1] The 74LV123 is guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (input levels GND or V_{CC}); [Section 9 “Static characteristics”](#) are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$.

[2] Except for Schmitt-trigger inputs n \bar{A} and nB.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|---------------------------|--|-----------------------|--------------------|-----------------------|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 0.9 | - | - | V |
| | | V _{CC} = 2.0 V | 1.4 | - | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | 0.3 | V |
| | | V _{CC} = 2.0 V | - | - | 0.6 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3 × V _{CC} | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 1.2 V | - | 1.2 | - | V |
| | | I _O = -100 μA; V _{CC} = 2.0 V | 1.8 | 2.0 | - | V |
| | | I _O = -100 μA; V _{CC} = 2.7 V | 2.5 | 2.7 | - | V |
| | | I _O = -100 μA; V _{CC} = 3.0 V | 2.8 | 3.0 | - | V |
| | | I _O = -100 μA; V _{CC} = 4.5 V | 4.3 | 4.5 | - | V |
| | | I _O = -6 mA; V _{CC} = 3.0 V | 2.40 | 2.82 | - | V |
| | | I _O = -12 mA; V _{CC} = 4.5 V | 3.60 | 4.20 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.2 V | - | 0 | - | V |
| | | I _O = 100 μA; V _{CC} = 2.0 V | - | 0 | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 2.7 V | - | 0 | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 3.0 V | - | 0 | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 4.5 V | - | 0 | 0.2 | V |
| | | I _O = 6 mA; V _{CC} = 3.0 V | - | 0.25 | 0.40 | V |
| | | I _O = 12 mA; V _{CC} = 4.5 V | - | 0.35 | 0.55 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | 1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 20.0 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V | - | - | 500 | μA |
| C _I | input capacitance | | - | 3.5 | - | pF |
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 0.9 | - | - | V |
| | | V _{CC} = 2.0 V | 1.4 | - | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | 0.3 | V |
| | | V _{CC} = 2.0 V | - | - | 0.6 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3 × V _{CC} | V |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|------------------|---------------------------|--|-----|--------------------|------|------|
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 1.2 V | - | - | - | V |
| | | I _O = -100 μA; V _{CC} = 2.0 V | 1.8 | - | - | V |
| | | I _O = -100 μA; V _{CC} = 2.7 V | 2.5 | - | - | V |
| | | I _O = -100 μA; V _{CC} = 3.0 V | 2.8 | - | - | V |
| | | I _O = -100 μA; V _{CC} = 4.5 V | 4.3 | - | - | V |
| | | I _O = -6 mA; V _{CC} = 3.0 V | 2.2 | - | - | V |
| | | I _O = -12 mA; V _{CC} = 4.5 V | 3.5 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.2 V | - | - | - | V |
| | | I _O = 100 μA; V _{CC} = 2.0 V | - | - | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 2.7 V | - | - | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 3.0 V | - | - | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 4.5 V | - | - | 0.2 | V |
| | | I _O = 6 mA; V _{CC} = 3.0 V | - | - | 0.5 | V |
| | | I _O = 12 mA; V _{CC} = 4.5 V | - | - | 0.65 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | 1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 160 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V | - | - | 850 | μA |

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f \leq 2.5\text{ ns}$; for test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|-------------------|--|---------------------|--------------------|-----|-------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| Propagation delay; see Figure 7 | | | | | | | | |
| t_{pd} | propagation delay | $n\overline{RD}$, $n\overline{A}$ and nB to $n\overline{Q}$ | [2] | | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 120 | - | - | - | ns |
| | | $V_{CC} = 2.0\text{ V}$ | - | 40 | 76 | - | 92 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | 30 | 56 | - | 68 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | 25 | 48 | - | 57 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | 18 | 40 | - | 46 | ns |
| | | $n\overline{RD}$ to nQ (reset) | [2] | | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 100 | - | - | - | ns |
| | | $V_{CC} = 2.0\text{ V}$ | - | 30 | 57 | - | 68 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | 23 | 43 | - | 51 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | 20 | 38 | - | 45 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | 14 | 31 | - | 36 | ns |
| Inputs $n\overline{A}$, nB and $n\overline{RD}$; see Figure 7 | | | | | | | | |
| t_w | pulse width | $n\overline{A} = \text{LOW}$ | | | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | 30 | 5 | - | 40 | - | ns |
| | | $V_{CC} = 2.7\text{ V}$ | 25 | 3.5 | - | 30 | - | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 20 | 3.0 | - | 25 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 15 | 2.5 | - | 20 | - | ns |
| | | $nB = \text{HIGH}$ | | | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | 30 | 13 | - | 40 | - | ns |
| | | $V_{CC} = 2.7\text{ V}$ | 25 | 8 | - | 30 | - | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 20 | 7 | - | 25 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 15 | 5 | - | 20 | - | ns |
| | | $n\overline{RD} = \text{LOW}$; see Figure 13 | | | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | 35 | 6 | - | 45 | - | ns |
| | | $V_{CC} = 2.7\text{ V}$ | 30 | 5 | - | 40 | - | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 25 | 4 | - | 30 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 20 | 3 | - | 25 | - | ns |
| t_{trig} | retrigger time | nB to $n\overline{A}$; see Figure 12 | | | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | - | 70 | - | - | - | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | 55 | - | - | - | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | 45 | - | - | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | 40 | - | - | - | ns |

11. Waveforms

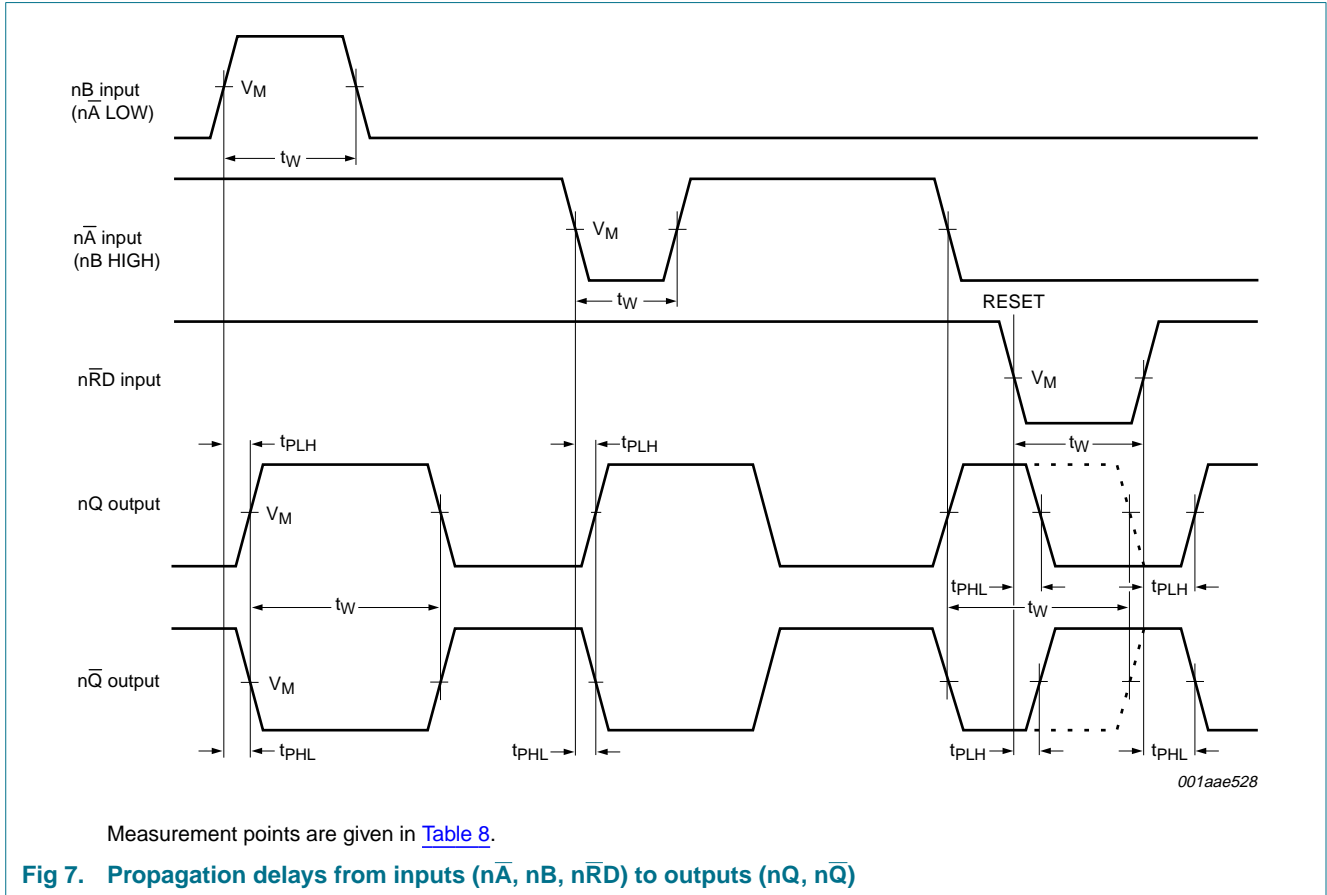


Table 8. Measurement points

| V_{CC} | V_M |
|---------------------|---------------------|
| $\geq 2.7\text{ V}$ | 1.5 V |
| $< 2.7\text{ V}$ | $0.5 \times V_{CC}$ |

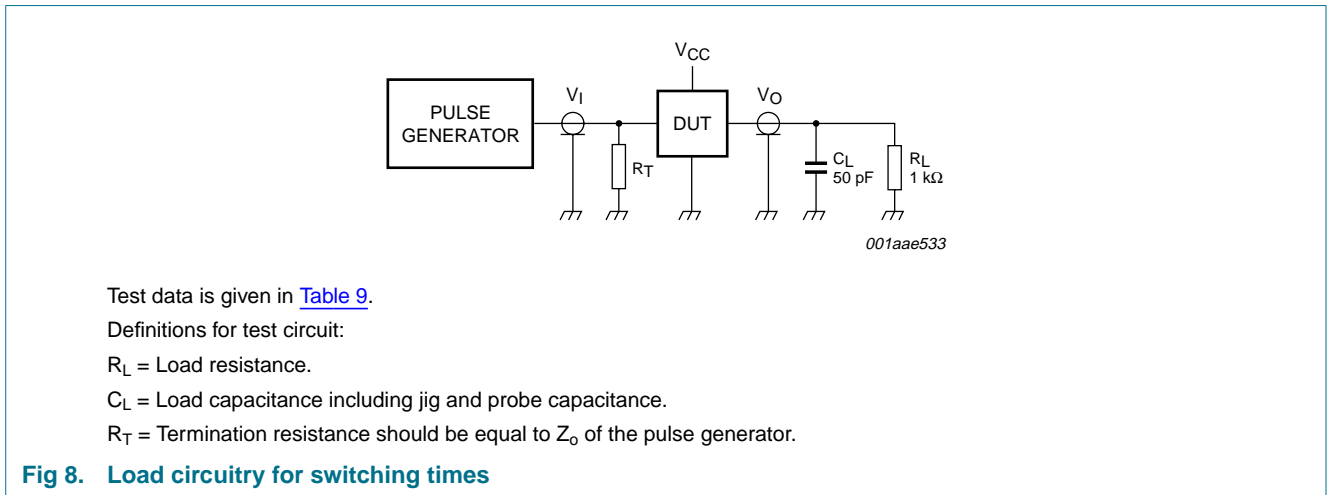


Table 9. Test data

| Supply voltage | Input | | Load | | Test |
|-----------------|-----------------|---------------------------------|----------------|----------------|-------------------------------------|
| V _{CC} | V _I | t _r , t _f | C _L | R _L | |
| < 2.7 V | V _{CC} | ≤ 2.5 ns | 50 pF | 1 kΩ | t _{PHL} , t _{PLH} |
| 2.7 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 1 kΩ | t _{PHL} , t _{PLH} |
| ≥ 4.5 V | V _{CC} | ≤ 2.5 ns | 50 pF | 1 kΩ | t _{PHL} , t _{PLH} |

12. Application information

12.1 Timing components

12.1.1 Basic timing

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.

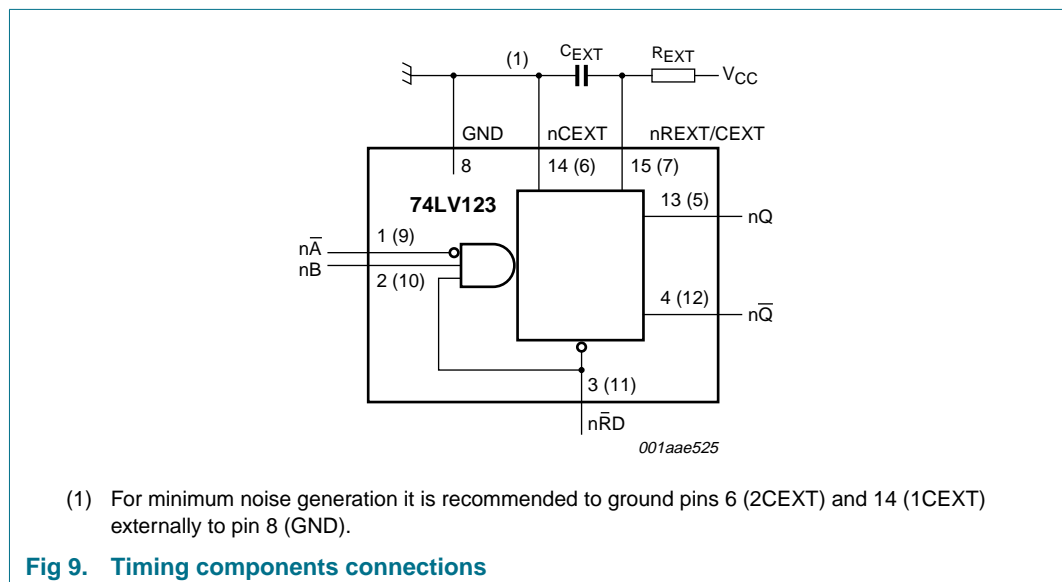


Fig 9. Timing components connections

If C_{EXT} > 10 nF, the following formula is valid: t_W = K × R_{EXT} × C_{EXT} (typ.) where:

t_W = output pulse width in ns

R_{EXT} = external resistor in kΩ

C_{EXT} = external capacitor in pF

K = constant: this is 0.45 for V_{CC} = 5.0 V and 0.48 for V_{CC} = 2.0 V (see [Figure 10](#))

The inherent test jig and pin capacitance at pin 15 and pin 7 (nREXT/CEXT) is approximately 7 pF.

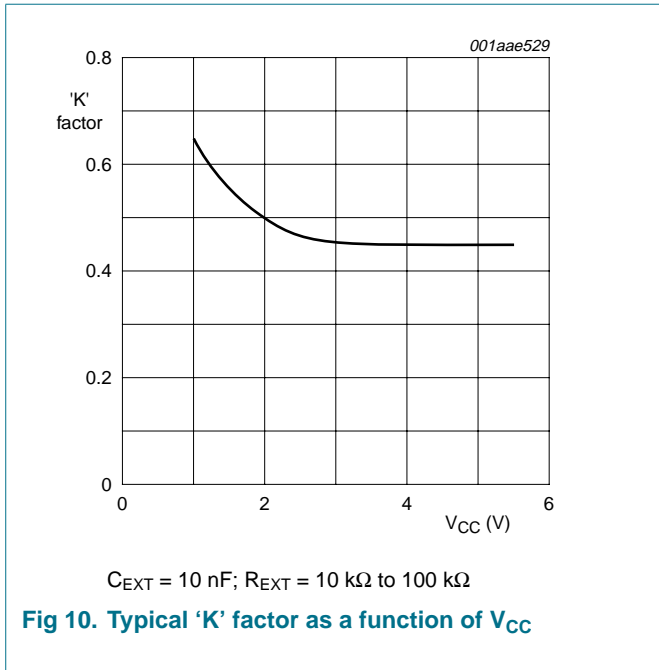


Fig 10. Typical 'K' factor as a function of V_{CC}

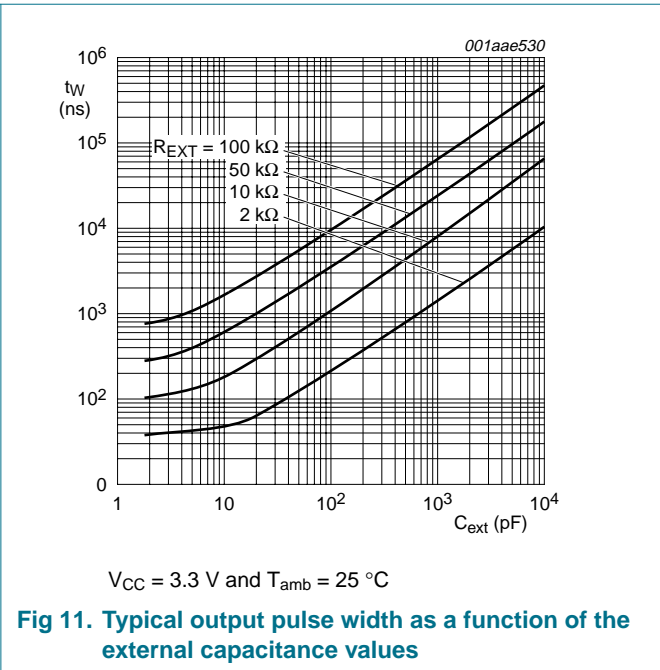


Fig 11. Typical output pulse width as a function of the external capacitance values

12.1.2 Retrigger timing

The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active going edges of the trigger pulses meets the minimum retrigger time. If C_{EXT} > 10 pF, the next formula for the set-up time of a retrigger pulse is valid:

at V_{CC} = 5.0 V: $t_{rtrig} = 30 + 0.19R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$ (typ.)

at V_{CC} = 3.0 V: $t_{rtrig} = 41 + 0.15R_{EXT} \times C_{EXT}^{0.9} \times 1 \times R_{EXT}$ (typ.)

where:

t_{rtrig} = retrigger time in ns

C_{EXT} = external capacitor in pF

R_{EXT} = external resistor in kΩ

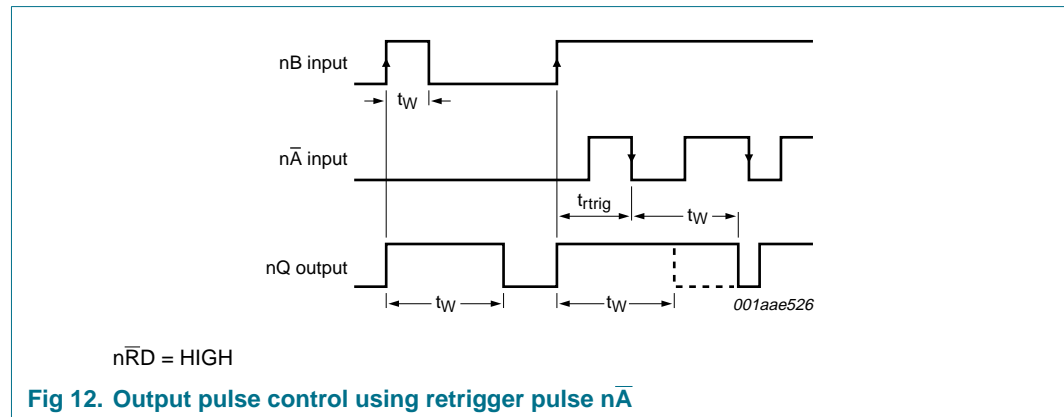


Fig 12. Output pulse control using retrigger pulse nA

12.1.3 Reset timing

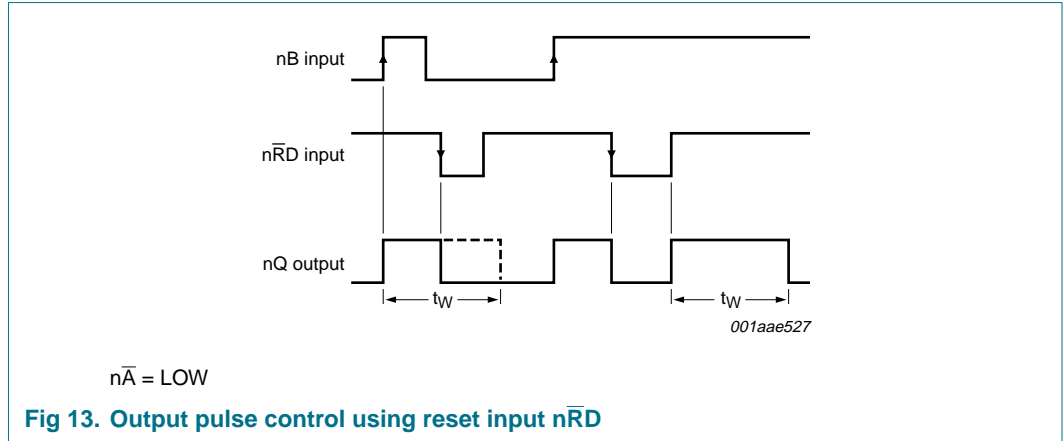


Fig 13. Output pulse control using reset input $n\bar{RD}$

12.2 Power considerations

12.2.1 Power-up

When the monostable multivibrator is powered-up, it may produce an output pulse with a pulse width defined by the values of R_{EXT} and C_{EXT} . This output pulse can be eliminated using the RC circuit on pin $n\bar{RD}$ shown in [Figure 14](#).

12.2.2 Power-down

A large capacitor (C_{EXT}) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, connect a damping diode D_{EXT} (preferably a germanium or Schottky type diode) able to withstand large current surges - see [Figure 14](#).

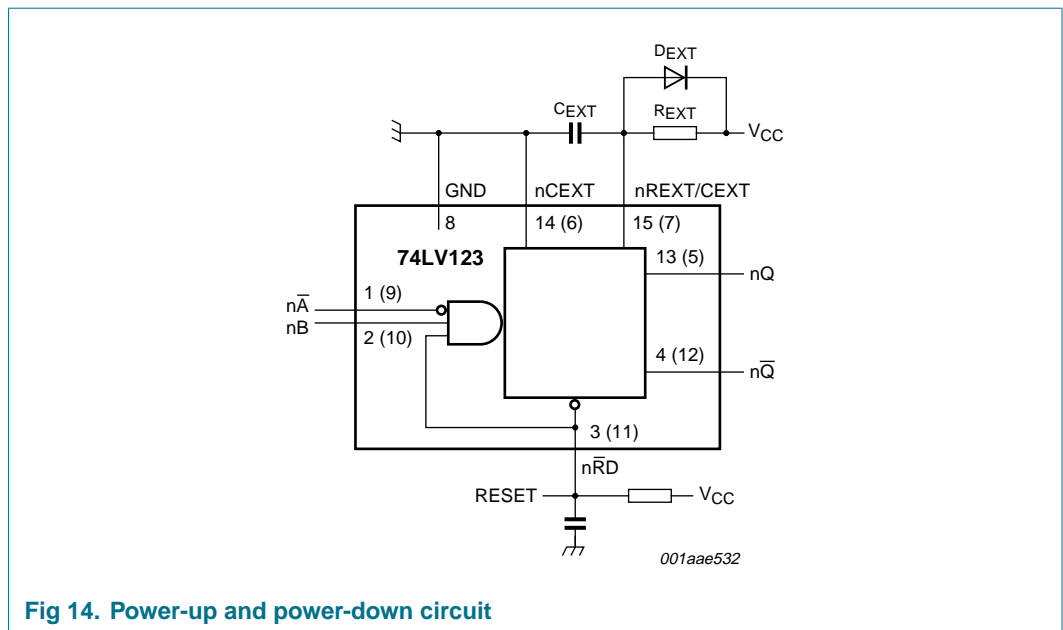


Fig 14. Power-up and power-down circuit

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

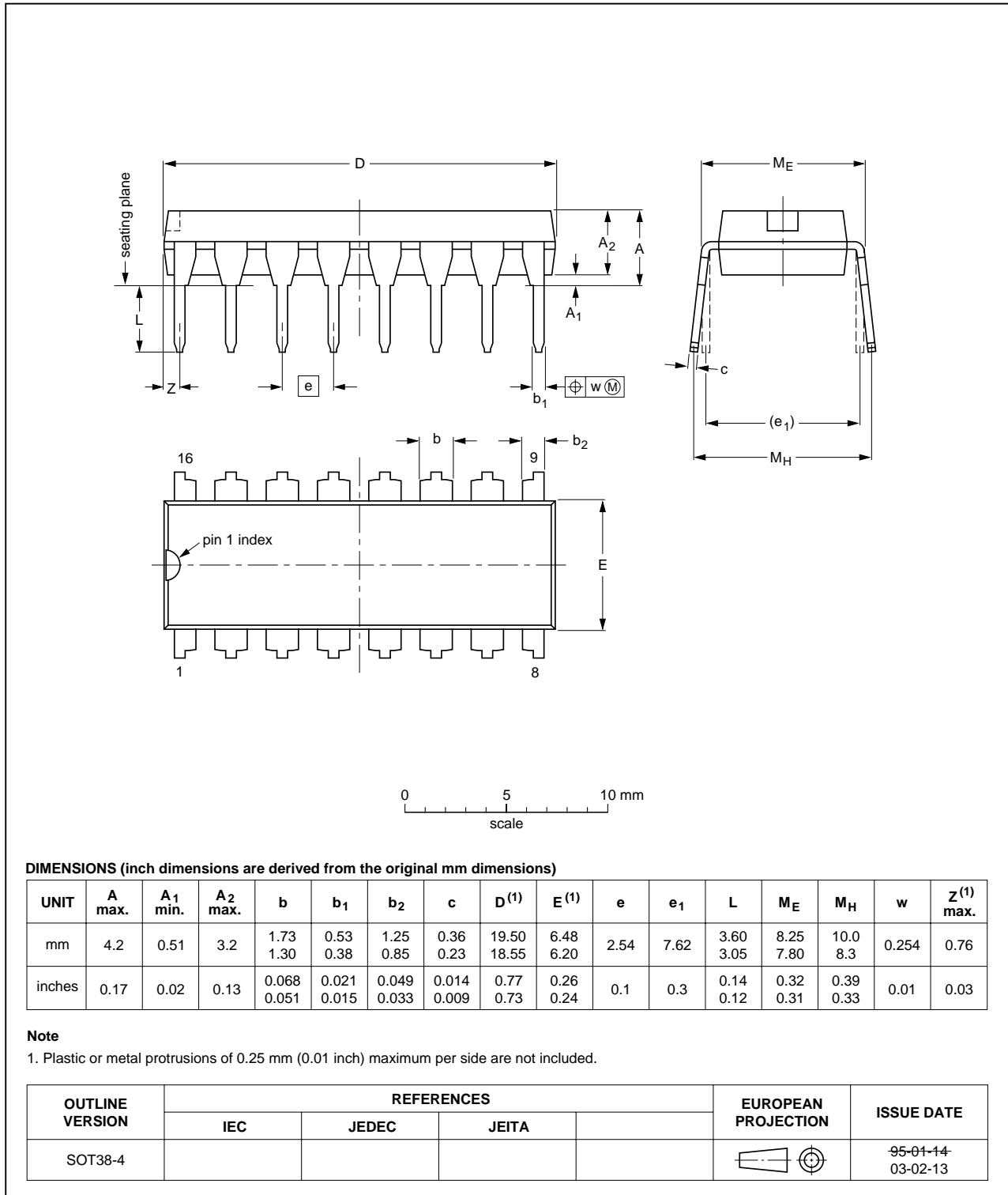


Fig 15. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

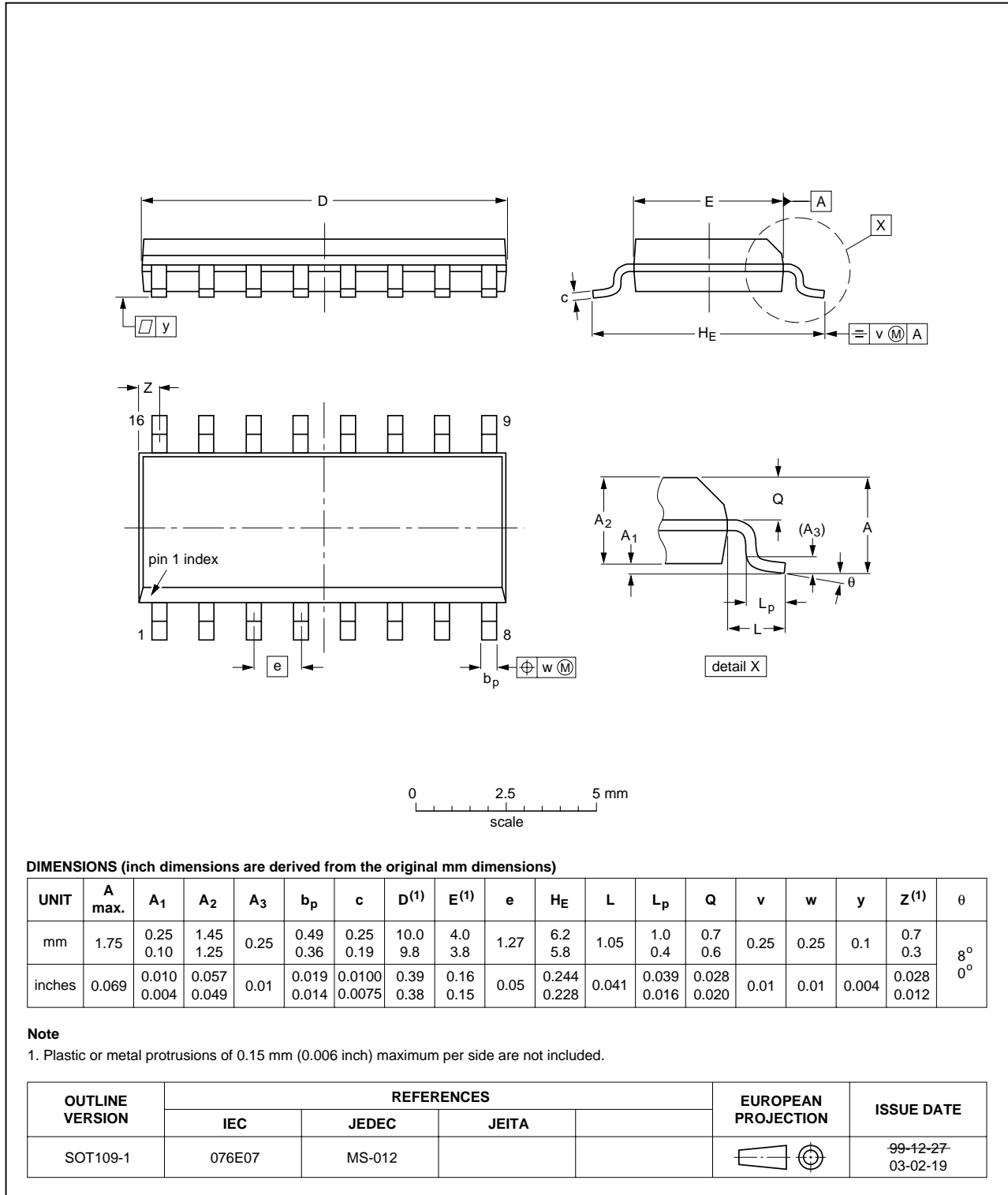


Fig 16. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

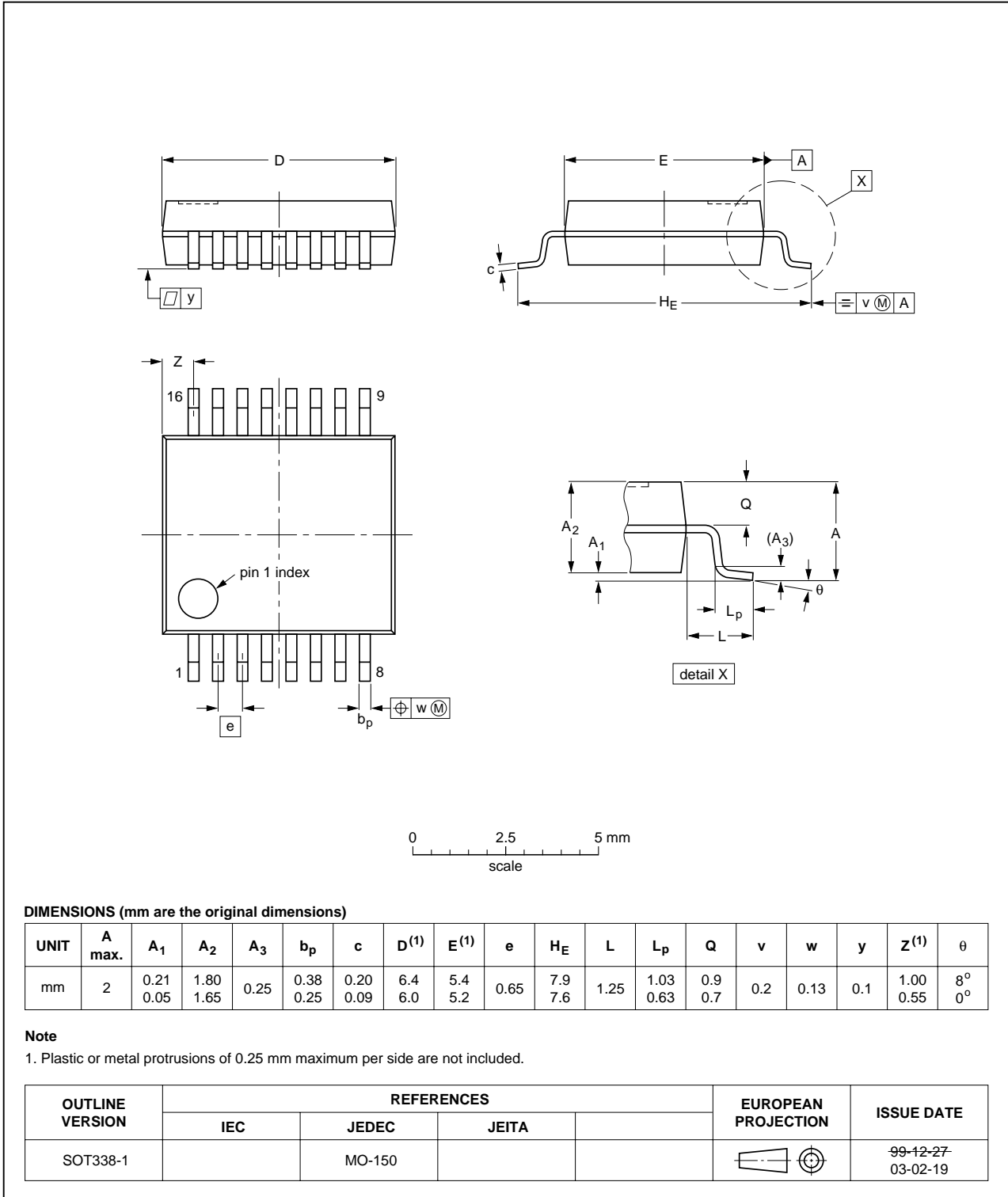


Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

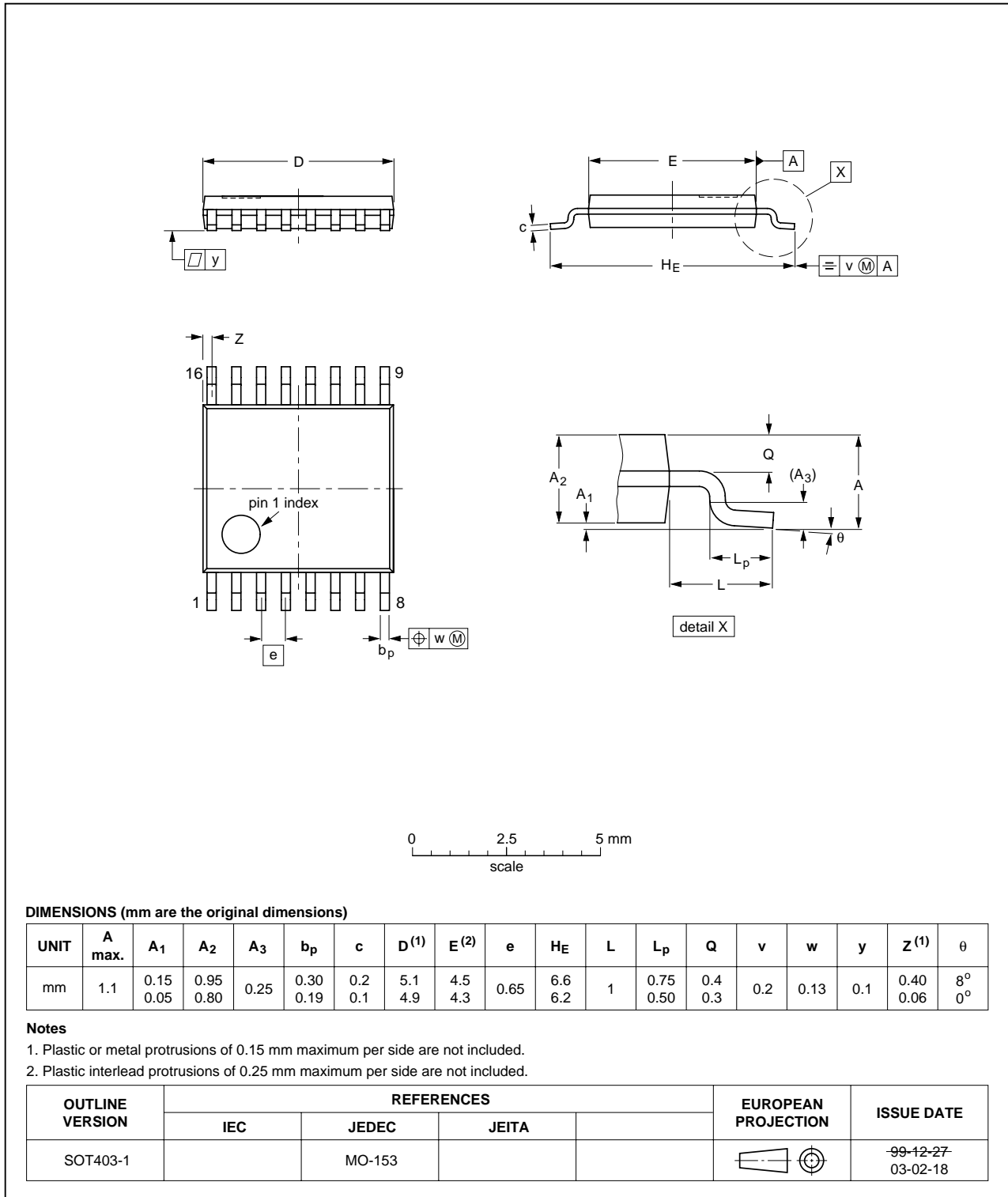


Fig 18. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

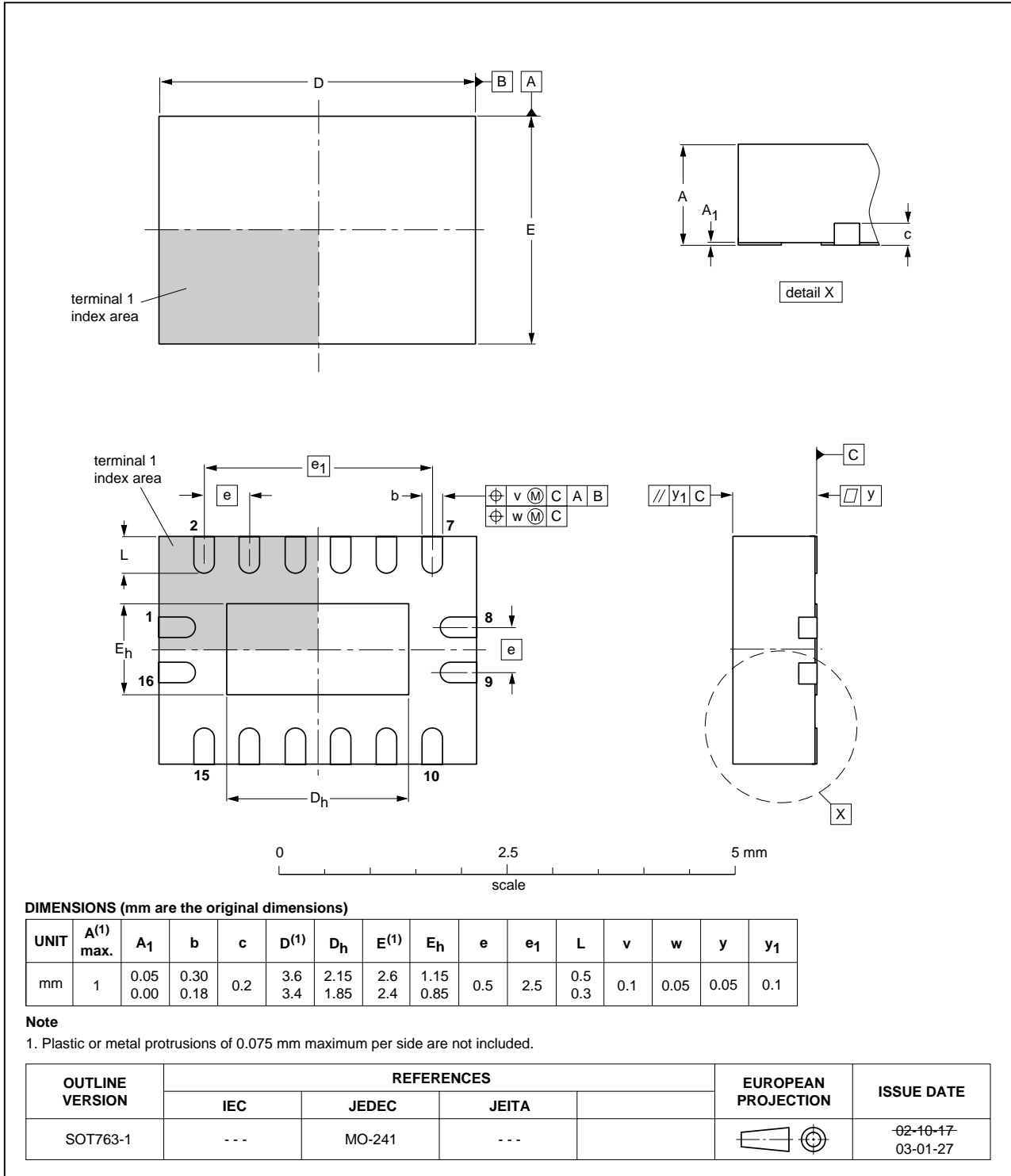


Fig 19. Package outline SOT736-1 (DHVQFN16)

14. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|-----------------------|---------------|------------|
| 74LV123_5 | 20071108 | Product data sheet | - | 74LV123_4 |
| Modifications: | • Changed: SOT38-1 changed into SOT38-4 | | | |
| 74LV123_4 | 20070919 | Product specification | - | 74LV123_3 |
| 74LV123_3 | 20030313 | Product specification | - | 74LV123_2 |
| 74LV123_2 | 19980420 | Product specification | - | 74LV123_1 |
| 74LV123_1 | 19970204 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

17. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features | 1 |
| 3 | Ordering information | 2 |
| 4 | Functional diagram | 2 |
| 5 | Pinning information | 5 |
| 5.1 | Pinning | 5 |
| 5.2 | Pin description | 5 |
| 6 | Functional description | 6 |
| 7 | Limiting values | 7 |
| 8 | Recommended operating conditions | 7 |
| 9 | Static characteristics | 8 |
| 10 | Dynamic characteristics | 10 |
| 11 | Waveforms | 12 |
| 12 | Application information | 13 |
| 12.1 | Timing components | 13 |
| 12.1.1 | Basic timing | 13 |
| 12.1.2 | Retrigger timing | 14 |
| 12.1.3 | Reset timing | 15 |
| 12.2 | Power considerations | 15 |
| 12.2.1 | Power-up | 15 |
| 12.2.2 | Power-down | 15 |
| 13 | Package outline | 16 |
| 14 | Revision history | 21 |
| 15 | Legal information | 22 |
| 15.1 | Data sheet status | 22 |
| 15.2 | Definitions | 22 |
| 15.3 | Disclaimers | 22 |
| 15.4 | Trademarks | 22 |
| 16 | Contact information | 22 |
| 17 | Contents | 23 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 8 November 2007

Document identifier: 74LV123_5