

October 1988 Revised March 2000

# **DM74LS573** Octal D-Type Latch with 3-STATE Outputs

#### **General Description**

The DM74LS573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable  $(\overline{OE})$  inputs.

This device is functionally identical to the DM74LS373, but has different pinouts.

#### **Features**

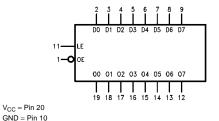
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to DM74LS373
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

## **Ordering Code:**

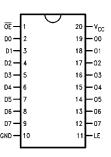
Order Number	Package Number	Package Description
DM74LS573WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS573N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

# **Logic Symbol**



## **Connection Diagram**



#### **Pin Descriptions**

Pin Names	Description
D0-D7	Data Inputs
LE	Latch Enable Input (Active HIGH)
	3-STATE Output Enable Input (Active LOW)
00-07	3-STATE Latch Outputs

#### **Function Tables**

Output Enable	Latch Enable	D	Output O
L	Н	Н	Н
L	Н	L	L
L	L	X	$Q_{O}$
Н	Х	Χ	Z

- I = I OW State
- H = HIGH State

- Z = High Impedance State
  Q<sub>O</sub> = Previous Condition of O

© 2000 Fairchild Semiconductor Corporation

www.fairchildsemi.com

# **Absolute Maximum Ratings**(Note 1)

Supply Voltage 7V Input Voltage 7V Operating Free Air Temperature Range  $0^{\circ}\text{C to } +70^{\circ}\text{C}$  Storage Temperature Range  $-65^{\circ}\text{C to } +150^{\circ}\text{C}$ 

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## **Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Input Current			-2.6	mA
I <sub>OL</sub>	LOW Level Output Current			24	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

## **Electrical Characteristics**

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$			-1.5	V
V <sub>OH</sub>	HIGH Level	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,	2.7	3.4		V
	Output Voltage	V <sub>IL</sub> = Max	2.7			
V <sub>OL</sub>	LOW Level	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,		0.35	0.5	
	Output Voltage	$V_{IH} = Min$		0.55	0.5	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min		0.25	0.4	
I	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$			1	mA
I <sub>IH</sub>	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$			20	μΑ
I <sub>IL</sub>	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA
los	Short Circuit	V <sub>CC</sub> = Max	-30		-130	mA
	Output Current	(Note 3)	-30			
Icc	Supply Current	V <sub>CC</sub> = Max			50	mA
l <sub>OZH</sub>	3-STATE Output	$V_{CC} = V_{CCH}$			20	μА
	OFF Current HIGH	$V_{OZH} = 2.7V$				
lozL	3-STATE Output	$V_{CC} = V_{CCH}$		-20		μА
	OFF Current LOW	$V_{OZL} = 0.4V$			-20	μΑ

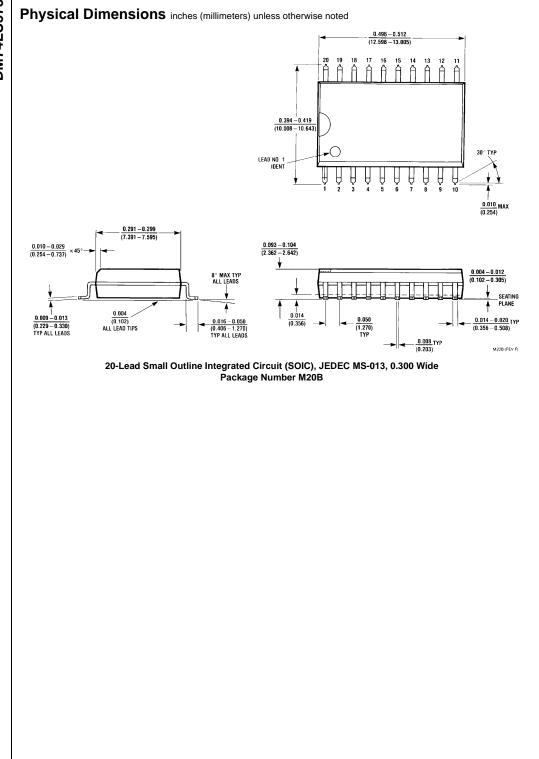
Note 2: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25$ °C.

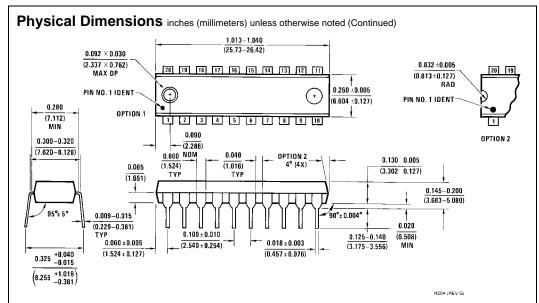
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

# **Switching Characteristics**

at  $V_{CC} = 5V$  and  $T_A = 25$  °C

		$R_L = 2 k\Omega,$ $C_L = 50 pF$			
Symbol	Parameter			Units	
		Min	Max		
t <sub>PLH</sub>	Propagation Delay		27	ns	
t <sub>PHL</sub>	Data to Q		18	115	
t <sub>PLH</sub>	Propagation Delay		36	ns	
$t_{PHL}$	LE to Q		25	115	
t <sub>PZH</sub>	3-STATE Enable Time		20	ns	
$t_{PZL}$	OE to Q		25	115	
t <sub>PHZ</sub>	3-STATE Enable Time		20	ns	
$t_{PLZ}$	OE to Q		25	115	
t <sub>S</sub> (H)	Setup Time (HIGH/LOW)	3		ns	
$t_S(L)$	Data to LE	7		115	
t <sub>H</sub> (H)	Hold Time (HIGH/LOW)	10		ns	
t <sub>H</sub> (L)	Data to LE	10		115	
t <sub>W</sub> (H)	Pulse Width (HIGH)	15			
	Data to LE	15		ns	





20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

www.fairchildsemi.com