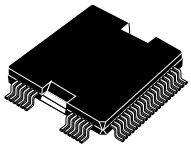
TDA7572

200W mono bridge PWM amplifier with built-in step-up converter

Preliminary Data

Features

- Input stage and gain compressor
- Over-modulation protection and current limiting
- Modulator
- DAC
- Step-up
- Mode control
- Diagnostics / safety
- Power control



HiQUAD-64

Description

TDA7572 is a highly integrated, highly versatile, semi-custom IC switch mode audio amplifier. It integrates audio signal processing and power amplification tailored for standalone remote bass box applications, while providing versatility for full bandwidth operation in either automotive or consumer audio environments. It's configured as one full bridge channel, using two clocked PWM modulators driving external, complementary FET's.

Broad operating voltage is supported, allowing operation from both 14V and 42V automotive power buses, as well as from split supplies for consumer electronics use.

A current mode control boost converter controller is provided to allow high power operation in a 14V environment. Turn-on and turn-off transients are minimized by soft muting/unmuting and careful control of offsets within the IC.

Digital Audio input is supported by an integrated one channel DAC. Sophisticated diagnostics and protection provide fault reporting via I^2C and power shutdown for safety related faults.

TDA7572 is packaged in a HiQUAD-64 package.

Table 1. Device summary

Order code	Package	Packing
TDA7572	HiQUAD-64	Tray

Contents

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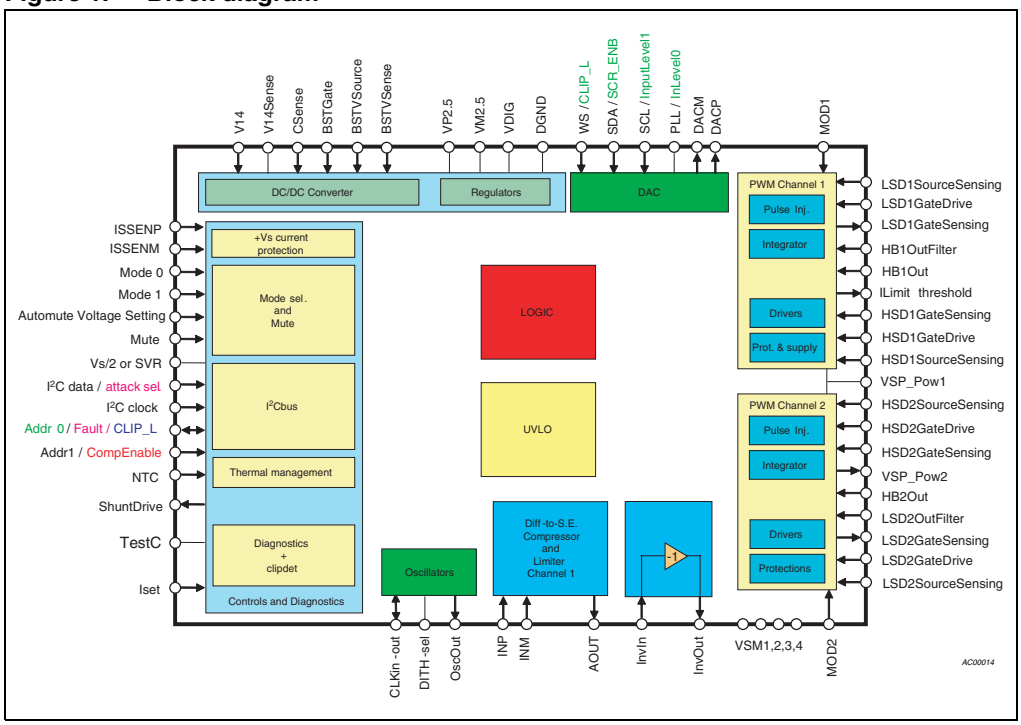
1 Detailed features

- Input Stage and Gain Compressor
  - Differential, high CMRR, analog input
  - Programmable input attenuation/gain to support up to four drive levels
  - Noiseless Gain compression of up to 16 dB with programmable attack and decay.
  - Compressor controlled by monitoring estimated THD
  - Soft mute / un-mute for pop control
- Over-modulation Protection and Current Limiting
  - Adaptive pulse injection prevents missing pulses due to over modulation which maximizes useful output swing.
  - Programmable current limiting based on FET VDS
- Modulator
  - Optimized for low distortion at low switching frequency (approximation 110KHz)
  - Dual Clocked PWM modulators for 3 state switching
  - External gain control / internal integrator components
  - Controls 4 external FETS with switching optimized for low EMI
  - Oscillation frequency selectable by I^2C
  - Anti-pop shunt driver
- DAC
  - 18bit, mono
  - I^2S inputs 38-48KHz, 96KHz, 192 KHz
  - Hybrid architecture, area optimized for Bass
  - Full bandwidth supported by off loading the interpolator function
  - Synchronization with modulator
- Step-Up
  - On board STEP-UP step up converter, synchronized to the modulator frequency
  - Drives external NFET switch
  - Externally compensated
  - Soft start and current limiting
- Mode Control
  - Critical modes controllable by mode pins for bus-less operation
  - I^2C provides additional mode control
- Diagnostics / Safety
  - Offset, short, open, overcurrent, over temperature
  - I^2C used to report errors, and for configuration control
  - Faults pin used to report errors in bus-less environment
  - Clipping reported at a separate pin
  - Abnormal supply current detection disables input power for fail safe operation
  - Output current limiting
  - Power control
  - Latching control of an external PMOS power switch for safety related faults.
  - Power is switched off for safety related faults of abnormal supply current, excessive internal or external temperature, or persistent output stage over-current that fails to be controlled by the pulse-by-pulse current limiting method

2 Interface description

I²C bus and mode control pins are use to control operation. Default values of all the operating modes are deterministic, some of these values are intrinsic to the IC and some are determined by configurations pins. The configuration pins are read at power-up and copied into registers, which may later be modified using the I²C bus, if one is present. This allows varied operation in an environment where NOI²C bus is present, while allowing full control and override of pin programmed modes when used with I²C.

Figure 1. Block diagram



3 Pins description

Figure 2. Pins connection (top view)

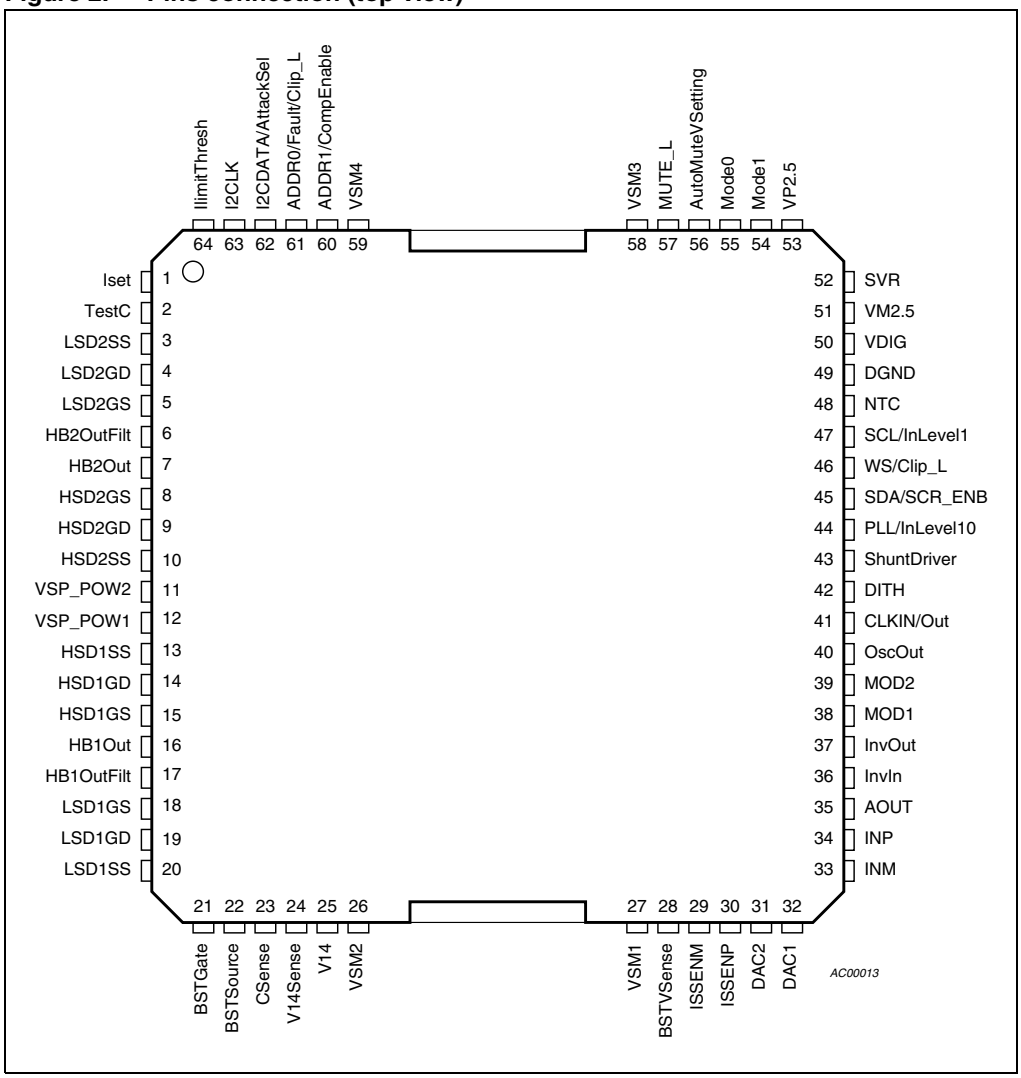


Table 2. Pin list by argument

Pin #	Pin name	Description
On/Off Circuitry		
11	VSP_POW2	Positive supply power for low power, non gate-drive functions with a separate bonding to power the gate drive of modulator two
53	VP2.5	+2.5V analog supply output
51	VM2.5	-2.5 V analog supply output
50	VDIG	5V logic supply decoupling
49	DGND	Digital gnd
52	SVR	Vs/2 analog reference filter capacitor. Reference for input stage.
55	Mode0	Mode control bit0, selects standby/normal/ I^2C/diagnostic operation
54	Mode1	Mode control bit1, selects standby/normal/ I^2C/diagnostic operation
57	MUTE_L	Mute input and / or timing cap, assertion level low
56	AutoMuteVSetting	Auto-mute Voltage Setting
Input/ Gain Compressor		
34	INP	Non inverting audio input
33	INM	Inverting audio input
35	AOUT	Compressed Audio Output
		Input Stage gain selection – see PLL pin in DAC *Section 8*
		Compressor attack/decay select – see I^2C data pin in DAC *Section 8*
Inverter		
36	InvIn	Inverter input
37	InvOut	Inverter Output
Modulator		
64	IlimitThresh	Output stage Current Limiting trip voltage set point
32	LVLSFT	Gain program pin for SVR to HVCC level shifting
38	MOD1	Modulator1 Inverting / Summing node
20	LSD1SS	Lowside1 Source Sensing
19	LSD1GD	Lowside1 Gate Drive
18	LSD1GS	Lowside1 Gate sense
17	HB1OutFilt	Half bridge1 post-LC filter – for diagnostics
16	HB1Out	Half-bridge1 output, HSD 1 drain sense, LSD1 Drain Sense
15	HSD1GS	Highside1 Gate sense
14	HSD1GD	Highside1 Gate Drive
13	HSD1SS	Highside1 Source sense
12	VSP_POW1	Positive supply voltage connection for gate drive circuitry

Table 2. Pin list by argument (continued)

Pin #	Pin name	Description
39	MOD2	Modulator2 Inverting / Summing node
10	HSD2SS	Highside2 Source sense
9	HSD2GD	Highside2 Gate Drive
8	HSD2GS	Highside2 Gate sense
7	HB2Out	Half-bridge2 output, HSD 1 drain sense, LSD1 Drain Sense
6	HB2OutFilt	Half bridge2 post-LC filter – for diagnostics
5	LSD2GS	Lowside2 Gate sense
4	LSD2GD	Lowside2 Gate Drive
3	LSD2SS	Lowside2 Source Sense
27	VSM1	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
26	VSM2	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
58	VSM3	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
59	VSM4	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
43	ShuntDriver	Shunt Driver
DC-DC		
28	BSTVSense	Voltage feedback input for Voltage Booster
22	BSTSource	Boost Converter NFET Source
21	BSTGate	Boost Converter NFET gate drive
23	CSense	Inverting input for Booster Current Sensing and Digital Test Enable (operating when is more then about 3V under the V14 pin level)
24	V14Sense	Non-inverting input for Booster Current Sensing
25	V14	Power for Boost converter gate drive and Output LSD's
Oscillator		
41	CLKIN/Out	Clock input
42	DITH	Dither capacitor
40	OscOut	Oscillator output
Diagnostics / Bus		
62	I^2CDATA/AttackSel	I^2C data (I^2C mode) Compressor aggressiveness selection (non-bus mode)
63	I^2CLK	I^2C Clock

Table 2. Pin list by argument (continued)

Pin #	Pin name	Description
61	ADDR0/Fault/Clip_L	I^2C address set (I^2C mode) Fault output in non bus mode (non-bus mode) Clipping indicator, assertion level low, (when DAC is enabled)
60	ADDR1/CompEnable	I^2C address set (I^2C mode) Compressor Enable/disable (non-bus mode)
48	NTC	Connection for NTC thermistor
2	TestC	Test cap used to generate the slow current pulses
1	ISet	Program pin for current level used in Short/Open test
30	ISSENP	Supply non-inverting current sense
29	ISSENM	Supply inverting current sense
DAC		
46	WS / Clip_L	I^2S Word select / Clipping indicator, assertion level low (non-DAC mode)
45	SDA/SCR_ENB	I^2C serial data / SCR ENABLE (non DAC mode)
47	SCL/ InLevel1	I^2C serial data bit clock/ Input Level selection bit1 (non-DAC mode)
44	PLL/InLevel0	DAC clock PLL filter/ Input Level selection bit 0 (non-DAC mode)
31	DAC2	DAC output voltage p
32	DAC1	DAC output voltage n

Table 3. Pin list by pin

Pin #	Pin name	Description
1	Iset	Program pin for current level used in Short/Open test
2	TestC	Test cap used to generate the slow current pulses
3	LSD2SS	Lowside2 Source Sense
4	LSD2GD	Lowside2 Gate Drive
5	LSD2GS	Lowside2 Gate sense
6	HB2OutFilt	Half bridge2 post-LC filter – for diagnostics
7	HB2Out	Half-bridge2 output, HSD 1 drain sense, LSD1 Drain Sense
8	HSD2GS	Highside2 Gate sense
9	HSD2GD	Highside2 Gate Drive
10	HSD2SS	Highside2 Source sense
11	VSP_POW2	Positive supply power for low power, non gate-drive functions with a separate bonding to power the gate drive of modulator two
12	VSP_POW1	Positive supply voltage connection for gate drive circuitry
13	HSD1SS	Highside1 Source sense
14	HSD1GD	Highside1 Gate Drive
15	HSD1GS	Highside1 Gate sense

Table 3. Pin list by pin (continued)

Pin #	Pin name	Description
16	HB1Out	Half-bridge1 output, HSD 1 drain sense, LSD1 Drain Sense
17	HB1OutFilt	Half bridge1 post-LC filter – for diagnostics
18	LSD1GS	Lowside1 Gate sense
19	LSD1GD	Lowside1 Gate Drive
20	LSD1SS	Lowside1 Source Sensing
21	BSTGate	Boost Converter NFET gate drive
22	BSTSource	Boost Converter NFET Source
23	CSense	Inverting input for Booster Current Sensing and Digital Test Enable (operating when is more then about 3V under the V14 pin level)
24	V14Sense	Non-inverting input for Booster Current Sensing
25	V14	Power for Boost converter gate drive and Output LSD's
26	VSM2	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
27	VSM1	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
28	BSTVSense	Voltage feedback input for Voltage Booster
29	ISSENM	Supply inverting current sense
30	ISSENP	Supply non-inverting current sense
31	DAC2	Half VCC (VSP- VSM)/2 Used for output stage reference.
32	DAC1	Gain program pin for SVR to HVCC level shifting
33	INM	Inverting audio input
34	INP	Non inverting audio input
35	AOUT	Compressed Audio Output
36	InvIn	Inverter input
37	InvOut	Inverter Output
38	MOD1	Modulator1 Inverting / Summing node
39	MOD2	Modulator2 Inverting / Summing node
40	OscOut	Oscillator output
41	CLKIN/Out	Clock input
42	DITH	Dither capacitor
43	ShuntDriver	Shunt Driver
44	PLL/InLevel0	DAC clock PLL filter/ Input Level selection bit 0 (non-DAC mode)
45	SDA/SCR_ENB	I^2C serial data / SCR ENABLE (non DAC mode)
46	WS / Clip_L	I^2S Word select / Clipping indicator, assertion level low (non-DAC mode)
47	SCL/ InLevel1	I^2C serial data bit clock/ Input Level selection bit1 (non-DAC mode)
48	NTC	Connection for NTC thermistor

Table 3. Pin list by pin (continued)

Pin #	Pin name	Description
49	DGND	GND logic supply decoupling
50	VDIG	5V logic supply decoupling
51	VM2.5	-2.5 V analog supply output
52	SVR	Vs/2 analog reference filter capacitor. Reference for input stage.
53	VP2.5	+2.5 V analog supply output
54	Mode1	Mode control bit1, selects standby/normal/I^2C/diagnostic operation
55	Mode0	Mode control bit0, selects standby/normal/ I^2C/diagnostic operation
56	AutoMuteVSetting	Auto-mute Voltage Setting
57	MUTE_L	Mute input and / or timing cap, assertion level low
58	VSM3	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
59	VSM4	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
60	ADDR1/CompEnable	I^2C address set (I^2C mode) Compressor Enable/disable (non-bus mode)
61	ADDR0/Fault/Clip_L	I^2C address set (I^2C mode) Fault output in non bus mode (non-bus mode) Clipping indicator, assertion level low, (when DAC is enabled)
62	I^2CDATA/AttackSel	I^2C data (I^2C mode) Compressor aggressiveness selection (non-bus mode)
63	I^2CLK	I^2C Clock
64	IlimitThresh	Output stage Current Limiting trip voltage setpoint

4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameters	Test Conditions	Min.	Max.	Units
V_{SP}	Supply voltage		V_{SM} -0.6	V_{SM} +58	V
V_{peak}	Peak supply voltage	(V_{S+} - V_{S-}) time ≤ 50ms		68	V
V_{DATA}	Data pin voltage	w.r.t Dgnd	V_S—0.6	6V	V
T_J	Junction temperature		-40	150	C
T_{Stg}	Storage temperature		-55	150	C
P_{DMAX}	Power Dissipation	Any operating condition For thermal budgeting		2.5	W

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameters	Value	Units
$R_{Th\ j\text{-}case}$	Thermal resistance junction to case	3	°C/W

4.3 Electrical characteristics

Unless otherwise specified, all ratings below are for -40°C < T_J < 125°C, V_{SP} = 42V, V_{SM} = 0V and the application circuit of *Figure 12*. Operation of the IC above this junction temperature will continue without audible artifacts until thermal shutdown, but these parameters are not guaranteed to be within the specifications below. F_{PWM}=110KHz, Booster not enabled.

4.3.1 Operating voltage and current

Table 6. Operating voltage and current

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{SP42}	Operating voltage 42V automotive range	Normal operation without audible defects required Single ended supply 42V configuration, V_{SM}=0	30	42	58	V
V_{SP14}	Operating voltage 14.4V automotive range	Normal operation without audible defects required Single ended supply 14V configuration, V_{SM}=0	9	14.4		

Table 6. Operating voltage and current (continued)

Symbol	Parameters	Test conditions		Min.	Typ.	Max.	Units
V_{SPLIT}	Operating voltage V_{SP} - V_{SM} split supply rails	Normal operation required Split supply application configuration, $V_{SM}<V_{SVR}-4$, $V_{SP}>V_{SVR}+4$		8	48	58	V
I_{stdby}	Stand-by current	IC in standby, Mode0, and Mode1 low V_s = 42V				50 at T = 25°C 10 at T = 85°C	µA
$I_{tristate}$	Tristate current	Outputs tristated Booster not running, F_{pwm} = nominal	V14		13	20	mA
			VSP		15	25	
I_{MUTE}	Mute mode current	MUTE asserted,	V14		10		mA
			VSP		20		

4.3.2 Under voltage lockout

Table 7. Under voltage lockout

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{LimAM}	AutomuteVSetting pin voltage limit	Voltage limit respect to the SVR pin Allowed voltage range on Automute pin	0.5		2.1	V
VSP UVLO						
V_{AM}	Auto-mute supply voltage VSP	Mute is forced if VSP-VSVR or VSVR-VSM is less than this value VautomuteVSetting-V_{SVR}=VVSVR	-15%	VVSVR* 7	+15%	V
VPO-	Auto-tristate supply voltage VSP **negative slope**	The IC is set in tristate if VSP-VSM is less than this value Vautomute VSetting-V_{SVR}=VVSVR	-15%	VVSVR *12	+15%	V
VPO+	Auto-tristate supply voltage VSP **positive slope**	The IC is set out from tristate if VSP-VSM is higher than this value Vautomute VSetting-V_{SVR}=VVSVR	-15%	VVSVR *13	+15%	V
V_U	Auto-tristate supply voltage VSP Relative maximum value	The IC is set in tristate if VSP-VSM is more than this value Vautomute VSetting-V_{SVR}=VVSVR	-15%	VVSVR* 48	+15%	V
V_{UC}	Auto-tristate supply voltage VSP Absolute maximum value	The IC is set in tristate if VSP-VSM is higher than this value	60	63	66	V

Table 7. Under voltage lockout (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V14 – UVLO						
V14-	Auto-tristate supply voltage V14 **negative slope**	The IC is kept in tristate if 14V - VSM become lower than this value	5.5		7	V
V14+	Auto-tristate supply voltage V14 **positive slope**	The IC is goes out from tristate if 14V-VSM become higher than this value	6.5		8	V
V14h	Auto-tristate 14V voltage hysteresis	Comparator hysteresis for auto-tristate threshold	0.8			V
V14su	Step-up tristate	The step-up is in tristate when voltage lower than this threshold	5		8	V
V14mute-	Auto-mute supply voltage V14 **negative slope**	The IC goes in mute if 14V-VSM become lower than this value	V14- + 0.7V		V14- + 1.2V	V
V14mute+	Auto-mute supply voltage V14 **positive slope**	The IC goes in play if 14V-VSM become higher than this value	V14V+ + 40mV		V14V+ + 170mV	
SVR – UVLO						
Vsvr-	Auto-tristate SVR voltage **negative slope**	The IC is kept in tristate if VSvr - VSM become less than this value Vautomute VSetting-V_{SVR}=VVSVR	-15%	5 x VVSVR	+15%	V
Vsvr+	Auto-tristate SVR voltage **positive slope**	The IC is goes out from tristate if Vvr - VSM become higher than this value Vautomute VSetting-V_{SVR}=VVSVR	-15%	6 x VVSVR	+15%	V
VPOH	Auto-tristate SVR Voltage hysteresis	Comparator hysteresis for auto-tristate threshold Vautomute VSetting-V_{SVR}=VVSVR	0.40 X VVSVR		1.2V X VVSVR	V

4.3.3 Input stage

Table 8. Input stage

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Input diff. amp./ gain attenuator						
R_{IN}, No compression	Input resistance	INLEVEL1=0, INLEVEL0=0	-30%	20	+30%	KΩ
		INLEVEL1=0, INLEVEL0=1	-30%	12	+30%	
		INLEVEL1=1, INLEVEL0=0	-30%	22	+30%	
		INLEVEL1=1, INLEVEL0=1	-30%	12	+30%	
R_{IN} max compression		INLEVEL1=0, INLEVEL0=0	-30%	15.6	+30%	
		INLEVEL1=0, INLEVEL0=1	-30%	12	+30%	
		INLEVEL1=1, INLEVEL0=0	-30%	16	+30%	
		INLEVEL1=1, INLEVEL0=1	-30%	12	+30%	
V_{InMax}	Input clipping level Voltage level of the input that trespassed cause clipping in the preamplifier	INLEVEL1=0, INLEVEL0=0	2			V_{RMS}
		INLEVEL1=0, INLEVEL0=1	7			V_{RMS}
		INLEVEL1=1, INLEVEL0=0	2.6			V_{RMS}
		INLEVEL1=1, INLEVEL0=1	9.5			V_{RMS}
		INLEVEL1=1,INLEVEL0=1 Not tested in production	-10		+10	
A_{IN_0}	Input stage gain	(V_{AOUT}-V_{SVR}) / (VInP-VinM) INLEVEL1=0, INLEVEL0=0, no compression	-4	-3	-2	dB
A_{IN_2}		(V_{AOUT}- V_{SVR}) / (VInP-VinM) INLEVEL1=0, INLEVEL0=1, no compression	-15	-14	-13	dB
A_{IN_1}		(V_{AOUT}- V_{SVR}) / (VInP-VinM) INLEVEL1=1, INLEVEL0=0 no compression	-6.3	-5.3	-4.3	dB
A_{IN_3}		(V_{AOUT}- V_{SVR}) / (VInP-VinM) INLEVEL1=1, INLEVEL0=1, no compression	-17.6	-16.6	-15.6	dB
V_{outH}	AOUT output voltage swing	With respect to SVR, 10K loading to a buffered version of SVR	2			V
V_{outL}	AOUT output swing	With respect to SVR, 10K loading to a buffered version of SVR			-2	V
$AOUT_{THD}$	THD	Vin=1Vrms, f=20-20KHz, INLEVEL1=0, INLEVEL0=0, no compression		0.01	0.05	%

Table 8. Input stage

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
	Output slew rate	Vin=1KHz square wave, 2Vpp, INLEVEL1=0, INLEVEL0=0, no compression Time to transition from 10% to 90%			8	µS
	AOUT clip detector	Duty cycle of the Clipping signal when there is 5% distortion at the output of AOUT, f=1KHz, R_L =10kOhm	TBD			%
			15		25	
f_{-3dB}	Frequency response	Vin=1Vrms, INLEVEL1=0, INLEVEL0=0	20			KHz
CMRR	Common Mode Rejection Ratio	V_{CM}=1V_{RMS} @1KHz CMRR= A_{VDIFF}/A_{VCM} INLEVEL1=0, INLEVEL0=0 No compressor	47			dB
CG	Common gain	V_{CM}=1V_{RMS} @1KHz INLEVEL1=0, INLEVEL0=0 No compressor	51			dB
CG	Common gain	V_{CM}=1V_{RMS} @1KHz INLEVEL1=1, INLEVEL0=0 No compressor	51			dB
CG	Common gain	V_{CM}=1V_{RMS} @1KHz INLEVEL1=0, INLEVEL0=1 No compressor	51			dB
CG	Common gain	V_{CM}=1V_{RMS} @1KHz INLEVEL1=1, INLEVEL0=1 No compressor	51			dB
PSRR	Power Supply Rejection, Vsp supply	freq<10KHz	60	80		dB
V_{offset}	Output offset	V_{Offset} with respect to SVR Rin=100 ohms, Mute state	-4	0	+4	mV
Eno	Noise	Noise at output of this stage f = 20-20KHz, R_{input} = 100ohms A weighting		7	10	µV_{RMS}
Gain compressor						
	Maximum attenuation	INLEVEL1=0, INLEVEL0=0	-21	-19	-17	dB
		INLEVEL1=0, INLEVEL0=1	-30	-28	-26	
		INLEVEL1=1, INLEVEL0=0	-25	-23	-21	
		INLEVEL1=1, INLEVEL0=1	-34	-32	-30	

Table 8. Input stage

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
	Attenuation step size	INLEVEL1=0, INLEVEL0=0	0.5-0.25	0.5	0.5+ 0.25	dB
		INLEVEL1=0, INLEVEL0=1	0.44- 0.25	0.44	0.44+ 0.25	
		INLEVEL1=1, INLEVEL0=0	0.55- 0.25	0.55	0.55+ 0.25	
		INLEVEL1=1, INLEVEL0=1	0.48- 0.25	0.48	0.48+ 0.25	
	Gain Change ZC comparator offset (in the diff. – S.E. block) offset	Observed at AOUT pin ZC crossing must be detected within 50mV of the actual zero crossing,	-80		80	mV
	Gain Change ZC comparator offset (in the diff. – S.E. block) offset	Observed at InvOut pin ZC crossing must be detected	-220		+220	mV
Mute						
	Mute attenuation	Mute pin voltage = Dgnd Vin=1Vrms	90			dB
	Charge current	Mute Pin Voltage(57) = 1.5V	-30%	100	+30%	µA
	Discharge current	Mute Pin Voltage(57) = 1.5V	-30%	100	+30%	µA
	Mute threshold	Maximum voltage where we must be in complete mute			1.5	V
	Unmute threshold		2.5			V
	Mute to unmute transition voltage		0.2	0.3	0.42	V
	Vol	IC in mute mode, FastMute=1 Iout=0			Digital GND + 0.1	V
	Voh	IC in unmute, Iout=0	$V_{DIGITAL}$-0.1			V
	Fast mute Resistance	FASTMUTE=1 Vmutepin=1.5Volts	420	550	680	Ohm

4.3.4 Oscillator

Table 9. Oscillator

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Internal oscillator						
F_{PWM_NOM}	Switching frequency	PWMCLOCK=[0 1]	100K	120	140K	KHz
		PWMCLOCK=[1 0]		F_{PWM_NOM} *2		
		PWMCLOCK=[0 0]		F_{PWM_NOM} /2		
CLK_{DC}	Duty cycle		48	50	52	%
V_{CLK_High}	Maximum voltage level	Clock output high value Load = 20Kohm and 100pF to buffered SVR	V_{P25}-0.1		V_{P25}	V
V_{CLK_Low}	Minimum voltage level	Clock output low value Load = 20Kohm and 100pF to buffered SVR	V_{M25}-0.1		V_{M25}	V
$V_{CLK-P-P}$	Peak-peak voltage	Load = 20Kohm and 100pF to SVR	-10%	4.7	+10%	V
	Dither cap charge current	Dither pin voltage= 2.5V	-20%	100	+20%	µA
	Dither cap discharge current		-20%	100	+20%	µA
	Peak-peak dither voltage swing		1.4	1.6	1.7	V
	Dither external clock determination	Voltage at the dither pin at to select external clock function	VDIG-0.2			V
	No dither	Voltage at the dither pin at which no dither will occur			VDGND +0.2	V
	Peak F_{PWM} increase due to dither	Cdither=100nF	+8	+10	+12	%
	Peak F_{PWM} decrease due to dither	Cdither=100nF	-8	-10	-12	%
	Triangular peak value		VGND+ 1V		VDIG- 1V	

4.3.5 Modulator

Table 10. Modulator

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Integrator op. amp.						
Int_Voff	Input offset voltage		-2.5		+2.5	mV
Int_ibias	Input bias current	Guaranteed by design			500	nA
T_{off}	Maximum duty cycle	V_{sp} =1 4.4			1.1	µs

4.3.6 Gate drive and output stage control

Table 11. Gate drive and output stage control

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{OL_LSD}	LSG low voltage	I_{sink} = 0.5A I_{sink} = 20mA			1.75 0.080	V
V_{OH_LSD}	LSG high voltage	I_{source} = 0.5A I_{source} = 20mA	7 9.2			V
V_{OL_HSD}	HSG low voltage	I_{sink} = 0.5A I_{sink} = 20mA			VSP-7 VSP-9.2	V
V_{OH_HSD}	HSG high voltage	I_{source} = 0.5A I_{source} = 20mA	VSP-1.75 VSP-0.080			V
	HSG low Z drive t_{delay}	After a commutation	2		10	µs
	LSG low Z drive t_{delay}	After a commutation	2		10	µs
	HSG HiZ sink current	$V_{HSG}=V_{SP}$ t>5uS			150	mA
	LSG HiZ source current	$V_{LSG}=V_{SM}$, t>5uS			150	mA
Overcurrent sensing						
$I_{limThresh}$	Range of $I_{lim\ Trthresh}$		0.3		1.1	V
Vilim	Vilim	Engagement of the current limiting VlimitTreshold=1V w.r.t. VM2p5	Vlim* 3.0		Vlim* 5.0	V
	Vitrip	Start of cycle by cycle current limiting	-15%	Vlim * 6.0	+15%	V
Anti-shoo through						
PV_{GS_ON}	PFET gate voltage that will block NFET enhancement		-2.5			V
PV_{GS_OFF}	PFET gate voltage that will allow NFET enhancement				-3.5	V

Table 11. Gate drive and output stage control (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
NV_{GS_ON}	NFET gate voltage that will block PFET enhancement		2.5			V
NV_{GS_OFF}	NFET gate voltage that will allow PFET enhancement				3.5	V

4.3.7 Diagnostics

Table 12. Diagnostics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Turn-on diagnostics/ Power up diagnostics						
I_{TEST}	Test current for short/open		-15%	2.45/(3* Riset)	+15%	mA
		R_i set = 56ohm	-15%	15	+15%	
	R_{ISET} allowed range		5.6			ohm
V_{LSSHRT}	Short threshold to lower supply rail				-Vs +1	V
V_{NOP}	Normal operation thresholds		-Vs+2		-Vs+5.5	V
	Short to supply		-Vs+8			
	Shorted load				6	mV
	Normal load		.025		1	V
	Open load		2			V
	Test charge current		-30%	10µA	+30%	µA
t_{TEST}	Test time		60	80	100	ms
Permanent Diagnostics						
V_{offACT}	DC offset detected		+-3			Volts
V_{offACT}	DC offset not detected, normal operation allowed				+-1.2	Volts
Temperature						
T_{WARN}	Chip thermal warning		135	150	165	°C
	Chip thermal warning hysteresis		3	5	7	
T	Chip thermal shutdown		155	160	175	°C
	Shutdown hysteresis		3	5	7	°C
	External thermal warning		-10%	V_{DIG} *.4	+10%	V
	External thermal warning hysteresis		Vdig*0.030		Vdig*0.044	V

Table 12. Diagnostics (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
	Ext thermal shut down		-15%	V_{DIG} *.36	+15%	V
	Ext thermal shut down hysteresis		Vdig*0.032		Vdig*0.046	V
Supply I_{sense}						
	Supply sense trip voltage		16	20	25	mV
	AOUT levels that allow sensing of supply current				3	V
	Duration of AOUT under threshold to allow supply current sensing		-25%	80	+25%	ms
I_{ssenp}			200		700	µA
I_{ssenM}			-500		500	nA

4.4 Voltage booster

Table 13. Voltage booster

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Current mode control topology						
BST_{DCMAX}	Max duty cycle				88	%
BST_{DCMIN}	Min duty cycle		0			%
BSTREF	Vref		-8%	2.5	+8%	V
$IBIAS_{BSTREF}$	V_{sense} input bias current		-100		100	nA
V_{SENSE_UL}	V_{sense} pin allowed voltage range		-0.6		58	V
BSTVGain	Voltage-error gain ΔDuty cycle/ΔBSTVSense		0.4	0.8	1.2	%D.C. per mV
$BSTDC_{NOM}$	Nominal duty cycle		55		65	%D.C.
C_{sense_UL}	C_{sense} pin allowed voltage range		-0.6		58	V
$C_{sense\ gain}$	C_{sense} gain ΔDuty cycle / ΔC_{sense}		0.120		0.350	%D.C. per mV
	V_{C_SENSE} at max current	$V_{Vsense} = V_{reference}$ DC=0%				
$Csense_{Trip}$	Ilimit trip point		0.220		0.440	V
T_{SS}	Soft-start step period not yet tested (to be confirmed)			3		ms
	Soft start steps			16		

Table 13. Voltage booster

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{OH_BST}	BST gate high voltage	I_{source} = 0.5A I_{source} = 20mA	7 9.2			V
V_{OL_BST}	BST gate low voltage	I_{sink} = 0.5A I_{sink} = 20mA			1.75V 0.080	V

4.4.1 Digital to analog converter

Table 14. Digital to analog converter

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
	Dynamic range at -60dBFS	At output of analog filter -60dBFS input 1KHz sine tone	80	90		dB
	Noise floor	At output of analog filter after > 25mS of –97dBFS input 20-20k Hz flat			20	µV
	THD+N at maximum useful input level	Input=-1.5dBFS The DAC output is limited to prevent operation in regions of degraded DAC performance. This spec represents the performance at this maximum practical value			-60	dB
	Silent Mute	Must engage after 25mS of <-96dbFS input signal	20		30	ms
	Differential output voltage	Magnitude of –1.5dBFS sine, 1 KHz	-10%	2.1	+10%	Vrms
	Output resistance		1.8K	2.5K	2.8K	Ohms

4.4.2 I/O pin characteristics

Table 15. I/O pin characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
$I_{SCL/CLIP\_L}$	SCL/CLIP_L pin leakage current		-15		15	µA
$I_{SCL/CLIP\_L}$	SCL/CLIP_L pin sink	$V_{SCL/CLIP\_L}$ <375mV	1			mA
	V_{OH}, digital output pins					
	V_{OL} digital output pins					
	V_{INL}				1.5	V
	V_{INH}		2.3			V
	ADDR0 ADDR1 threshold low				1	
	ADDR0 ADDR1 threshold high		4			

4.4.3 Op. amp. cells

Table 16. Op. amp. cells

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Int_OLGain	Open loop voltage gain	Guaranteed by design	80			dB
PSRR	V_{SP} power supply rejection	PSRR = 20*log10(Vsp/= F < 10KHz V_{SP} ripple=1Vrms Guaranteed by design	-50			dB
Int_Voff	Input offset voltage	Guaranteed by design	-3		3	mV
Int_ibias	Input bias current	Guaranteed by design			500	nA

4.4.4 Shunt

Table 17. Shunt

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
I_{source}	Source current		70	100	130	µA
I_{sink}	Sink current		70	100	130	µA
V_{sd}	Shunt drive current activation Vs. Mute pin voltage (the shunt current is sourced when Vmute is lower than the threshold).		0.8		1.2	V
V_{sdh}	Shunt drive current activation hysteresis		80		140	mV

4.4.5 Application information

These are required parameters of the overall operation of the Cortina IC in its application circuit and will form the overall functional testing for Cortina

Table 18. Analog operating characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
	THD+Noise	1W, 100Hz, V_{SP}=14.4 Rl=2 ohm Only modulator (1)			0.5	%
		4W V_{CC} = 14V and V_{CC} = 42V F_R =1 00Hz (1)			0.3	%
		50W F_R=1kHz V_{CC} = 42V			0.4	%
	Output noise	V_{SP}=14.4V (1)			400	µVrms
	Output offset	V_{CC} = 14.4V V_{CC} = 42V	-100 -200	0 0	100 200	mV
	Output offset	Offset modulator only (V_{CC} =14.4V)	-70	0	70	mV

1. Note: the measure is affected by the testing board noise.

5 I²C and mode control

The Mode1 and Mode0 pins are used to enable TDA7572. These perform the function of bringing the IC out of standby (typically handled by a single standby pin on most audio IC's) as well as determining if the I²C bus is active or if power-up Diagnostics shall automatically occurs.

The Auto-mute Voltage pin is used to provide an under-voltage-lockout for the IC. Using a resistor divider between V2P5 and SVR a series of comparator prevent the IC from power-up further until sufficient voltage is present at VSP and SVR(equal to GND in the split supply case. Once this voltage requirement is met, the chip is forced into mute (a special, direct form of mute that does not use or act upon the MUTE pin) under a second, higher voltage threshold is met. At this point the IC performs its normal power-up, controlled by the state of the MODE pins and the various configuration pins. Refer to the under-voltage lockout (UVLO) section of the documentation for details on these thresholds.

The Auto-mute Voltage pin is also used to provide an over-voltage shutdown based on absolute voltage of VSP-VSM.

Table 19. Power-up mode control

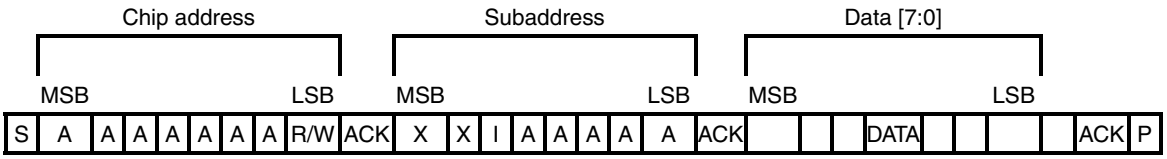
Mode1	Mode0	State/function
0	0	Standby, or “Off”
0	1	NO I²C BUS mode TDA7572 enabled Configuration defaults read from pin I²C disabled Power-Up-Diagnostics disabled
1	1	I²C BUS mode TDA7572 enabled I²C enabled Power-Up-Diagnostics disabled TDA7572 enabled Configuration defaults read from pins I²C disabled Power-Up-Diagnostics enabled
1	0	DIAGNOSTIC mode TDA7572 enabled Configuration defaults read from pins I²C disabled Power-Up-Diagnostics enabled

When I²C bus is active, determined by the Mode0 and Mode1 pins, any operating mode of the IC may be modified and diagnostics may be controlled and results read back.

The protocol used for the bus is the following and comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read / write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Table 20. Addresses



S = Start

R/W = "0" -> Receive-Mode (Chip could be programmed by µP)

"1" -> Transmission-Mode (Data could be received by µP)

I = Auto increment - when 1, the address is automatically increased for each byte transferred

X: not used

ACK = Acknowledge

P = Stop

MAX CLOCK SPEED 500kbits/s

The I²C address is user determined by pins ADDR1 and ADDR0. See table below:

Table 21. I²C chip address

MSB							LSB
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
0	1	0	0	0	ADDR1	ADDR0	X

Write procedure:

Two possible write procedures are possible:

1. without increment: the I bit is set to 0 and the register is addressed by the subaddress. Only this register is written by the data following the subaddress byte.
2. with increment: the I bit is set to 1 and the first register read is the one addressed by subaddress. Are written the register from this address up to stop bit or the reaching of last register.

Example of write instruction with increment:

	Device Address	R/$\overline{W}$		Register Address		DATA 1				DATA 2				DATA n				
S	0011000	0	A	ADDR	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	A	P

Read Procedure:

Two possible read procedures are possible:

1. without increment: the I bit is set to 0 and the register is addressed by the subaddress sent in the previous write procedure. Only this register is written by the data following the address.
2. with increment: the I bit is set to 1 and the first register read is the one addressed by subaddress sent in the previous write procedure. Are written the register from this address up to stop bit or the reaching of last register.

Example of read instruction with increment and previous addressing by write instruction and restart bit (Sr)

	Device Address	**R/$\overline{W}$**		**Register Address**			**Device Address**	**R/$\overline{W}$**		**DATA 1**				**DATA 2**				**DATA n**				
S	0011000	0	A	ADDR	A	Sr	0011000	1	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	NA	P

In the following tables are reported the meaning of each I²C bus present in the device.

5.1 Input control register

Subaddress: XXI00001.

Table 22. Input control register

MSB							LSB	Function
D_7 R/W	D_6 R/W	D_5 R/W	D_4 R/W	D_3 R/W	D_2 R/W	D_1 R/W	D_0 R/W	
1	1	1	1	0	0	0	1	**Power-up default, I²C enabled**
AttackSel (pin)=1 → [11]		AttackSel (pin)=1 → [11]		CompEnable (pin)=1 → [01]		Read from PLL/Gain pin	0	**Power-up default I²C disabled**
AttackSel (pin)=0 → [10]		AttackSel (pin)=0 → [10]		CompEnable (pin)=0 → [00]				
								Mute 1 Mute 0 Play
								INLEVEL0 0 Low Gain 1 High Gain
								Gain table 0 0 Compressor disabled 0 1 THD=0.02; Nb. step=1 1 0 THD=3.0; Nb. step=2 1 0 THD=0.02; Nb. step=1 1 0 THD=3.0; Nb. step=2 1 1 THD=5.0; Nb. step=3 Not used
								Release (400kHz clock) 0 0 20.48ms 0 1 40.96ms 1 0 81.92ms 1 1 163.4ms
								Attack (400kHz clock) 0 0 160µs 0 1 320µs 1 0 640µs 1 1 1.28ms

5.2 Faults 1 register

Subaddress: XXI 00010.

Table 23. Faults 1 register

MSB							LSB	Function
D_7 R/W1TC	D_6 R/W1TC	D_5 R/W1TC	D_4 R/W	D_3 R/W1TC	D_2 R/W1TC	D_1 R/W1TC	D_0 R/W1TC	
			0	0	0	0	0	**Power-up default**
							0 1	**GNDshort** Short to ground detected
						0 1		**V_{CC}short** Short to a “Vcc” detected
					0 1			**Open/offset** Open load detected during
				0 1				**LOADshort** Short across the load detected
			0 1					**DiagnENB** Diagnostic disabled or finished To run the Diagnostic/diagnostic in progress
								UVLO flag UVLO event
								NOT USED
								NOT USED

5.3 Faults 2 register

Subaddress: XXI 00011.

Table 24. Faults 2 register

MSB							LSB	Function
D_7	D_6	D_5 R/W1TC	D_4 R/W1TC	D_3 R/W1TC	D_2 R/W1TC	D_1 R/W1TC	D_0 R/W1TC	
		0	0	0	0	0	0	**Power-up default**
							0 1	**Clip** Clipping of modulator and/or preamplifier
						0 1		**Offset** Offset detected
					0 1			**IsenTrip** Power supply current threshold trespass
				0 1				**IoutTrip** Output stage current limiting has been enabled
			0 1					**ExtTwarn** External thermal warning threshold trespassed
		0 1						**TJwarn** Internal thermal warning threshold trespassed
								NOT USED
								NOT USED

5.4 Control register

Subaddress: XXI 00100.

Table 25. Control register

MSB							LSB	Function
D_7 R/W	D_6 R/W	D_5 R/W	D_4 R/W	D_3 R/W	D_2 R/W	D_1 R/W	D_0 R/W	
0	0	0	0	1	0	1	0	**Power-up default I²C enabled**
0	0	0	0	1	SDA/SCR_ENB	1	0	**Power-up Default I²C disabled**
							0 1	**Mute speed** Slow Mute Fast Mute
						0 1		**OffsetENB** Enable the offset detection
					0 1			**PassFET Control ENB** Enable the SCR intervention
				0 1				**BOOST** Enable the step-up
			0 1					**L/R** Read left channel from I²S Read right channel from I²S
		0 1						**Fratio1** Fs = 96 kHz Fs= 192 kHz
	0 1							**Fratio0** Bass range digital input Fs= 38 to 48 kHz Full band digital input (Fs=96 or 192 kHz selectable by Fratio1)
0 1								**DACEnb** Enable DAC operation

5.5 Modulator register

Subaddress: XXI 00101.

Table 26. Modulator register

MSB							LSB	Function
D_7 R/W	D_6 R/W	D_5 R/W	D_4 R/W	D_3 R/W	D_2 R/W	D_1 R/W	D_0 R/W	
0	1	1	0	0	1		0	**Power-up default I²C disabled**
0	1	0	0	0	SCL/InLevel1 pin		1	**Power-up default I²C enabled**
							0 1	**SHUNT** Turn-on shunt
								NOT USED
					0 1			**INLEVEL1** High level couple
			0 1					**DAC synchronization** Synchronize the modulator with the DAC
			0 1					**SVR** Turn On the charge of SVR
		0 1						**Tristate** Tristate modulator
0 0 1 1	0 1 0 1							**PWMClock** 55kHz 110kHz 220kHz 110kHz

5.6 Testing register

Subaddress: XXI 00110.

Table 27. Testing register

MSB							LSB	Function
D_7 R/W	D_6 R/W	D_5 R/W	D_4 R/W	D_3 R/W	D_2 R/W	D_1 R/W	D_0 R/W	
				0	0	0	0	**Power-up default**
							0 1	**Or ZC** (nIN xnor pIN) or (nOUT xnor pOUT) are put on the clipping output
						0 1		**Ramp** Generate a ramp on the compressor gain
					0 1			**TestDriving** Turn off limitation of driving current for the external MOS
				0 1				**Fast** All time constant used in the logic block are devided by 100
								Not used
								Not used

6 Input stage and gain compressor

6.1 Input stage

The input stage accepts differential analog audio and provides a single ended output that is referenced to SVR, a slowly changing reference signal that is close to $V_{CC/2}$. This signal is present on the pin 6 (SVR). Four input stage gains are selectable, chosen such that input signal levels of either $2V_{RMS}$, $2.6V_{RMS}$, $7V_{RMS}$, or $9.7V_{RMS}$ will provide full scale unclipped output swing of this stage.

The variable gain is realized by a single ended input attenuator (with respect to SVR), such that both differential and common-mode voltages are attenuated, and by, mean of a reconfiguration of the Op-Amp feedback.

These are controlled by two bits, one controlling the input attenuator, and the other controlling the Op-Amp configuration. The bits INLEVEL0 in the InputControl register (register addr 1, bit 1) and INLEVEL1 in the Modulator register (register addr. 5, bit 2) determine the gain selection. The default value of INLEVEL0 and INLEVEL1 bits are determined by the voltage levels at power-up on pins PLL/INLEVEL0 (pin 63) pin and SCL/INLEVEL1 (pin 62) respectively allowing gain selection without the requirement of an I^2C bus. INLEVEL0 controls the input attenuator, and INLEVEL1 controls the configuration of the feedback around the op. amp.

INP - pin 12 : positive input

INM - pin 13 : negative input

AOUT - pin 14 : output

SCL/INLEVEL1 - pin62 : gain selection bit 1

PLL/INLEVEL0 - pin63 : gain selection bit 0

This stage is powered from ±2.5Volts, centered around SVR. Output swing is nominally ±2 volts. The input common mode range is a function of the gain setting, the electrical parameters section must be consulted for details. It is expected that the inputs will be ac coupled, and because of this consideration must be given to the rate of change of SVR, as rapid changes to SVR could cause the inputs of this amplifier to run out of common mode range. i.e. the input decoupling capacitors can not charge fast enough to keep up with SVR

6.2 Gain compressor

A gain compressor is integrated in the front end of this stage, which provides up to 16dB of differential attenuation in approximately 0.5dB steps, varying somewhat depending on gain configuration. Compressor aggressiveness is programmable by the I^2C data/AttackSel pin (providing a choice from two attack-time/decay-time pairs) in non-I^2C bus mode, or by I^2C bus with 2 bits each for attack and decay and 2 bits for the distortion-to-attenuation table. These are bits ATTACK[1:0], DECAY[1:0], and TABLE[1:0] in the InputControl register. The ADDR1/CompEnable pin is used in non-I^2C mode to enable or disable gain compression entirely.

The gain compressor operates by monitoring the estimated in THD due to clipping, over-modulation or over-current and commanding a change in the input attenuation based on the THD estimate. The input attenuator has 32 discrete steps. THD is estimated by measuring the time period between zero crossings where there is no clipping and the time when there

is clipping during that period. The THD estimate is calculated from the ratio between these times. Clipping means are any of the following conditions occurred: maximum modulation reached, output current limiting active, or voltage clipping at the AOUT pin. These are used to estimate THD, which is then mapped to a desired number of discrete steps of gain reduction. Attenuation is then changed at the next zero crossing of the signal at the Input Stage block

The attack time sets the minimum time allowed between gain reductions. At low frequency signals, where the time between zero crossings is greater than the attack time, the attack rate is dictated by the signal frequency, rather than this setting. Similarly, the decay time sets the minimum time allowed between gain increases, with the same caveats about rate dictated by the signal frequency.

The major tuning control here is the distortion-to-attenuation lookup table. It will determine how aggressively to operate and thus the relative amount of audible artifact. Decay time adjustment can be varied for audible effect and to mange average power.

Following are reported the correspondence between I^2C bus registers and coefficients for Attack and decay time. The first table reports the one for compressor setting:

6.2.1 Setting in I^2C bus mode

GainTable[1:0]: Selects the distortion versus gain step size table to be used, including the ability to disable the gain compressor.

Table 28. Distortion versus gain step size

GainTable [1:0]	Pseudo THD,% / T2/T1 ratio	Number of gain steps
00	Gain compressor disabled	
01	0.02 3.0	1 2
10	0.02 3.0 5.0	1 2 3
11	0.02 3.0 5.0 15.0	1 2 3 4

RELEASE[1:0]: Sets the maximum release rate of the gain compressor according to the table below:

Table 29. Sets the maximum release rate of the gain compressor

Release [1:0]	Clock counts	Nominal time at 400KHz clock
00	2^{13}	20.48ms
01	2^{14}	40.96ms
10	2^{15}	81.92ms
11	2^{16}	163.4ms

ATTACK[1:0]: Sets the maximum Attack rate of the gain compressor according to the table below:

Table 30. Sets the maximum attack rate of the gain compressor

Attack [1:0]	Clock counts	Nominal time at 400KHz clock
00	2^6	160µs
01	2^7	320µs
10	2^8	640µs
11	2^9	1.28ms

Setting in NOI^{2}CBUS mode:

I^{2}CDATA/AttackSel - pin 51 -> Attack/release rate selection

ADDR1/CompEnable - pin 54 -> Gain compression effort selection

Table 31. Attack/release rate and gain compression effort selection

INPUT PIN/VALUE	DGND	VDIG
Pin 51	Attack[1:0] = “10” Release[1:0] = “10”	Attack[1:0] = “11” Release[1:0] = “11”
Pin 54	GainTable[1:0]=”00”	GainTable[1:0]=”01”

6.2.2 Soft-mute function, without pre-limiter

Well-behaved over-modulation protection and current-limiting allow this IC to not require a pre-limiter before the modulator. This allows the amplifier to always take advantage of the available supply voltage. A limited output voltage can be done in a crude manner by using AOUT's max output swing, and counting on its clipping signal to drive the compressor.

A soft mute/unmute is incorporated at AOUT. It works by slowly muxing AOUT from the input signal to SVR. In this way, dc offsets occurring in any upstream stages are kept inaudible. The mux slew time is determined by the voltage slew rate at the MUTE_L pin (pin 10), which is asserted low. Mute can by driven either be by external means, or controlled by I2C command.

The MUTE bit, present in the input control register (D0, InputControl register), controls muting by discharging or charging the MUTE_L pin. The default value for this bit for NOI2C mode is 0 that lead to a charging of mute cap. Abrupt muting is available by use of the MuteSpeed bit. When MuteSpeed is asserted, MUTE_L is rapidly charged and discharged by a small resistance (approximately 500 ohms). In the pictures below are reported the two application circuits and the internal circuitry of mute correspondent to.

Figure 3. Mute by external command

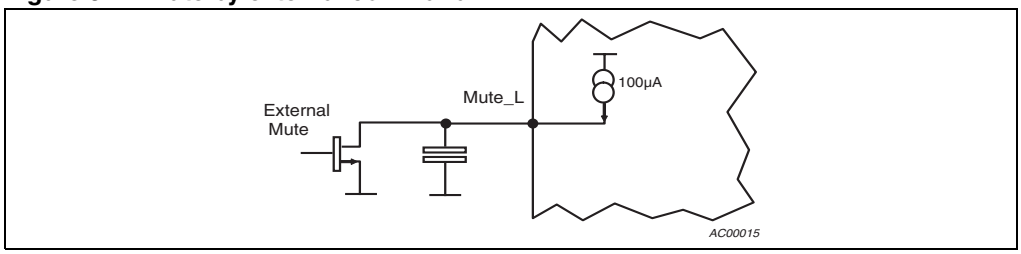
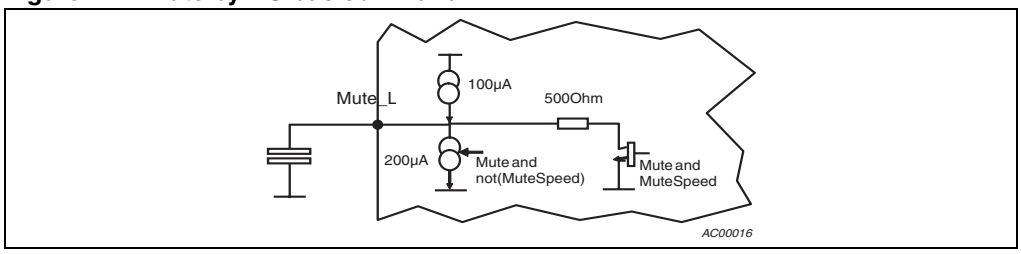


Figure 4. Mute by I²C bus command

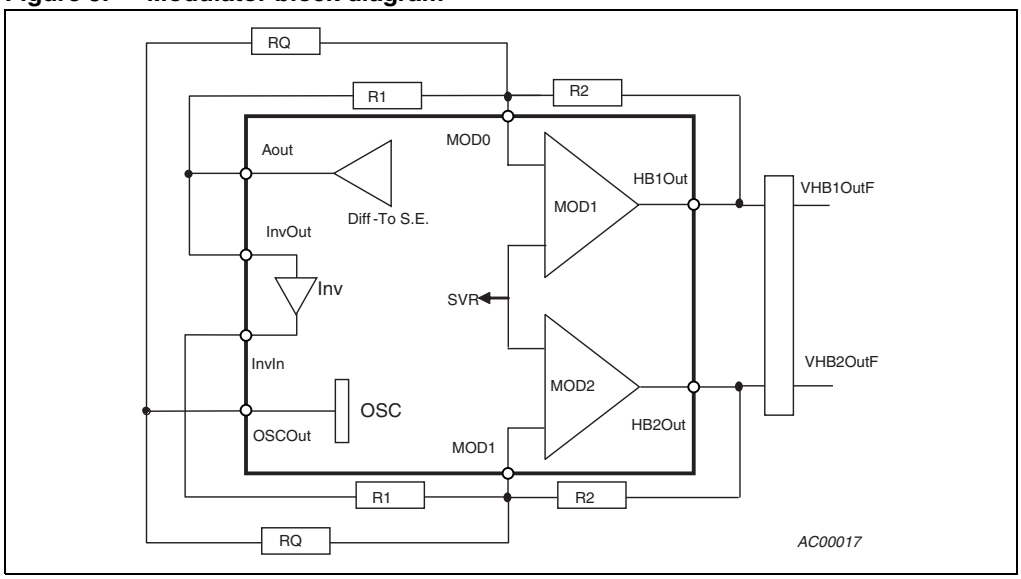


Note: when the modulator is set in TRISTATE the mute pin is fast-discharged by the fast-mute internal circuitry. When the modulator is take back out of TRISTATE the preamplifier is put in play back by a fast un-mute transient.

7 Modulator

The modulator PWM is the main function of device. Two modulators are provided which are operated independently but configured for bridged mono operations. They are synchronized by virtue of the common clock that drives them and operate as a three-state modulator (phase shifting PWM modulation type) when the audio is inverted going to one modulator. This inversion is accommodated by a dedicated inverter block present between the InvIn and InvOut pin.

Figure 5. Modulator block diagram



The above scheme reports the application circuits and internal block involved in the PWM modulator. The analog signal is differential to single ended converted by the amplifier. The signal obtained is inserted as current in the virtual ground of modulator MOD0. The conversion is obtained trough R1 resistor. The same signal, output of AOUT, is inverted and inserted in the virtual ground MOD1 through the resistor R1.

In order to obtain a PWM signal a square wave is inserted in both MOD0 and MOD1 through the RQ resistor. The Gain of Modulator is equal to the ratio of R1/R2. In Order to choose the value of RQ has to take into account the stability of modulator, guarantee if the following relation is respected:

Equation 1 $$\frac{VP2.5}{RQ} > \frac{VAOUTmax}{R1} + \frac{VSP - VSVR}{R2}$$

Clocked PWM modulators using an integrated T-network double integrator are implemented. The end user has the ability to trade distortion for EMI by switching faster or slower, controlled by PWMClock[1:0] in the modulator register.

Table 32. PWMClock table

PWMClock [1:0]	Ratio	Nominal frequency
00	$F_{NOM}/2$	55KHz
01	F_{NOM}	110KHz
10	$F_{NOM}*2$	220KHz
11	F_{NOM}	110KHz

Pulse injection is being used with the clocked PWM scheme to prevent missing pulses from an over-modulation condition. The minimum pulse width is dynamically determined by looking at the delay from the comparator output to the actual switching of the FET stage. This delay is used to extend any pulses from the modulator that would otherwise be too short. Circuitry is provided to keep the integrator hovering near the level at which limiting first occurred, which prevents transients once we leave the over modulation condition. This is done by summing in a current that is proportional to the amount of time that the pulse is extended.

Since only three- state modulation is supported, it may prove necessary to slightly delay the clock going to one modulator to prevent the noise from the switching of one modulator affecting the second modulator when there is no audio input. This can be done with a small RC on the clock feeding one modulator. The same result could be obtained adding the RC on the feedback feeding one modulator.

The reference voltage of the modulator changes from SVR at it's input, to Vcc/2 at its output. This allows output signal to be centered between the supply rails, increasing unclipped output voltage swing by preventing asymmetric clipping. This is accomplished using the LVLSFT pin, as described in the previous paragraph. It has been pointed out that there is potential for abrupt transients at the output stage, as this scheme will attempt to have the outputs track VCC/2, while it may be better for avoiding pops to have them rise slowly with SVR. The end user needs to make this decision by making or not the connection between HVCC and LVLSFT pin. Will not be present pop noise in a system with perfect symmetry between the two modulators branch. Pop noise will rise with increasing of asymmetry.

7.1 FET drive

Gate drive circuits are provided to drive complementary external FETS. An internal regulator to supply the low side gate drivers provides a voltage 10V above VSM. This fully enhances the FETs without exceeding their V_{GS} limits. A separate regulator 10V below V_{SP} is used for the high side gate drivers.

Shoot-through is prevented by sensing V_{GS} of each FET with a dedicated sense line (GateSensing), and blocking the opposite FET turn-on if the active FET in a ½ bridge has a $|V_{GS}| > |V_{Threshold}|$. This allows discrete components to be used to adjust gate charging without concern over shoot-through.

The drivers are capable to provide high current for a short time (about 5µs) and a lower current after this time(~150mA). This is done to give enough charge current at the commutation and avoid short-cut overcurrent.

The V_{DS} of the enhanced FET of each ½ bridge is used monitor current and detect overcurrent condition. The sensed V_{DS} signal is blanked such that sensing is only active when the FET is enhanced and any turn on transients have settled. There are two type of overcurrent intervention: current limitation, cycle-by-cycle limitation. The current limitation

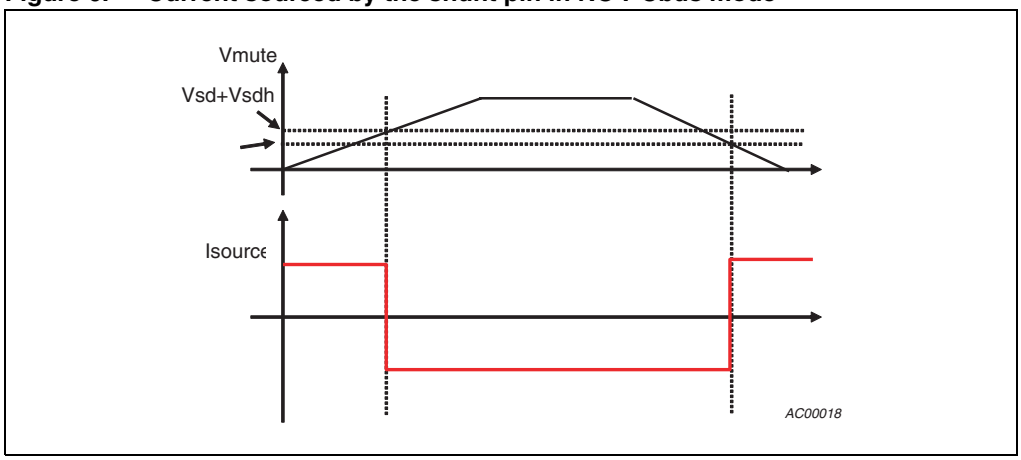
consists in a clipping of current when the first threshold for V_{DS} is trespassed. It is obtained by sink or source current to the virtual ground of modulator integrator. The cycle-by-cycle limitation is a strong limitation. If the second V_{DS} threshold is trespassed for more than about 2µs the half bridge is tri-stated. If this condition persists for more then four PWM periods the modulator is definitely tri-stated. It is possible setting the threshold V_{DS} voltage for the current limiting by the pin IlimitThreshold: the first threshold is the value voltage value of this pin (referred to VN2.5), the second one is the same value multiply by the factor 1.5.

7.2 ANTI-POP shunt driver

The device is provided by a driver able to control an anti-pop shunt MOS which is connectable in series or in parallel to the load. During the mute-to-play or play-to-mute transition an external MOS is able to disconnect (MOS in series) or short (MOS in parallel) the speaker in order to reduce the audible pop noise.

The shunt driver is able to source or sink a predefined current (see *Table 17*). The following diagram reports the temporal behave of current at the shunt pin respect to the voltage on the mute pin in NOI^{2}CBUS mode.

Figure 6. Current sourced by the shunt pin in NO I^{2}Cbus mode



In I^{2}Cbus mode it is possible to change the driver current direction only by change the bit D0 of byte 5. When the bit is set to 1 the current is sourced. By default the current is sourced.

8 DAC

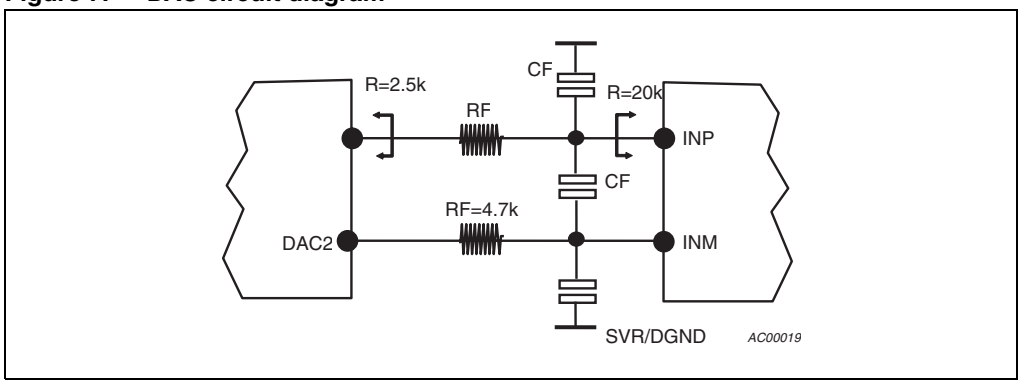
A one channel DAC is provided. A balance between die area and functionality has been made - the interpolator function required for full bandwidth operation has been off-loaded to an external DSP. This allows Bass-only operation of the DAC without any processing assistance, while full bandwidth audio requires external interpolation assistance.

The DAC has a differential output:

- positive output DAC1(32)
- negative output DAC2(31)

On these pins are present a four level squared wave, composed by the differences of two PWM wave have one an amplitude 16 times lower than the other. The output voltage on DAC1 and DAC2 is compatible to the digital supply VDIG.

Figure 7. DAC circuit diagram



where is filtered by means of capacitors and put in the AOUT Differential to single-ended input, as reported in the picture above. The maximum signal present output of converter is 1.4 Vrms. The setting to use for the Diff-to-SE converter is Gain= -3dB (INLEVEL1=0,INLEVEL0=0).

Communication is through a standard I^2S port. I^2C is available too.

Acting on the I^2C Control registers it is possible turn-on the DAC (DACEnb) and choose the configuration (Fratio(1:0)). With Fratio = "00"/"01" the configuration is for bass only. The Input sample frequency is 48kHz (Fs). In case of Fratio = "10" the configuration is for full band. The input sample rate for this case is 96kHz (Fs) and the first x2 interpolator has to be implemented off-line in the DSP. A well checked structure to realize could be the following:

Oversampling		Increasing word rate from Fs to 2Fs.
Filter	Type	Remez filter, half band
	Taps, bit	57, 12
	Attenuation	50db attenuation out of 0.55Fs
	Coefficients	It is an Half-Band filter then we have only 15 coefficients (see following)

Coefficients: -11,11,-16,22,-30,40,-53,69,-91,122,-168,247,-426,1300,2047,1300,….

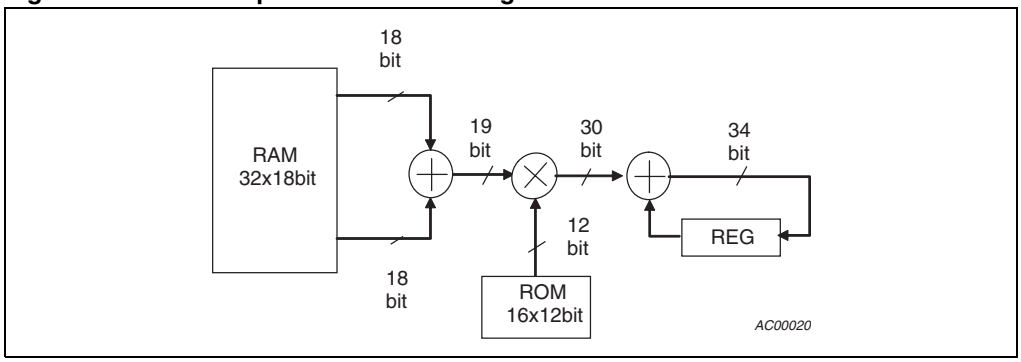
In case of Fratio = "11" the configuration is still for full band. The input sample rate for this case is 192kHz (Fs) and the first x4 interpolator has to be implemented off-line in the DSP. For the first x2 interpolator could be used the precedent, for the second one should be used the following:

Oversampling		Increasing word rate from 2Fs to 4Fs.
Filter	Type	Remez filter, half band
	Taps, bit	7, 12
	Attenuation	50db attenuation out of 0.77*(2Fs)
	Coefficients	It is an Half-Band filter then we have only 3 coefficients (see following)

Coefficients: -190, 1199,2047,…

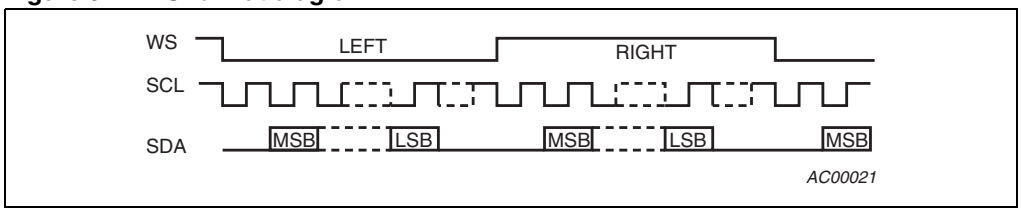
To implement the first interpolator are necessary 28 memory access, 14 sum and14 MAC (multiply with accumulation) at rate Fs. For the second one are, instead, enough 4 memory access, 2 sum and 2 MAC at rate 2Fs. In the following schematic is reported the structure for the two interpolator eventually to implement in the DSP.

Figure 8. Two interpolator structure diagram



The I^2S format is used to transfer audio samples:

Figure 9. I^2S format diagram



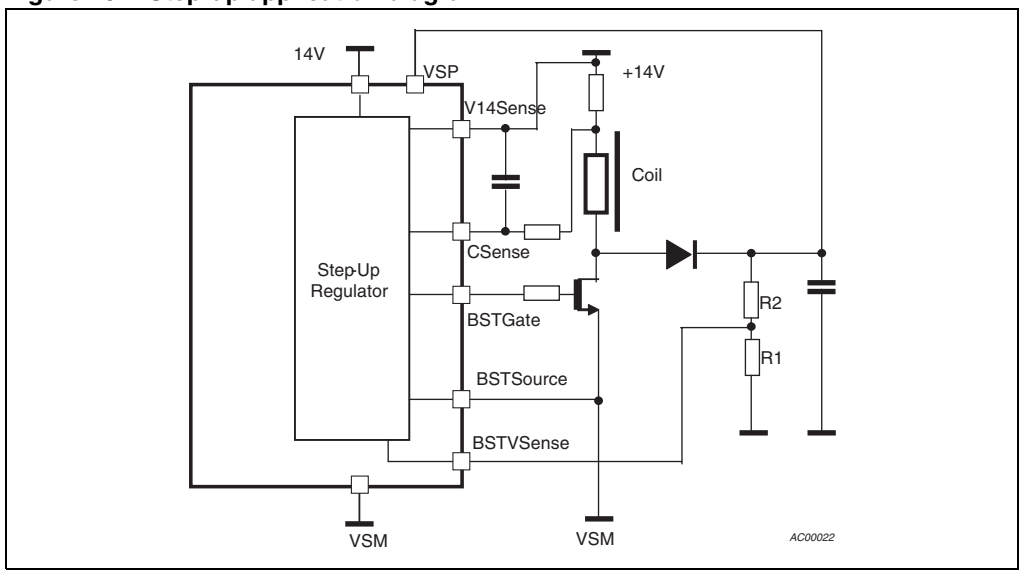
Where the WS is a clock at frequency Fs(48,96,192kHz) and discern which channel is transferred, where the SCL is the interface clock at 64*Fs(3.07, 6.14, 12.29MHz). The SDA are the bit transferred, 32 for each channel. Only the first 18 bits are taken into account and only one channel. The Control register bit L/R selects the channel amplified.

The internal clock used to clock the DAC logic is obtained from the PLL that lock to the I2S clock present on pin SCL. In order to work the PLL needs a RC series network connected to pin PLL/INLEVEL0 (pin 44). Optimal value are C=100nF, R=33Ohm with in parallel an 1.8pF capacitance

9 Step-up

A current boost controller is provided to allow high power operation in the 14V automotive environment. This is a clocked PWM, current mode control block that drives an external NFET. Following is present the application circuits.

Figure 10. Step-up application diagram



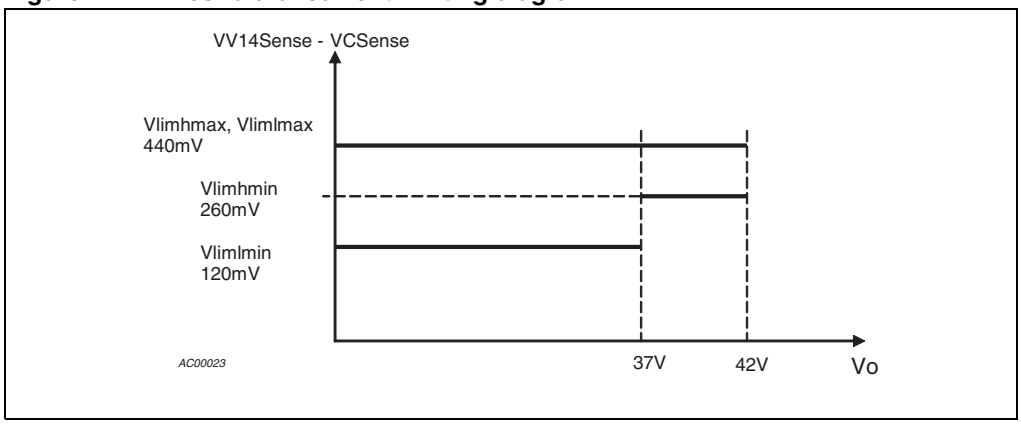
In the Step-up implemented is present a current control loop and a voltage one to fix the output voltage. On the pin BSTVSense is reported the voltage VSP except for the gain of Step-up, here imposed by the ratio R1 and R2. To improve stability, response time and inductor requirements, an inner current control loop has been implemented. The inductor parasitic resistance will be an adequate current sensor, and it is expected that with an RC could be cancelled the zero of the boost inductor. Instead of use the parasitic resistor of inductor a series sensing resistor could be used. The current sensing is take out by the pins V14Sense and Csense.

To avoid destructive startup currents, soft startup is provided which functions by increasing the allowed current limit using 4 steps roughly 4ms apart.

An overcurrent condition is declared if there is an extended period of high current.

Excessive current is detected (by monitoring the voltage across Csense and V14Sense pins) for a period exceeding 20ms, which are considered to be caused by a fault condition, are detected as Csense exceeding a voltage threshold and are handled by forcing a restart of the soft start sequence when over-current is declared. Following are reported the threshold of current limiting.

Figure 11. Threshold of current limiting diagram



The I^2C bus register that is set for default to "habilitation" enables the step up. In case of 14V operation or split supply the step-up and no i2c bus mode the step-up is disabled by connects the BSTVSense pin to a reference of at least five volts over VSM.

During the testing phase the digital test mode is entered by put Csense pin at least 3V under 14V pin.

10 Diagnostics

Diagnostics are grouped into two categories, those performed only during standby, and those available during amplifier operation.

When Mode[1:0] indicate the I^2C is active, the RunDiag bit must be set (by an I^2C write to the Faults1 register) to initiate diagnostics.

When Mode[1:0]indicate the I^2C is not active, the state of Mode[1:0] are further decoded to determine if the diagnostics should be run automatically during power-up

Diagnostics performed during power-up (Power Up Diagnostic or PUD, sometimes called "Turn-on-diagnostics") are:

1. Output shorted to ground
2. Output shorted to Vs
3. Shorted transducer
4. Open Transducer

During operation the following conditions are continuously monitored:

1. DC offset across the speaker
2. Die temperature
3. External temperature
4. Output Clipping
5. Output overcurrent
6. Power supply overcurrent

Faults are reported in a simple manner for bus free operation. The open drain WS/Clip_L pin asserts when clipping occurs, and the Address0/Fault_L pin asserts if any there are any other faults. In case of busfree operation the Address0/Fault is the logical OR of all fault conditions. When I^2C bus is present, one can read detailed fault status, as well as control the diagnostics being performed via TDA7572's registers, Address0/Fault_L is used to determine which one has to be the I^2C bus Address0 of this IC or, in case of DAC operation, it is used to assert when clipping occurs. In this case the Address0 of I^2C bus address is automatically set to zero, which implies that only two TDA7572 can be addressed. In any Mode case a clipping output is present.

The detailed procedure implemented to manage these faults follows:

10.1 Faults during operation:

10.1.1 DC offset across the speaker

I^2Cbus: If the module of VHOUTF1 - VHOUTF2 > 3Vfor more then 100ms the Offset bit in register Faults2 is set and the external FET's are tristated. The bit is cleared using the W1TC procedure. Resetting the bit removes the tristate mode and modulator operation is restored

No I^2Cbus: Operation is as above except the fault is also reported by asserting the Address0/Fault_L pin. In order to restart the system is necessary to pass through standby mode.

10.1.2 Die temperature

- I²Cbus: The Twarn bit in register Faults2 bus register is set when the first threshold is exceeded. If the second threshold is exceeded the SCR is enabled (only if the PassFETctrl bit is set to one) which allows the external power switch to latch off, and can only be restarted by removing and reapplying power. Twarn is cleared using the W1TC procedure.
- No I²Cbus: Operates as above, except the non-latched version (real-time version) of the Twarn bit is reported on the Address0/Fault_L pin. The value of PassFETctrl is determined by the SDA/SCR_Enb pin, which is read at powerup.

10.1.3 External temperature

- I²C bus: The ExtTwarn bit is set if the voltage at the NTC pin exceeds the first threshold. If the second threshold is exceeded the SCR is enabled (only if the PassFETctrl register is set to one). ExtTwarn is cleared by the W1TC procedure
- No I²C bus: Operates as above, except the non-latched version (real-time version) of ExtTwarn register is reported on the Address0/Fault pin. The value of PassFETctrl bit is determined by the SDA/SCR_Enb pin, which is read at powerup

10.1.4 Output clipping

- I²C bus: The Clip bit in the Faults2 register is set when the clipping detected. The Clip bit is cleared by the W1TC procedure. Clipping is detected if there is maximum modulation or over current control at the modulator, or if the AOUT pin clips.
- No I²C bus: The instantaneous value of clipping, as defined above, is reported on the SCL/CLIP_L pin. The pin is pulled low during a clipping event (assertion level low).
- DAC Enabled: To handle the case when the DAC is in use and to meet the requirement of a physical clipping signal, the clipping signal is brought out to the Addr0/Fault pin

10.1.5 Output over-current

- I²C bus: The output current is clipped/limited by pulse injection into the modulator when the qualified VDS of the active FET exceeds the first threshold, at the same time the IoutTrip bit is set. If the second threshold is exceeded the current is cycle-by-cycle limited by switching the FET's off after few microsecond. If the cycle-to-cycle limitation is present for more then 4 cycle the SCR is enabled (only if the PassFETctrl register is set to one) and the external FET are tristated. In case of the SCR is disabled the external FET are not tristated and the limitation still going. The register is cleared by the W1TC procedure.
- No I²Cbus: In addition to the above, the clipping out pin is engaged by the current limitation. The value of PassFETctrl bit is determined by the SDA/SCR_Enb pin, which is read at powerup

10.1.6 Power supply overcurrent

- I^2Cbus: The bit IsenTrip is set when the voltage between the ISSENP and ISSENM pins exceeds the threshold. Also, the power control SCR is turned on (only if the PassFETctrl register is set to one). IsenTrip is cleared by the W1TC procedure.
- No I^2Cbus: In addition the above, the non-latched version of IsenTrip register is reported on the Address0/Fault_L pin. The value of PassFETctrl bit is determined by the SDA/SCR_Enb pin, which is read at powerup:
- NOTE: The Output current is monitored only when the output signal is in the +/-1.2V (see offset detector specification) range for more then 100ms. When this condition is reached a switch present between ISSENM and ISSENP is switched off. Normally this switch shorts the ISSENM pin to the ISSENP, allowing external filter caps to used to condition the current sense signal.

10.1.7 Fault handling

Table 33. Fault handling

Fault	1st Threshold (Bus mode: I^2C/No I^2C)	2nd Threshold
DC offset	- Latch the offset bit - Tristate the modulator	
	- Latch the offset bit and Fault pin - Tristate the modulator	
Die temperature	- Latch the Twarn bit	The SCR is activated if enabled
	- Latch the Twarn bit - Assert the fault pin	
Output clipping	- Latch the Clip bit - Assert the SCL_CLIP_L (if no DAC) - Assert the Address0 (if DAC)	
	- Latch the Clip bit - Assert SCL_CLIP_L	
Output overcurrent	- Latch the IsenTrip bit - Clip the output current by modulator injection	Cycle-to-cycle Current limiting is activated. If the cycle-by-cycle limitation is present for more then four PWM cycles the SCR is activated if the SCR is enabled and the output FET are tristated. If the SCR is disabled the cycle-by cycle limitation keep going.
	- Latch the IsenTrip bit - Clip the output current by modulator injection	
Power supply overcurrent	- Latch the IoutTrip bit - The SCR is activated if enabled	
	- Latch the IoutTrip bit - Assert the Fault pin - The SCR is activated if enabled	

Note: in legacy mode (no I^2C bus) the Output over-current warning information is not reported on the fault pin, while is present on the clipping detector output pin.

Events that put in tri-state the Modulator:

- Diagnostic on
- Offset detection
- Output over-current second threshold trespassed

Events that enable the Fault Pin without I^2C bus:

- Diagnostic Fault
- Junction thermal warning
- External thermal warning
- Supply current over-threshold
- Offset detection

Events that enable the SCR:

- Over-temperature protection
- Output over-current second threshold trespassed
- Supply current over-threshold

10.1.8 Faults during power-up:

This is a power-up diagnostic useful to detect: load short to ground, load short to supply, short across the transducer, open transducer. The PUD could be performed with and without I^2C bus.

- I^2Cbus: setting the bit 4 of Fault1 register the diagnostic begin. The capacitor TestC is then charged by a Thevenin circuits with R = 155 kOhm and supply equal to 1.75V. The value of capacitor is choose in order to have an audible charge ramp and at the same time in order to have an acceptable charge time. The diagnostic time start when the TestC pin reaches the 98% of full charge. During the diagnostic time of 100 ms a current equal to

$$I = \frac{2.45}{3 \cdot RISet}$$

  The drop across the load produced by this current is continuously monitored. A fault is detected if the drop and/or the absolute value of pin HB1Out and HB2Out are abnormal for the full 100 ms period set when a fault is detected the correspondent bit in the Fault1 register is set and the diagnostic keep running until the fault is present. In case no fault is detected after the 100 ms period the capacitor is discharged and the current on the load is reduced down to zero. When this current is at the 2% of is nominal value the bit 4 of Fault1 register is set to zero. Pulling this register the operator could understand the state of diagnostic. Note that during diagnostic cycle the output FET are in tristate.
- No I^2C bus: The operation of diagnostic is equal to the one with I^2C bus. The only differences are about the habilitation, which is selected by the mode, and the assertion of fault presence, which is done trough the addr0/Fault pin. At the end of diagnostic the Fault pin is for sure low and the external FET start to commute.

These are the thresholds to take into account for short to ground and short to supply

	SGND		X		Normal operation	X		SVCC
Voltage threshold	VSM	VSM+1V		VSM+2V	VSM+5.5V		VSM+8V	VSP

These are instead the thresholds to take into account for the short and open transducers with some example with a predefined current

	SL	X	Normal load	X	OL
Voltage threshold	-	6 mV	20 mV	1	2	-
Itest=14mA	-	0.4Ω	1.43Ω	71Ω	143Ω	-
Itest=140mA	-	0.04Ω	0.14Ω	7.1Ω	14.3Ω	-

11 Oscillator

A common clock is needed to run all switching blocks at one frequency to avoid beating. The internally generated clock is used for the PWM modulators and to run the dc-dc converter. To blur the EMI spectrum, sub-audible frequency dither incorporated.

- When the DITH-sel pin is logic gnd then the internal oscillator operates without dither.
- With a cap there is +-100UA dithering functions
- Putting DITH-sel to VDIG allows an external clock to be accepted from CLKin-out at 4X the selected frequency
- Clock out is referred to VP2.5 and VM2.5, while external clock input is referred to DGND and VDIG
- External CLKin-out is always active. When DITH-sel is different to VDIG on this pin is present a 4X modulator frequency at digital level.

The dither acts to span the intermodulation products present around multiple of switching frequency. Dither the modulator frequency means make it slowly changing around a nominal value. In case of a capacitor is connected to the DITH-sel pin a triangular drop is present across it and the modulator frequency value follows these behave. The maximum value reaches by it is the nominal value plus 10%, while the minimum value is nominal one minus 10%. This pick frequency values are reached when the DITH-sel pin reach the maximum voltage value. The value of capacitor is involved in the ratio of variation of modulator frequency, provided that it acts on triangular wave frequency.

In case of DAC operation the modulator frequency of PWM digital out of this component is lock to the I2S input frequency, which is different from the analog modulator frequency imposed by the described oscillator. No high value intermodulation product are generated by difference of this frequency because the presence of filter between DAC out and Diff-to-SE input. However a multiple frequency of DAC could be imposed to analog modulator by the CLKin-out pin. In this case no dither can be introduced.

12 Under voltage lock out (UVLO)

The UVLO lock at the voltage references value used to run the device. If some of them are not in the rate band the system is put in tristate or in stand-by. The Auto-mute Voltage Setting pin (pin56) voltage is used to define the limits of this voltage references.

List of monitored pin:

1. MODE0 and MODE1 voltage value
2. VSP-VSM voltage difference
3. SVR voltage value
4. VSP-SVR or VSR-VSM voltage difference
5. V14 voltage value

In the UVLO could be defined four blocks:

- VSP - UVLO
- VP2.5/VM2.5 UVLO
- V14 - UVLO
- SVR - UVLO

12.1 VSP-UVLO

This block monitors the VSP-VSM drop and eventually moves the modulator in mute or in tristate. The limits imposed by the VSP-UVLO block are principally three:

1. an adjustable limit on the minimum supply/drop
2. an adjustable limit on the maximum supply/drop
3. an absolute limit on the maximum supply

The adjustable limits are obtained by means of the reference voltage present on the AutomuteVSetting pin, which is fixed by means of a ladder resistor of R1 and R2 between VP2.5 and SVR.

The comparators that sense the voltage drop for the auto mute are provided of hysteresis. An hysteresis is still present for the auto-tristate and expressed in the spec as two different thresholds that are function of reference voltage and slope polarity.

12.2 V14 - UVLO

This block monitors the V14-VSM drop voltage and eventually moves the modulator in mute or in tristate. The V14-UVLO block fixes a limit on the minimum drop.

An hysteresis is present for the auto-tristate and expressed in the spec as two different thresholds that are function of slope polarity. An hysteresis is still present for the auto-mute and expressed in the spec as two different thresholds that are function of auto-tristate threshold and slope polarity.

12.3 SVR - UVLO

This block monitors the SVR-VSM drop voltage and eventually moves the modulator in tristate. The SVR-UVLO block fixes a limit on the minimum drop.

An hysteresis is present for the auto-tristate and expressed in the spec as two different thresholds that are function of slope polarity. An hysteresis is still present for the auto-mute and expressed in the spec as two different thresholds that are function of auto-tristate threshold and slope polarity.

13 Start-up procedures, modulator turn-on after a tristate condition.

13.1 Start-up

Condition to be respected to turn-on the modulator at the start-up:

- Are MODE0 and/or MODE1 pins at voltage higher than 2.3V?
- Is the command “TristateMOD” Set to “1”?
- Is the PLL locked? (Only in case of digital Input)
- Is the Thermal protection FLAG ON?
- Are the VSP-VP2.5 and VM2.5-VSM drop voltage respectively over VAP and VAM?
- Is the VSP-VSM voltage lower than V_U and V_{UC}?
- Is the total VSP-VSM Higher than VPO+?
- Is the SVR pin higher than Vsvr+?
- Is the 14V pin supply higher than V14mute+?

TristateMOD represents an internal signal which is

– in NOI^{2}CBUS MODE set to '1' when the digital supply pin VDIG (50) reaches its steady state value.
– in I^{2}C MODE set to '1' when the digital supply pin VDIG (50) reaches its steady state value and by I^{2}C bus is written '1' on the D4 bit of modulator register.
– in NOI^{2}CDIAGNOSTIC set to '1' when the digital supply pin VDIG (50) reaches its steady state value and the turn-on diagnostic has positive result.

The thermal protection represent an internal signal which is set to '1' at the start-up and eventually set to '0' if

– the internal temperature trespass the second threshold and/or
– the external temperature trespass the second threshold

Once all the listed condition present in the above table are respected the modulator is get out from tri-state after ~500µs.

13.2 Tristate

When the modulator is put in tristate by some diagnostic condition the system retrieve from this condition in two possible mode depending from the supplies configuration

– split supply: The modulator starts to switch ~500µs after all conditions listed in the above table are realized.
– Single-supply: Only in case of single supply, is activated a circuit that inhibit the startup of the SVR capacitor charge (then the modulator enable) if the SVR voltage is higher than 1.5V. If, during the normal activity of the modulator, an event that moves the modulator in tristate is present (due to, as example, an UVLO) the Vsvr gets to discharge until its value is under 1.5V. Ones reached this value the capacitor svr start to charge. The modulator starts to switch ~500µs after all conditions listed in the above table are realized. Purpose of this circuit is to avoid fast turn-off/on of the modulator and increase the pop performance.

14 Applications

14.1 Single supply

Figure 12. Single supply evaluation board schematic.

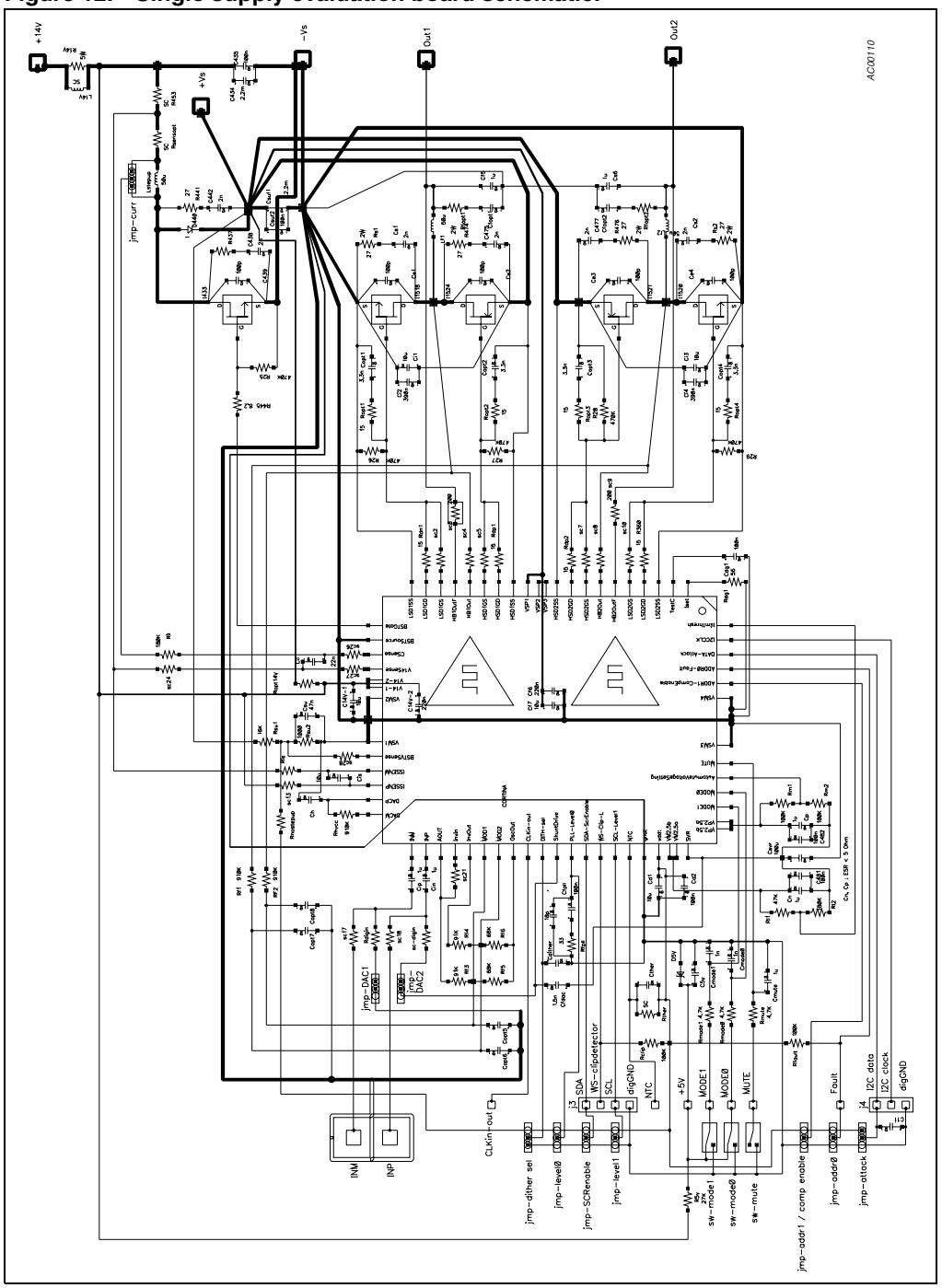
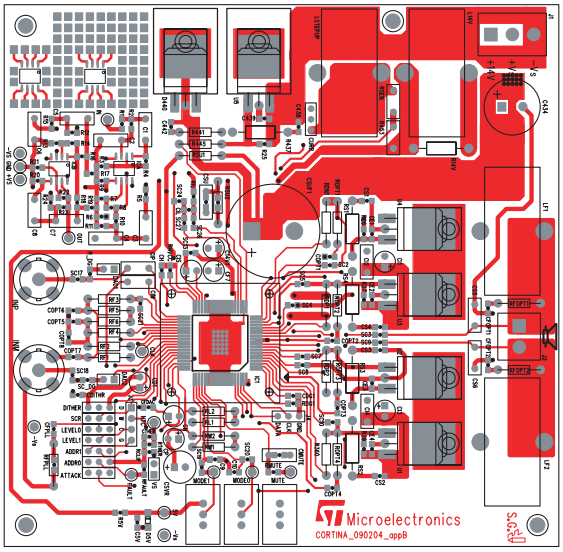
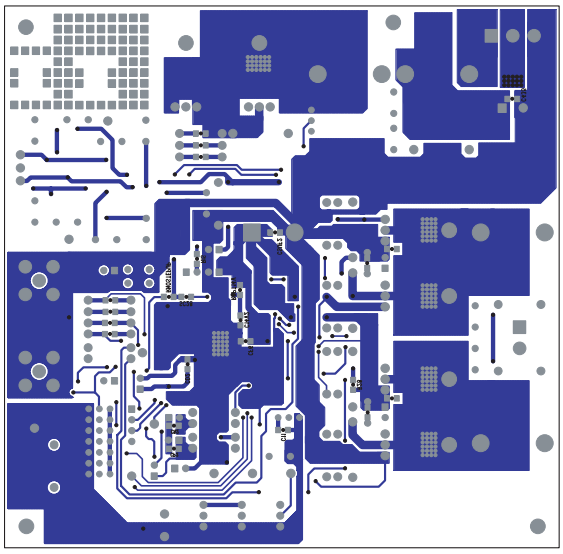


Figure 13. Single supply evaluation PCB



Top layer and component layout



Bottom layer

14.2 Split supply

Figure 14. Split supply evaluation board schematic.

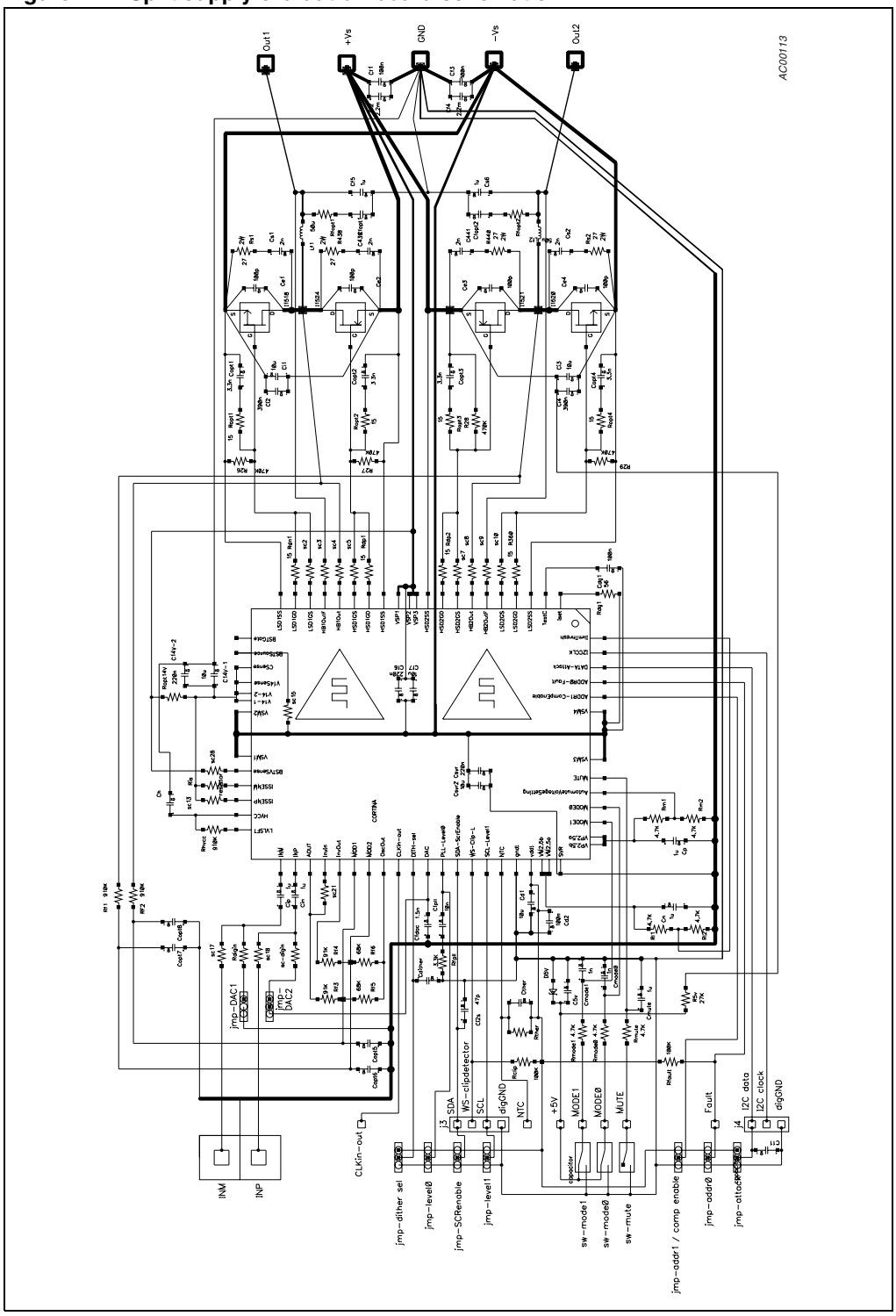
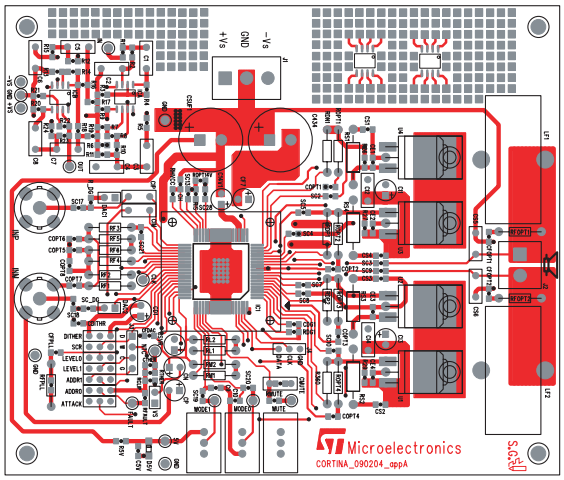
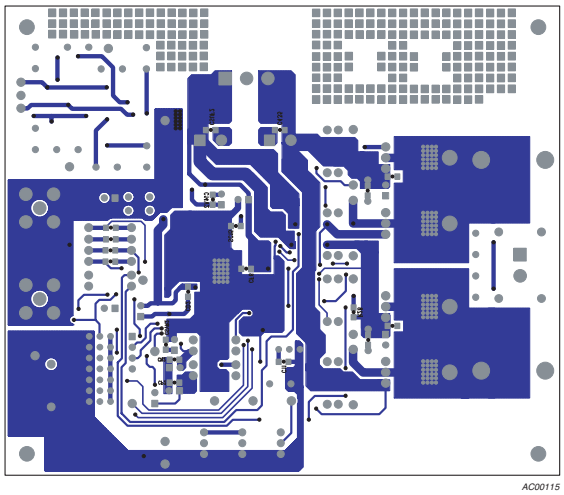


Figure 15. Split supply evaluation PCB



Top layer and component layout



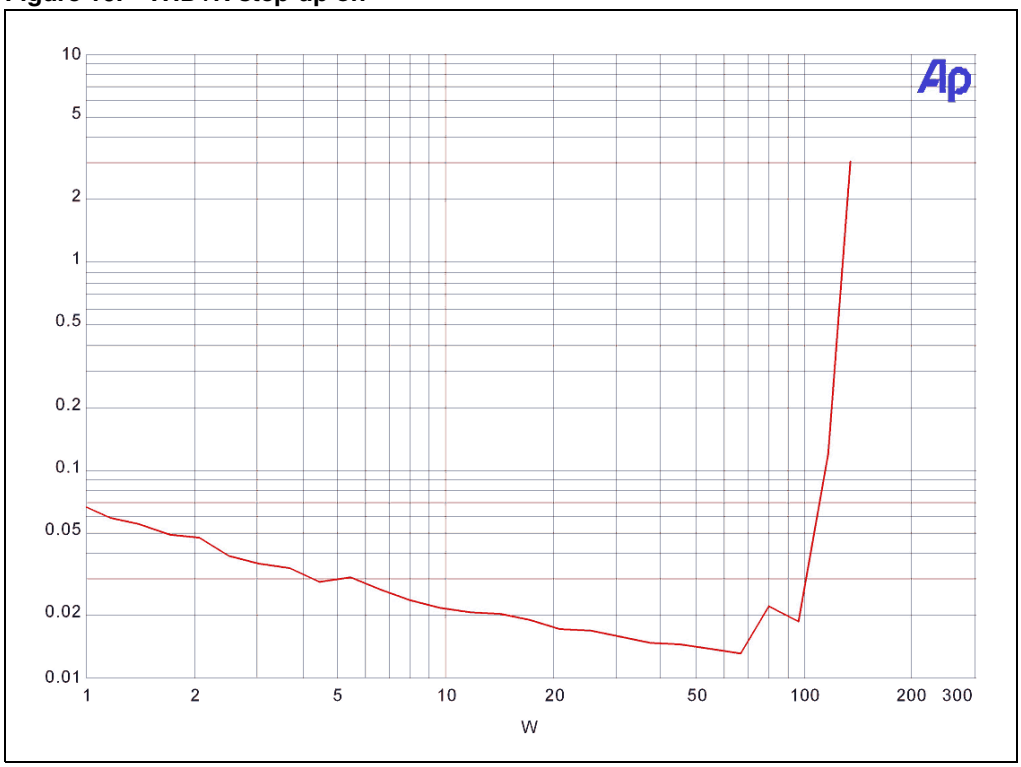
Bottom layer

14.3 THD+N step-up on

The graph below report the THD+N vs. Pout of a TDA7572 board with step-up on and 50Hz input sine wave. Condition and step to made the board working are:

1. connect a voltage supplier to the connector J1: Positive terminal (max 14V) connected to L14V, ground terminal connected to -Vs.
2. connect the differential input signal on INP and INM BNC input or connect the single ended input on the INP BNC and short cut the INM BNC.
3. connect the load of 4Ohm to the connector J2.
4. turn-on the device by means of MODE0 switch.
5. put in play the device by operating on MUTE switch

Figure 16. THD+N step-up on



15 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

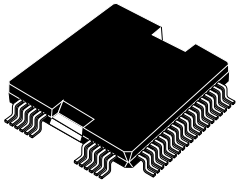
ECOPACK specifications are available at: www.st.com.

Figure 17. HiQUAD-64 mechanical data and package dimensions

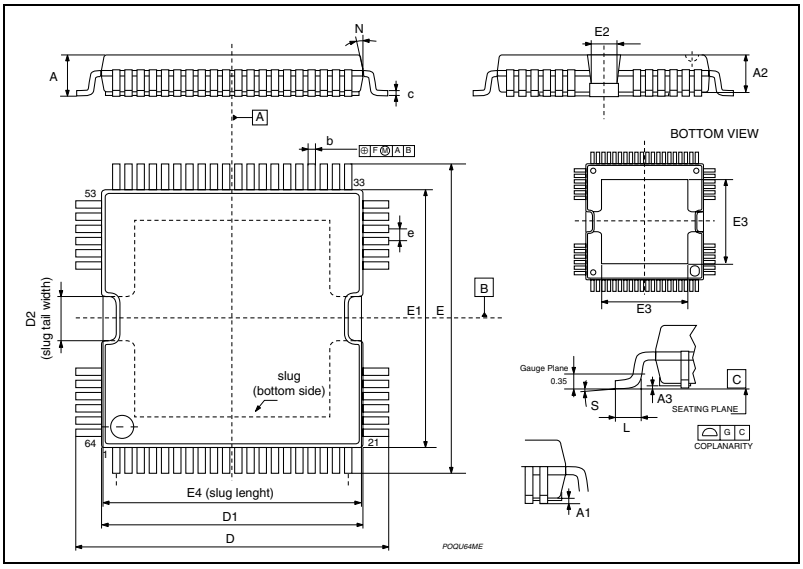
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.15			0.124
A1	0		0.25	0		0.010
A2	2.50		2.90	0.10		0.114
A3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	17.00		17.40	0.669		0.685
D1 (1)	13.90	14.00	14.10	0.547	0.551	0.555
D2	2.65	2.80	2.95	0.104	0.110	0.116
E	17.00		17.40	0.669		0.685
E1 (1)	13.90	14.00	14.10	0.547	0.551	0.555
e		0.65			0.025	
E2	2.35		2.65	0.092		0.104
E3	9.30	9.50	9.70	0.366	0.374	0.382
E4	13.30	13.50	13.70	0.523	0.531	0.539
F		0.10			0.004	
G		0.12			0.005	
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	0°(min.), 7°(max.)					

(1): "D1" and "E1" do not include mold flash or protusions
- Mold flash or protusions shall not exceed 0.15mm(0.006inch) per side

OUTLINE AND MECHANICAL DATA



HiQUAD-64



16 Revision history

Table 34. Document revision history

Date	Revision	Changes
3-Sep-2007	1	Initial release.