FAIRCHILD

SEMICONDUCTOR®

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74LCX162373

Low Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs and 26Ω Series Resistor

General Description

The LCX162373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state.

The LCX162373 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The 26Ω series resistor in the output helps reduce output overshoot and undershoot.

The LCX162373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant inputs and outputs

■ 2.3V–3.6V V_{CC} specifications provided

■ Equivalent 26Ω series resistor outputs

■ 6.2 ns t_{PD} max (V_{CC} = 3.3V), 20 μA I_{CC} max

■ Power down high impedance inputs and outputs

■ Supports live insertion/withdrawal (Note 1)

■ ±12 mA output drive (V_{CC} = 3.0V)

■ Implements patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

■ ESD performance:

　Human body model > 2000V

　Machine model > 200V

■ Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.
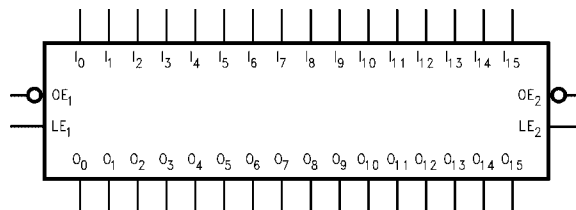
Ordering Code:

Order Number	Package Number	Package Description
74LCX162373GX (Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LCX162373MEA (Note 3)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX162373MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

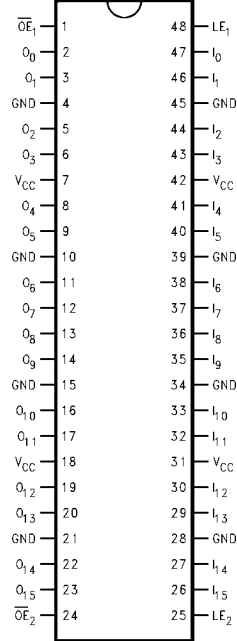**Note 2:** BGA package available in Tape and Reel only.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
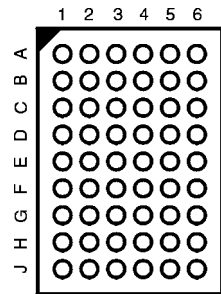
Logic Symbol

Connection Diagrams

Pin Assignment for SSOP and TSSOP

$\overline{OE}_1$	1	48	LE_1
O_0	2	47	I_0
O_1	3	46	I_1
GND	4	45	GND
O_2	5	44	I_2
O_3	6	43	I_3
V_{CC}	7	42	V_{CC}
O_4	8	41	I_4
O_5	9	40	I_5
GND	10	39	GND
O_6	11	38	I_6
O_7	12	37	I_7
O_8	13	36	I_8
O_9	14	35	I_9
GND	15	34	GND
O_{10}	16	33	I_{10}
O_{11}	17	32	I_{11}
V_{CC}	18	31	V_{CC}
O_{12}	19	30	I_{12}
O_{13}	20	29	I_{13}
GND	21	28	GND
O_{14}	22	27	I_{14}
O_{15}	23	26	I_{15}
$\overline{OE}_2$	24	25	LE_2

Pin Assignment for FBGA

(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	$\overline{OE}_1$	LE_1	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	$\overline{OE}_2$	LE_2	NC	I_{15}

Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

| Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Functional Description

The LCX162373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE_n}$) input. When $\overline{OE_n}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE_n}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams
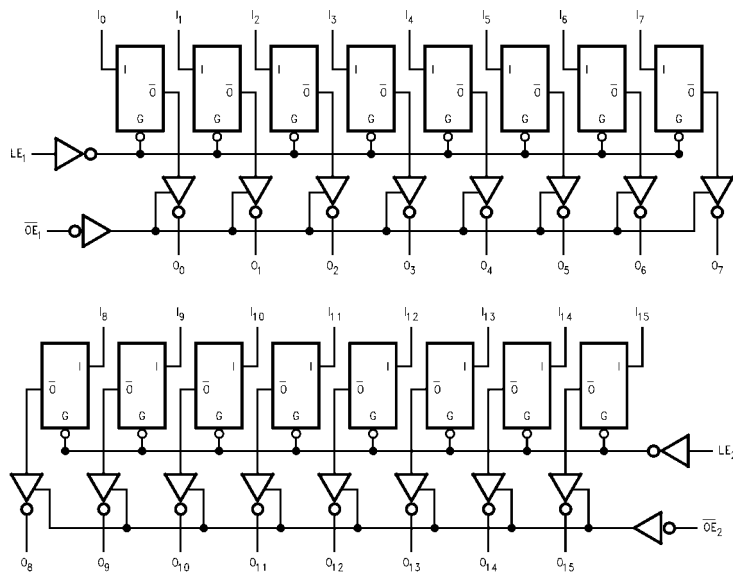
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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74LCX162373

Absolute Maximum Ratings(Note 4)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 5)	
I_{IK}	DC Input Diode Current	−50	$V_I <$ GND	mA
I_{OK}	DC Output Diode Current	−50	$V_O <$ GND	mA
		+50	$V_O > V_{CC}$	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 6)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0V – 3.6V$		12	mA
		$V_{CC} = 2.7V – 3.0V$		±8	
		$V_{CC} = 2.3V – 2.7V$		±4	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = −40°C$ to $+85°C$ Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = −100\ \mu A$	2.3 – 3.6	$V_{CC} – 0.2$		V
		$I_{OH} = −4$ mA	2.3	1.8		
		$I_{OH} = −4$ mA	2.7	2.2		
		$I_{OH} = −6$ mA	3.0	2.4		
		$I_{OH} = −8$ mA	2.7	2.0		
		$I_{OH} = −12$ mA	3.0	2.0		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\ \mu A$	2.3 – 3.6		0.2	V
		$I_{OL} = 4$ mA	2.3		0.6	
		$I_{OL} = 4$ mA	2.7		0.4	
		$I_{OL} = 6$ mA	3.0		0.55	
		$I_{OL} = 8$ mA	2.7		0.6	
		$I_{OL} = 12$ mA	3.0		0.8	
I_I	Input Leakage Current	$0 \le V_I \le 5.5V$	2.3 – 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.3 – 3.6		±5.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	μA
		$3.6V \leq V_I, V_O \leq 5.5V$ (Note 7)	2.3 – 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} -0.6V$	2.3 – 3.6		500	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500Ω$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	6.2	1.5	6.7	1.5	7.4	ns
t_{PLH}	I_n to O_n	1.5	6.2	1.5	6.7	1.5	7.4	
t_{PHL}	Propagation Delay	1.5	6.3	1.5	7.2	1.5	7.6	ns
t_{PLH}	LE to O_n	1.5	6.3	1.5	7.2	1.5	7.6	
t_{PZL}	Output Enable Time	1.5	6.9	1.5	7.3	1.5	9.0	ns
t_{PZH}		1.5	6.9	1.5	7.3	1.5	9.0	
t_{PLZ}	Output Disable Time	1.5	6.0	1.5	6.3	1.5	7.2	ns
t_{PHZ}		1.5	6.0	1.5	6.3	1.5	7.2	
t_S	Setup Time, I_n to LE	2.5		2.5		3.0		ns
t_H	Hold Time, I_n to LE	1.5		1.5		2.0		ns
t_W	LE Pulse Width	3.0		3.0		3.5		ns
t_{OSHL}	Output to Output Skew (Note 8)		1.0					ns
t_{OSLH}			1.0					

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.35	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.25	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.35	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.25	

Capacitance

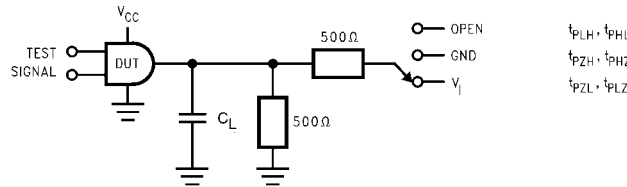| Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} =$ Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

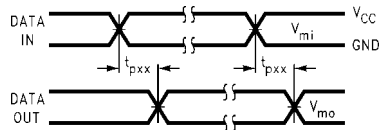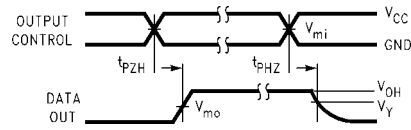# AC LOADING and WAVEFORMS Generic for LCX Family
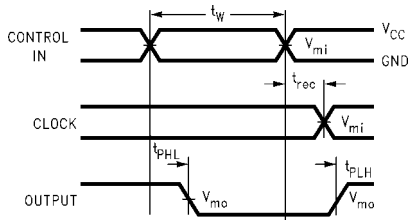

FIGURE 1. AC Test Circuit (C$_L$ includes probe and jig capacitance)

Test	Switch
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 ± 0.3V, and 2.7V V$_{CC}$ x 2 at V$_{CC}$ = 2.5 ± 0.2V
t$_{PZH}$, t$_{PHZ}$	GND

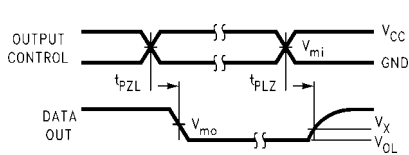**Waveform for Inverting and Non-Inverting Functions**

3-STATE Output High Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t$_{rec}$ Waveforms
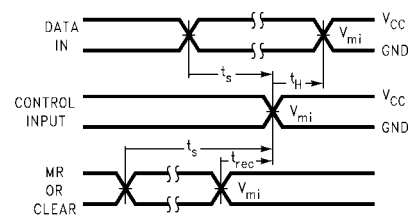
Setup Time, Hold Time and Recovery Time for Logic
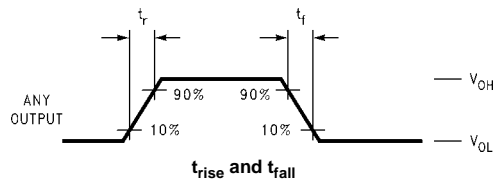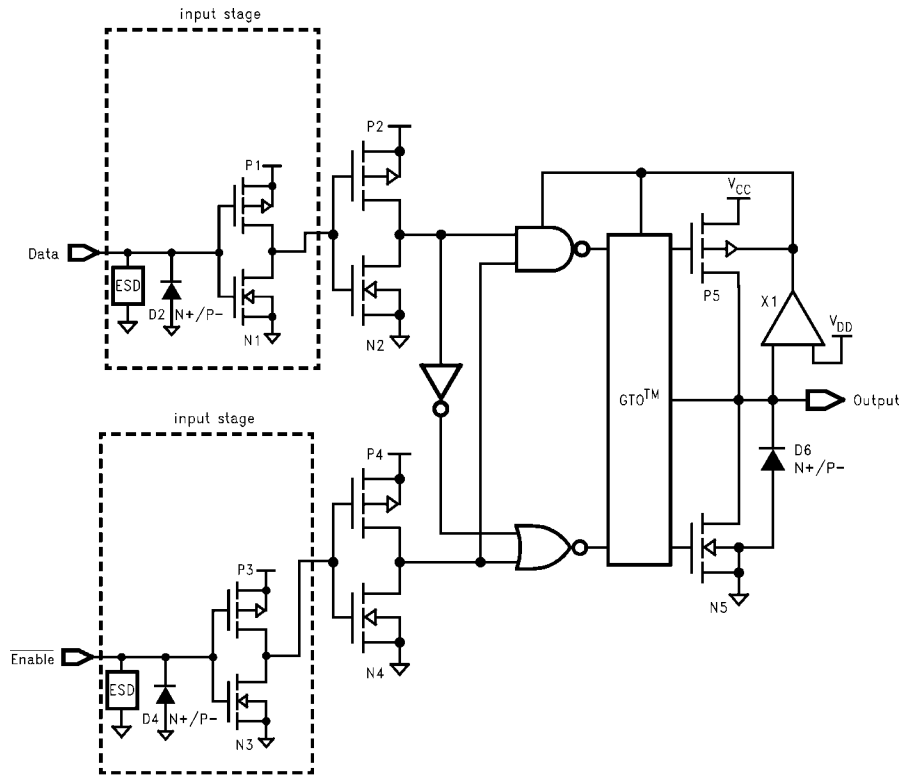

3-STATE Output Low Enable and Disable Times for Logic

t$_{rise}$ and t$_{fall}$

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t$_r$ = t$_f$ = 3ns)

Symbol	V$_{CC}$		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

Schematic Diagram Generic for LCX Family

Physical Dimensions inches (millimeters) unless otherwise noted

Top
View

Bottom
View

PIN ONE

54X 0.5 +0.05 / -0.05

Top View dimensions: 5.5, 8

Bottom View dimensions: 4, 0.8, 0.4, (0.8), (0.75), 6.4, 0.8

A B C D E F G H J

1 2 3 4 5 6

| 0.15 Ⓜ | C | A | B |
| 0.08 Ⓜ | C | | |

// 0.15 C

1.4MAX

0.45
0.35

SEATING PLANE

0.10 C

C
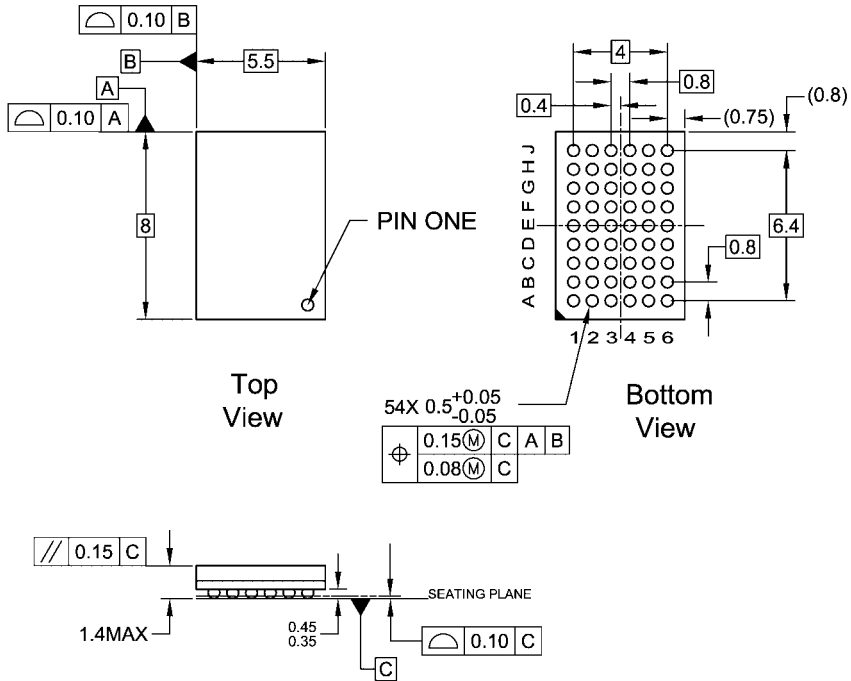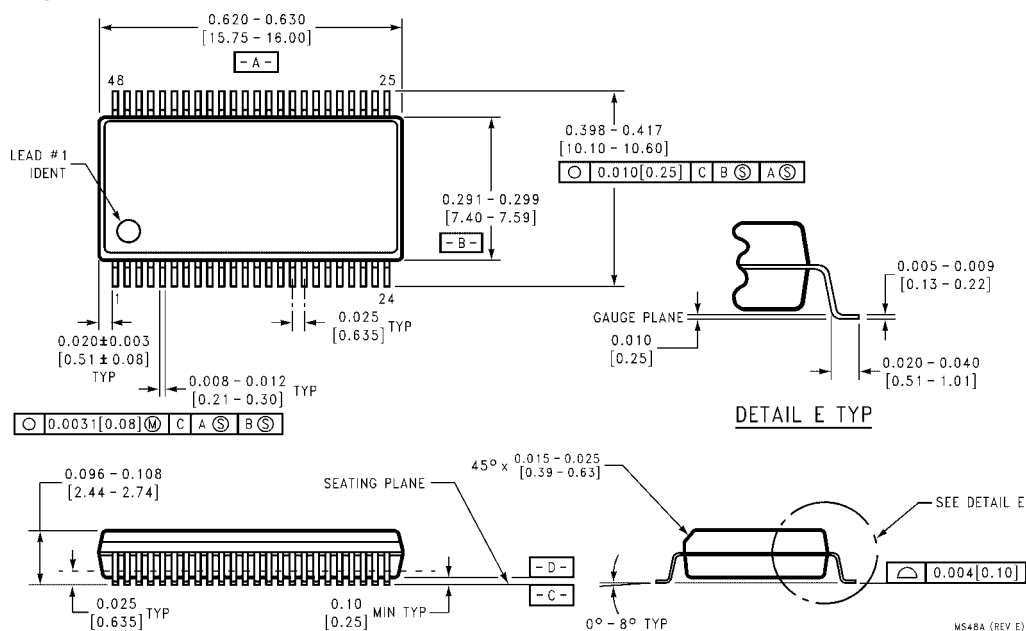
NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
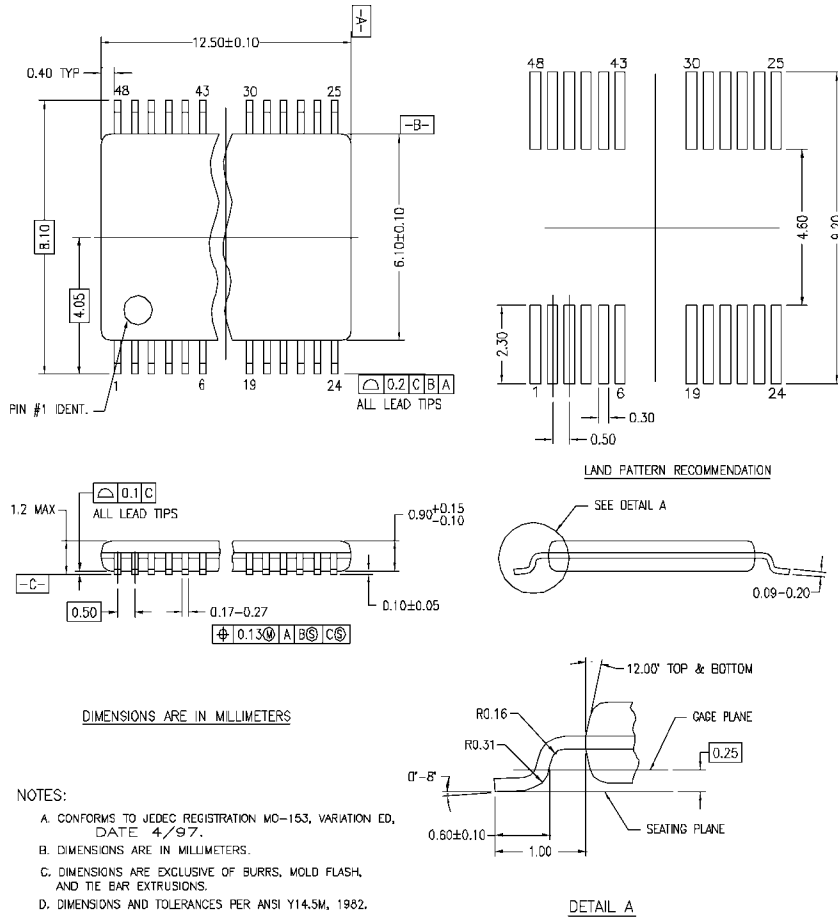D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.620 – 0.630
[15.75 – 16.00]
– A –

48   25

LEAD #1
IDENT

0.291 – 0.299
[7.40 – 7.59]
– B –

1   24

0.025
[0.635] TYP

0.020±0.003
[0.51 ± 0.08]
TYP

0.008 – 0.012
[0.21 – 0.30] TYP

⌀ 0.0031[0.08]Ⓜ C A Ⓢ B Ⓢ

0.398 – 0.417
[10.10 – 10.60]

⌀ 0.010[0.25] C B Ⓢ A Ⓢ

GAUGE PLANE

0.010
[0.25]

0.005 – 0.009
[0.13 – 0.22]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

– D –

– C –

45° x 0.015 – 0.025
[0.39 – 0.63]

0° – 8° TYP

SEE DETAIL E

△ 0.004[0.10]

MS48A (REV E)

48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO–153, VARIATION ED, DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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