

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX16373FT

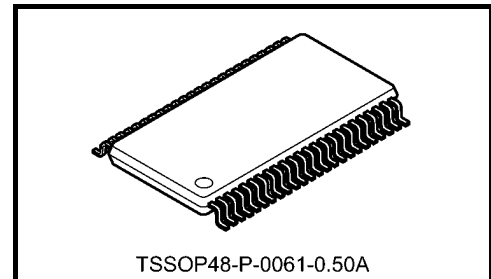
Low-Voltage 16-Bit D-Type Latch with 5-V Tolerant Inputs and Outputs

The TC74LCX16373FT is a high-performance CMOS 16-bit D-type latch. Designed for use in 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (2.5-V or 3.3-V) VCC applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This 16-bit D-type latch is controlled by a latch enable input (LE) and an output enable input (\overline{OE}) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the \overline{OE} input is high, the outputs are in a high-impedance state.

All inputs are equipped with protection circuits against static discharge.

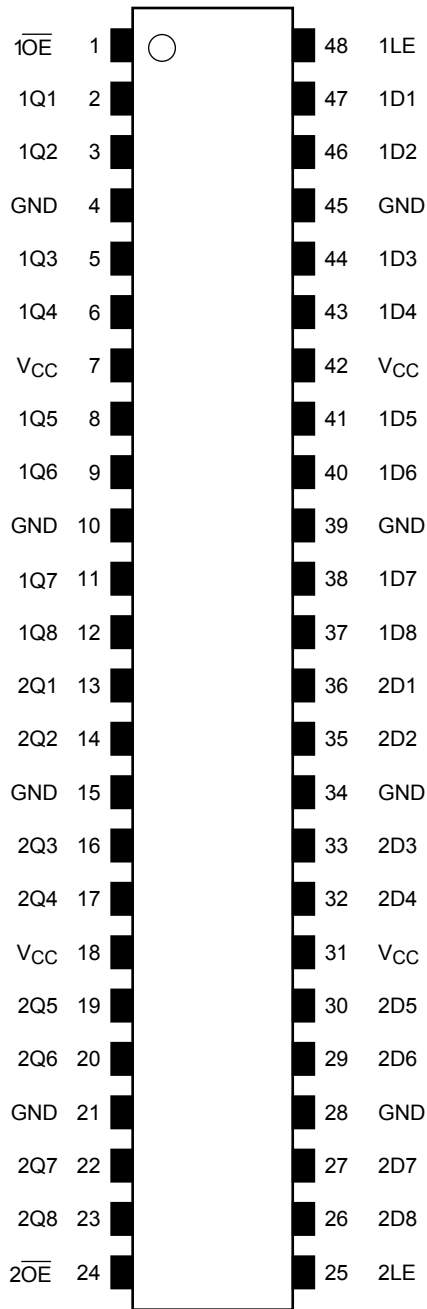


Weight: 0.25 g (typ.)

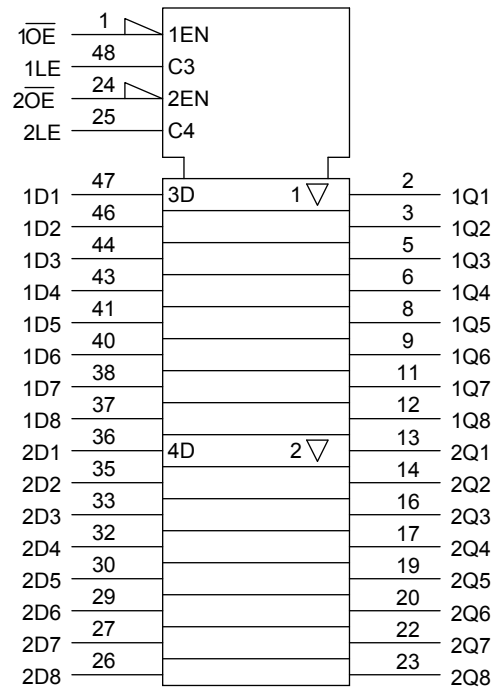
Features

- Low-voltage operation: $V_{CC} = 2.0$ to 3.6 V
- High-speed operation: $t_{pd} = 5.4$ ns (max) ($V_{CC} = 3.0$ to 3.6 V)
- Output current: $|I_{OH}|/I_{OL} = 24$ mA (min) ($V_{CC} = 3.0$ V)
- Latch-up performance: -500 mA
- Package: TSSOP
- Power-down protection provided on all inputs and outputs

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs			Outputs
$\overline{1OE}$	1LE	1D1-1D8	1Q1-1Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

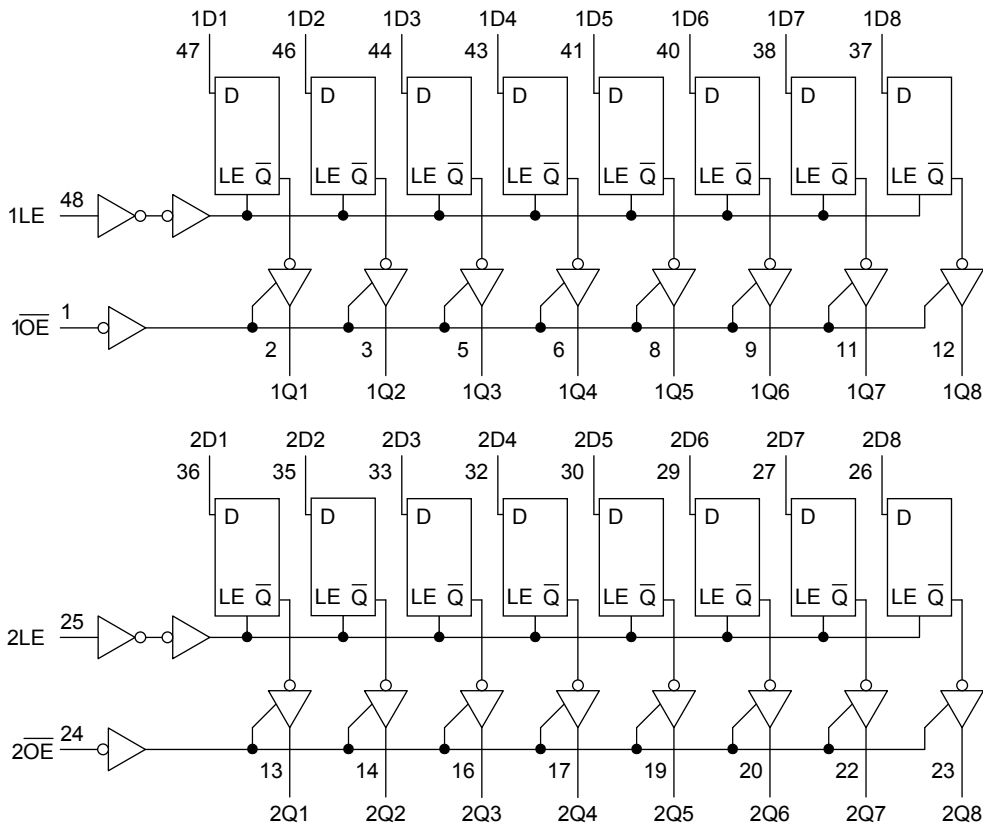
Inputs			Outputs
$\overline{2OE}$	2LE	2D1-2D8	2Q1-2Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to 6.0	V
Input voltage	V_{IN}	-0.5 to 7.0	V
Output voltage	V_{OUT}	-0.5 to 7.0 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	I_{IK}	-50	mA
Output diode current	I_{OK}	±50 (Note 4)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	400	mW
DC V_{CC} /ground current per supply pin	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0 to 3.6	V
		1.5 to 3.6 (Note 2)	
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to 5.5 (Note 3)	V
		0 to V_{CC} (Note 4)	
Output current	I_{OH}/I_{OL}	±24 (Note 5)	mA
		±12 (Note 6)	
		±8 (Note 7)	
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: Output in OFF state

Note 4: High or low state

Note 5: $V_{CC} = 3.0$ to 3.6 V

Note 6: $V_{CC} = 2.7$ to 3.0 V

Note 7: $V_{CC} = 2.3$ to 2.7 V

Note 8: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit	
Input voltage	H-level	V _{IH}	—		2.3 to 2.7	1.7	—	V	
					2.7 to 3.6	2.0	—		
	L-level	V _{IL}			2.3 to 2.7	—	0.7		
					2.7 to 3.6	—	0.8		
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}		I _{OH} = -100 μA	2.3 to 3.6	V _{CC} - 0.2	—	V
					I _{OH} = -8 mA	2.3	1.8	—	
					I _{OH} = -12 mA	2.7	2.2	—	
					I _{OH} = -18 mA	3.0	2.4	—	
					I _{OH} = -24 mA	3.0	2.2	—	
	L-level	V _{OL}			I _{OL} = 100 μA	2.3 to 3.6	—	0.2	
					I _{OL} = 8 mA	2.3	—	0.6	
					I _{OL} = 12 mA	2.7	—	0.4	
					I _{OL} = 16 mA	3.0	—	0.4	
					I _{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I _{IN}	V _{IN} = 0 to 5.5 V		2.3 to 3.6	—	±5.0	μA	
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 5.5 V		2.3 to 3.6	—	±5.0	μA	
Power-off leakage current		I _{OFF}	V _{IN} /V _{OUT} = 5.5 V		0	—	10.0	μA	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.3 to 3.6	—	20.0	μA	
			V _{IN} /V _{OUT} = 3.6 to 5.5 V		2.3 to 3.6	—	±20.0		
Increase in I _{CC} per input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V		2.3 to 3.6	—	500		

AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)		Min	Max	Unit
				CL(pF)			
Propagation delay time (D-Q)	t _{pLH} t _{pHL}	Figure 1, Figure 2	2.5 ± 0.2	30	1.5	6.5	ns
			2.7	50	1.5	5.9	
			3.3 ± 0.3	50	1.5	5.4	
Propagation delay time (LE-Q)	t _{pLH} t _{pHL}	Figure 1, Figure 2	2.5 ± 0.2	30	1.5	6.6	ns
			2.7	50	1.5	6.4	
			3.3 ± 0.3	50	1.5	5.5	
3-state output enable time	t _{pZL} t _{pZH}	Figure 1, Figure 3	2.5 ± 0.2	30	1.5	7.9	ns
			2.7	50	1.5	6.5	
			3.3 ± 0.3	50	1.5	6.1	
3-state output disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	2.5 ± 0.2	30	1.5	7.2	ns
			2.7	50	1.5	6.3	
			3.3 ± 0.3	50	1.5	6.0	
Minimum pulse width (LE)	t _w (H)	Figure 1, Figure 2	2.5 ± 0.2	30	3.5	—	ns
			2.7	50	3.0	—	
			3.3 ± 0.3	50	3.0	—	
Minimum setup time	t _s	Figure 1, Figure 2	2.5 ± 0.2	30	3.0	—	ns
			2.7	50	2.5	—	
			3.3 ± 0.3	50	2.5	—	
Minimum hold time	t _h	Figure 1, Figure 2	2.5 ± 0.2	30	2.0	—	ns
			2.7	50	1.5	—	
			3.3 ± 0.3	50	1.5	—	
Output to output skew	t _{osLH} t _{osHL}	(Note)	2.5 ± 0.2	30	—	—	ns
			2.7	50	—	—	
			3.3 ± 0.3	50	—	1.0	

Note: Parameter guaranteed by design.
 (t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)

Dynamic Switching Characteristics (Ta = 25°C, input: t_r = t_f = 2.5 ns, R_L = 500 Ω)

Characteristics	Symbol	Test Condition	V _{CC} (V)		Typ.	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	V _{IH} = 2.5 V, V _{IL} = 0 V, C _L = 30pF	2.5	0.6	V	
		V _{IH} = 3.3 V, V _{IL} = 0 V, C _L = 50pF	3.3	0.8		
Quiet output minimum dynamic V _{OL}	V _{OLV}	V _{IH} = 2.5 V, V _{IL} = 0 V, C _L = 30pF	2.5	0.6	V	
		V _{IH} = 3.3 V, V _{IL} = 0 V, C _L = 50pF	3.3	0.8		

Capacitive Characteristics (Ta = 25°C)

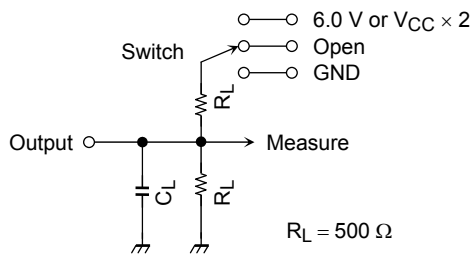
Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Input capacitance	C _{IN}	—	3.3	7	pF
Output capacitance	C _{OUT}	—	3.3	8	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz (Note)	3.3	25	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

AC Test Circuit



Parameter	Switch
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0 V @V _{CC} = 3.3 ± 0.3 V V _{CC} × 2 @V _{CC} = 2.5 ± 0.2 V
t _{pHZ} , t _{pZH}	GND

Figure 1

AC Waveform

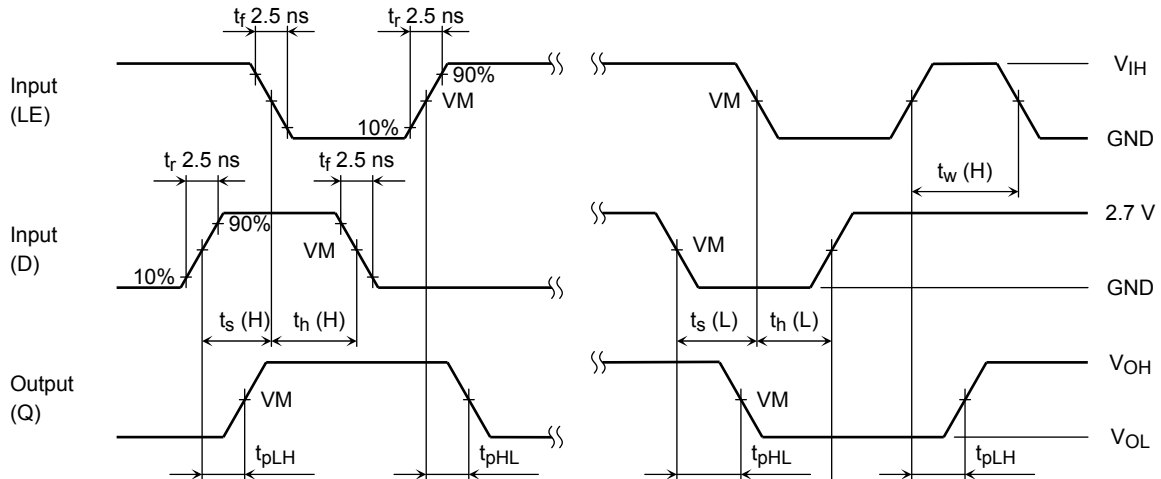


Figure 2 t_{pLH} , t_{pHL} , t_w , t_s , t_h

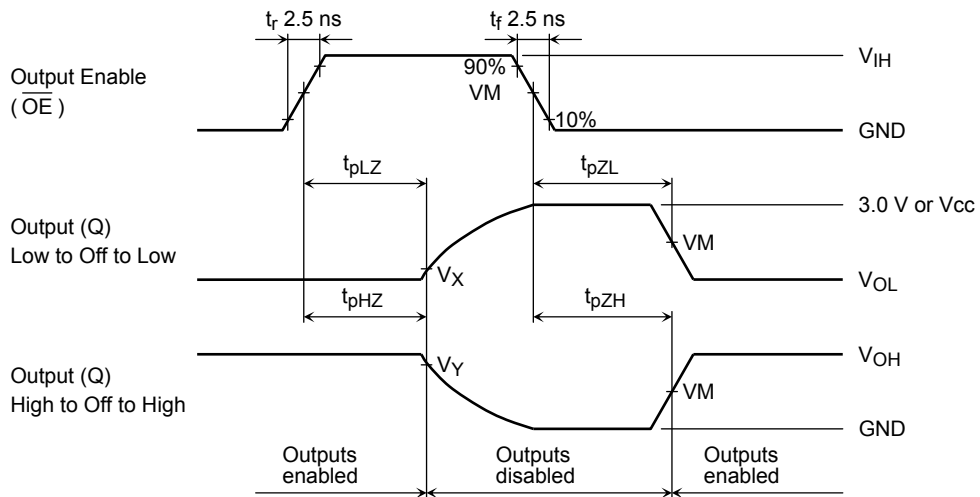


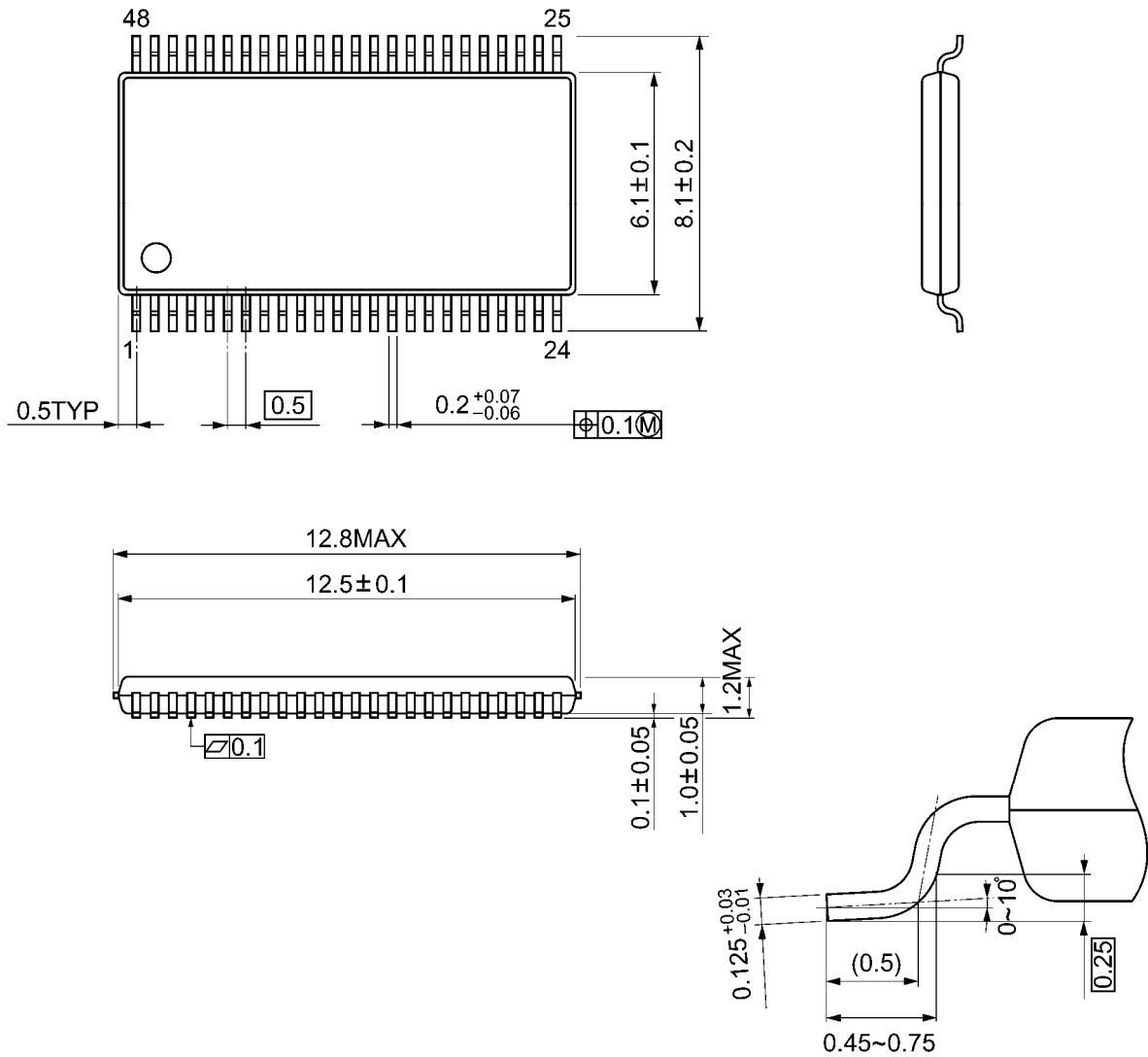
Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Symbol	V_{CC}		
	$3.3 \pm 0.3 \text{ V}$	2.7 V	$2.5 \pm 0.2 \text{ V}$
V_{IH}	2.7 V	2.7 V	V_{CC}
V_M	1.5 V	1.5 V	$V_{CC}/2$
V_X	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
V_Y	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

Package Dimensions

TSSOP48-P-0061-0.50A

Unit: mm



Weight: 0.25 g (typ.)

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