

# MC74HC573A

## Octal 3-State Noninverting Transparent Latch

### High-Performance Silicon-Gate CMOS

The MC74HC573A is identical in pinout to the LS573. The devices are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The HC573A is identical in function to the HC373A but has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

#### Features

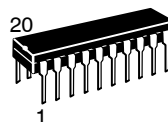
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates
- Pb-Free Packages are Available\*



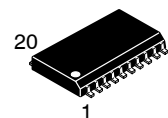
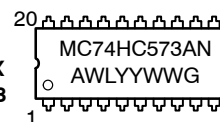
ON Semiconductor®

<http://onsemi.com>

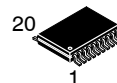
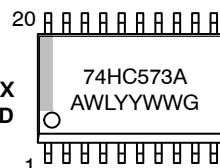
#### MARKING DIAGRAMS



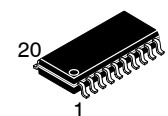
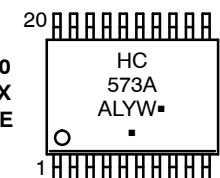
PDIP-20  
N SUFFIX  
CASE 738



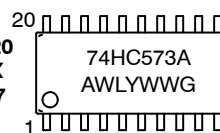
SOIC-20  
DW SUFFIX  
CASE 751D



TSSOP-20  
DT SUFFIX  
CASE 948E



SOEIAJ-20  
F SUFFIX  
CASE 967



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

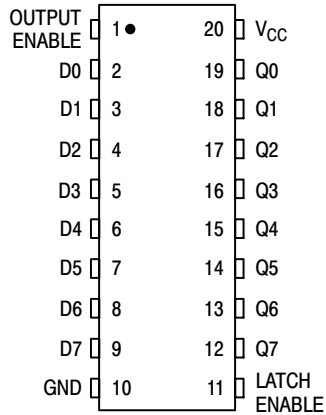
#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC573A

## PIN ASSIGNMENT



| Design Criteria                 | Value  | Units |
|---------------------------------|--------|-------|
| Internal Gate Count*            | 54.5   | ea.   |
| Internal Gate Propagation Delay | 1.5    | ns    |
| Internal Gate Power Dissipation | 5.0    | μW    |
| Speed Power Product             | 0.0075 | pJ    |

\*Equivalent to a two-input NAND gate.

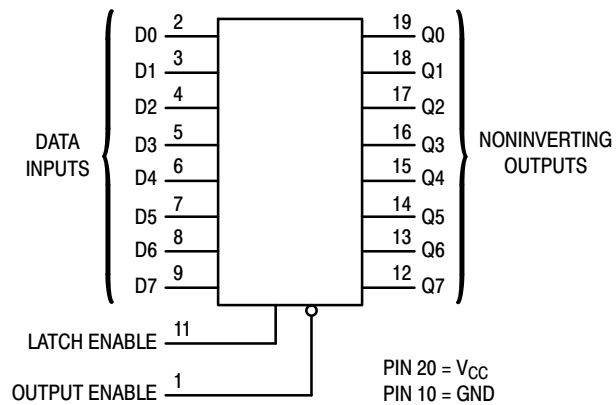
## FUNCTION TABLE

| Inputs        |              |   | Output    |
|---------------|--------------|---|-----------|
| Output Enable | Latch Enable | D | Q         |
| L             | H            | H | H         |
| L             | H            | L | L         |
| L             | L            | X | No Change |
| H             | X            | X | Z         |

X = Don't Care

Z = High Impedance

## LOGIC DIAGRAM



## ORDERING INFORMATION

| Device          | Package                | Shipping <sup>†</sup> |
|-----------------|------------------------|-----------------------|
| MC74HC573AN     | PDIP-20                | 18 Units / Rail       |
| MC74HC573ANG    | SOIC-20 (Pb-Free)      | 18 Units / Rail       |
| MC74HC573ADW    | SOIC-20 WIDE           | 38 Units / Rail       |
| MC74HC573ADWG   | SOIC-20 WIDE (Pb-Free) | 38 Units / Rail       |
| MC74HC573ADWR2  | SOIC-20 WIDE           | 1000 Tape & Reel      |
| MC74HC573ADWR2G | SOIC-20 WIDE (Pb-Free) | 1000 Tape & Reel      |
| MC74HC573ADT    | TSSOP-20*              | 75 Units / Rail       |
| MC74HC573ADTG   | TSSOP-20*              | 75 Units / Rail       |
| MC74HC573ADTR2  | TSSOP-20*              | 2500 Tape & Reel      |
| MC74HC573ADTR2G | TSSOP-20*              | 2500 Tape & Reel      |
| MC74HC573AFEL   | SOEIAJ-20              | 2000 Tape & Reel      |
| MC74HC573AFELG  | SOEIAJ-20 (Pb-Free)    | 2000 Tape & Reel      |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74HC573A

## MAXIMUM RATINGS

| Symbol    | Parameter   | Value                   | Unit |
|-----------|---|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)   | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)  | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)   | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin   | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin  | $\pm 35$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins  | $\pm 75$                | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>Plastic DIP†<br>SOIC Package†<br>TSSOP Package†      | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature   | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, TSSOP or SOIC Package) | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C  
TSSOP Package: -6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max                     | Unit |
|-------------------|--|--|-------------------------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0  | 6.0                     | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0  | $V_{CC}$                | V    |
| $T_A$             | Operating Temperature, All Package Types             | - 55   | + 125                   | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)               | $V_{CC} = 2.0 \text{ V}$<br>$V_{CC} = 4.5 \text{ V}$<br>$V_{CC} = 6.0 \text{ V}$ | 0<br>1000<br>500<br>400 | ns   |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol   | Parameter                                      | Test Conditions   | $V_{CC}$<br>V   | Guaranteed Limit |                         |                          | Unit          |
|----------|--|---|---|------------------|-------------------------|--------------------------|---------------|
|          |  |   |   | - 55 to<br>25°C  | $\leq 85^\circ\text{C}$ | $\leq 125^\circ\text{C}$ |               |
| $V_{IH}$ | Minimum High-Level Input Voltage               | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$                     | 2.0   | 1.5              | 1.5                     | 1.5                      | V             |
|          |  |   | 3.0   | 2.1              | 2.1                     | 2.1                      |               |
|          |  |   | 4.5   | 3.15             | 3.15                    | 3.15                     |               |
|          |  |   | 6.0   | 4.2              | 4.2                     | 4.2                      |               |
| $V_{IL}$ | Maximum Low-Level Input Voltage                | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$                     | 2.0   | 0.5              | 0.5                     | 0.5                      | V             |
|          |  |   | 3.0   | 0.9              | 0.9                     | 0.9                      |               |
|          |  |   | 4.5   | 1.35             | 1.35                    | 1.35                     |               |
|          |  |   | 6.0   | 1.8              | 1.8                     | 1.8                      |               |
| $V_{OH}$ | Minimum High-Level Output Voltage              | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$                                     | 2.0   | 1.9              | 1.9                     | 1.9                      | V             |
|          |  |   | 4.5   | 4.4              | 4.4                     | 4.4                      |               |
|          |  |   | 6.0   | 5.9              | 5.9                     | 5.9                      |               |
|          |  |   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 2.4 \text{ mA}$<br>$ I_{out}  \leq 6.0 \text{ mA}$<br>$ I_{out}  \leq 7.8 \text{ mA}$ | 3.0              | 2.48                    | 2.34                     |               |
| $V_{OL}$ | Maximum Low-Level Output Voltage               | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$                     | 2.0   | 0.1              | 0.1                     | 0.1                      | V             |
|          |  |   | 4.5   | 0.1              | 0.1                     | 0.1                      |               |
|          |  |   | 6.0   | 0.1              | 0.1                     | 0.1                      |               |
|          |  |   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 2.4 \text{ mA}$<br>$ I_{out}  \leq 6.0 \text{ mA}$<br>$ I_{out}  \leq 7.8 \text{ mA}$ | 3.0              | 0.26                    | 0.33                     |               |
| $I_{in}$ | Maximum Input Leakage Current                  | $V_{in} = V_{CC} \text{ or GND}$  | 6.0   | $\pm 0.1$        | $\pm 1.0$               | $\pm 1.0$                | $\mu\text{A}$ |
| $I_{OZ}$ | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>$V_{in} = V_{IL} \text{ or } V_{IH}$<br>$V_{out} = V_{CC} \text{ or GND}$ | 6.0   | - 0.5            | - 5.0                   | - 10                     | $\mu\text{A}$ |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC} \text{ or GND}$<br>$I_{out} = 0 \mu\text{A}$   | 6.0   | 4.0              | 40                      | 160                      | $\mu\text{A}$ |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

# MC74HC573A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

| Symbol                                 | Parameter   | V <sub>CC</sub><br>V | Guaranteed Limit |         |          | Unit |
|--|---|----------------------|------------------|---------|----------|------|
|  |   |                      | - 55 to 25 °C    | ≤ 85 °C | ≤ 125 °C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input D to Q<br>(Figures 1 and 5)        | 2.0                  | 150              | 190     | 225      | ns   |
|  |   | 3.0                  | 100              | 140     | 180      |      |
|  |   | 4.5                  | 30               | 38      | 45       |      |
|  |   | 6.0                  | 26               | 33      | 38       |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Latch Enable to Q<br>(Figures 2 and 5)   | 2.0                  | 160              | 200     | 240      | ns   |
|  |   | 3.0                  | 105              | 145     | 190      |      |
|  |   | 4.5                  | 32               | 40      | 48       |      |
|  |   | 6.0                  | 27               | 34      | 41       |      |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Q<br>(Figures 3 and 6)  | 2.0                  | 150              | 190     | 225      | ns   |
|  |   | 3.0                  | 100              | 125     | 150      |      |
|  |   | 4.5                  | 30               | 38      | 45       |      |
|  |   | 6.0                  | 26               | 33      | 38       |      |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Q<br>(Figures 3 and 6)  | 2.0                  | 150              | 190     | 225      | ns   |
|  |   | 3.0                  | 100              | 125     | 150      |      |
|  |   | 4.5                  | 30               | 38      | 45       |      |
|  |   | 6.0                  | 26               | 33      | 38       |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 5)     | 2.0                  | 60               | 75      | 90       | ns   |
|  |   | 3.0                  | 27               | 32      | 36       |      |
|  |   | 4.5                  | 12               | 15      | 18       |      |
|  |   | 6.0                  | 10               | 13      | 15       |      |
| C <sub>in</sub>                        | Maximum Input Capacitance   |                      | 10               | 10      | 10       | pF   |
| C <sub>out</sub>                       | Maximum 3-State Output Capacitance (Output in High-Impedance State) |                      | 15               | 15      | 15       | pF   |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |  | pF |
|-----------------|---|---|--|----|
|                 |   | 23                                      |  |    |
|                 |   |   |  |    |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## TIMING REQUIREMENTS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

| Symbol                          | Parameter                                   | Figure | V <sub>CC</sub><br>V | Guaranteed Limit |      |         |      |          |      | Unit |
|---------------------------------|---|--------|----------------------|------------------|------|---------|------|----------|------|------|
|                                 |   |        |                      | - 55 to 25 °C    |      | ≤ 85 °C |      | ≤ 125 °C |      |      |
|                                 |   |        |                      | Min              | Max  | Min     | Max  | Min      | Max  |      |
| t <sub>su</sub>                 | Minimum Setup Time, Input D to Latch Enable | 4      | 2.0                  | 50               |      | 65      |      | 75       |      | ns   |
|                                 |   |        | 3.0                  | 40               |      | 50      |      | 60       |      |      |
|                                 |   |        | 4.5                  | 10               |      | 13      |      | 15       |      |      |
|                                 |   |        | 6.0                  | 9.0              |      | 11      |      | 13       |      |      |
| t <sub>h</sub>                  | Minimum Hold Time, Latch Enable to Input D  | 4      | 2.0                  | 5.0              |      | 5.0     |      | 5.0      |      | ns   |
|                                 |   |        | 3.0                  | 5.0              |      | 5.0     |      | 5.0      |      |      |
|                                 |   |        | 4.5                  | 5.0              |      | 5.0     |      | 5.0      |      |      |
|                                 |   |        | 6.0                  | 5.0              |      | 5.0     |      | 5.0      |      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Latch Enable           | 2      | 2.0                  | 75               |      | 95      |      | 110      |      | ns   |
|                                 |   |        | 3.0                  | 60               |      | 80      |      | 90       |      |      |
|                                 |   |        | 4.5                  | 15               |      | 19      |      | 22       |      |      |
|                                 |   |        | 6.0                  | 13               |      | 16      |      | 19       |      |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times           | 1      | 2.0                  |                  | 1000 |         | 1000 |          | 1000 | ns   |
|                                 |   |        | 3.0                  |                  | 800  |         | 800  |          | 800  |      |
|                                 |   |        | 4.5                  |                  | 500  |         | 500  |          | 500  |      |
|                                 |   |        | 6.0                  |                  | 400  |         | 400  |          | 400  |      |

# MC74HC573A

## SWITCHING WAVEFORMS

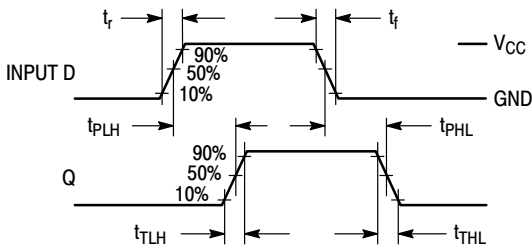


Figure 1.

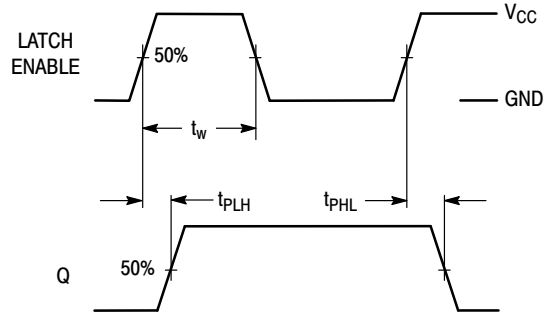


Figure 2.

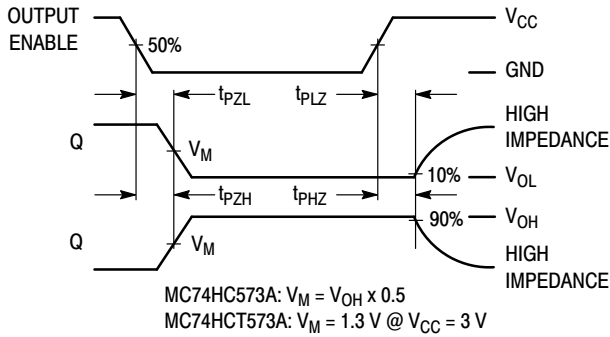


Figure 3.

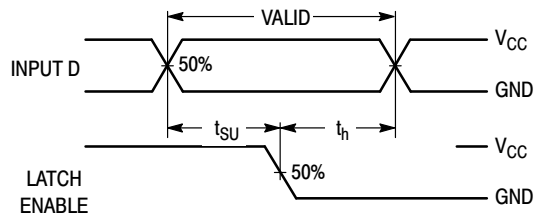
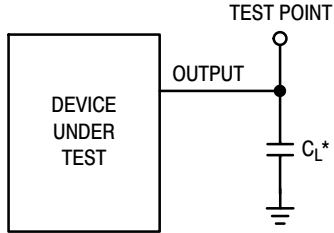
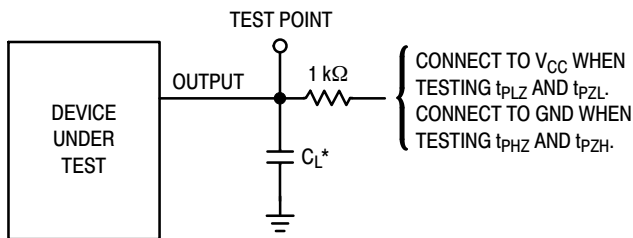


Figure 4.



\*Includes all probe and jig capacitance

Figure 5. Test Circuit



\*Includes all probe and jig capacitance

Figure 6. Test Circuit

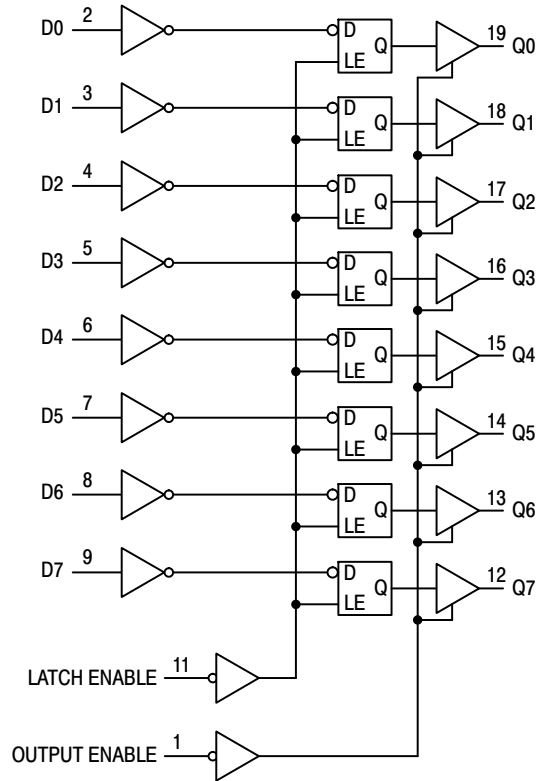
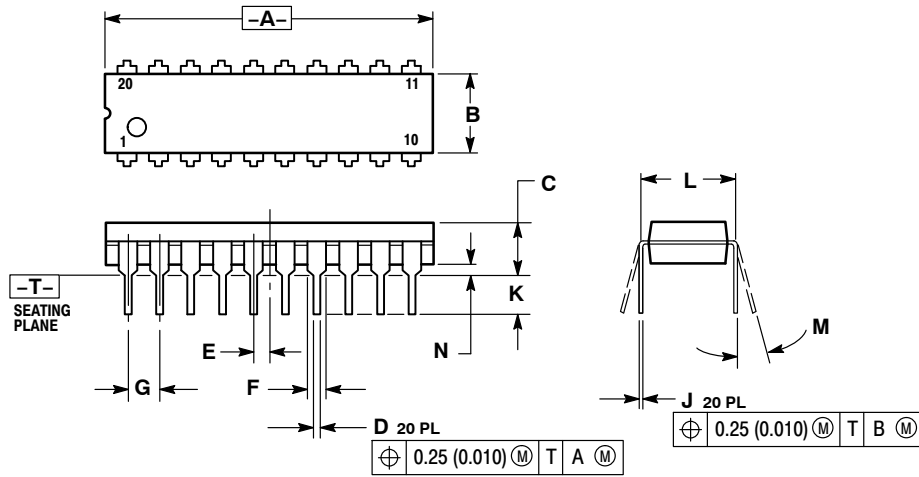


Figure 7. EXPANDED LOGIC DIAGRAM

# MC74HC573A

## PACKAGE DIMENSIONS

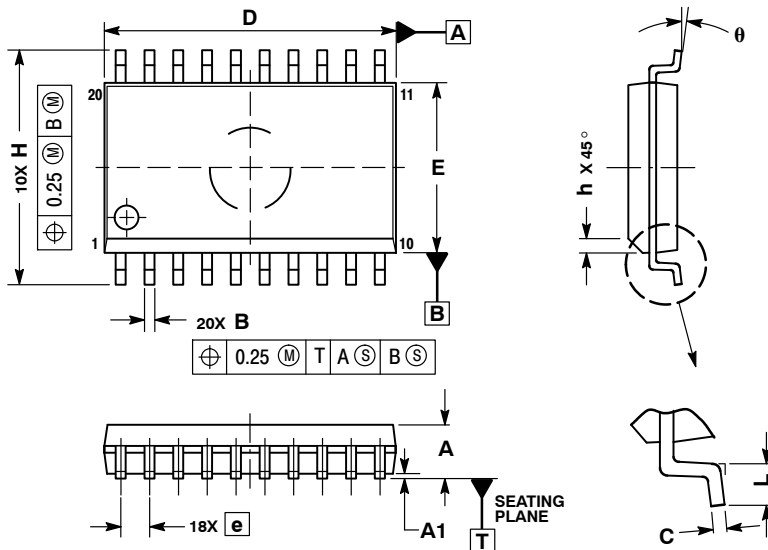
PDIP-20  
N SUFFIX  
CASE 738-03  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.010     | 1.070 | 25.66       | 27.17 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.150     | 0.180 | 3.81        | 4.57  |
| D   | 0.015     | 0.022 | 0.39        | 0.55  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.050     | 0.070 | 1.27        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.140 | 2.80        | 3.55  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |

SOIC-20  
DW SUFFIX  
CASE 751D-05  
ISSUE G



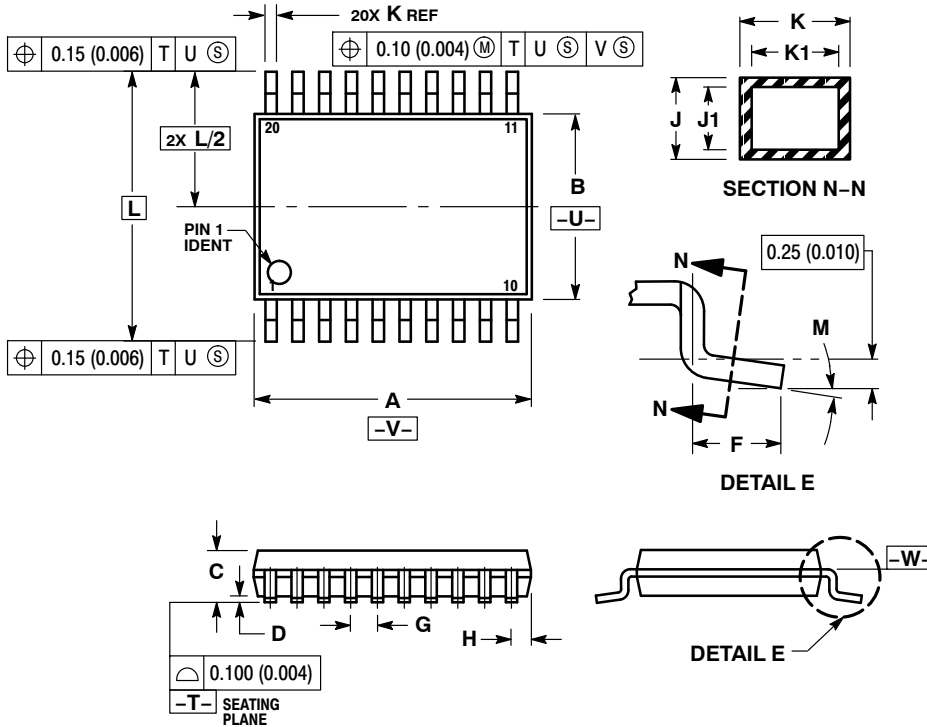
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM      | MILLIMETERS |       |
|----------|-------------|-------|
|          | MIN         | MAX   |
| A        | 2.35        | 2.65  |
| A1       | 0.10        | 0.25  |
| B        | 0.35        | 0.49  |
| C        | 0.23        | 0.32  |
| D        | 12.65       | 12.95 |
| E        | 7.40        | 7.60  |
| e        | 1.27 BSC    |       |
| H        | 10.05       | 10.55 |
| h        | 0.25        | 0.75  |
| L        | 0.50        | 0.90  |
| $\theta$ | 0°          | 7°    |

# MC74HC573A

## PACKAGE DIMENSIONS

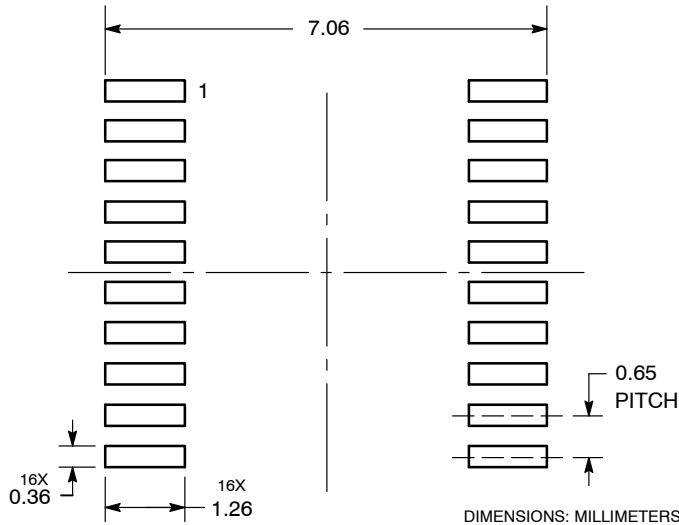
TSSOP-20  
DT SUFFIX  
CASE 948E-02  
ISSUE C



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

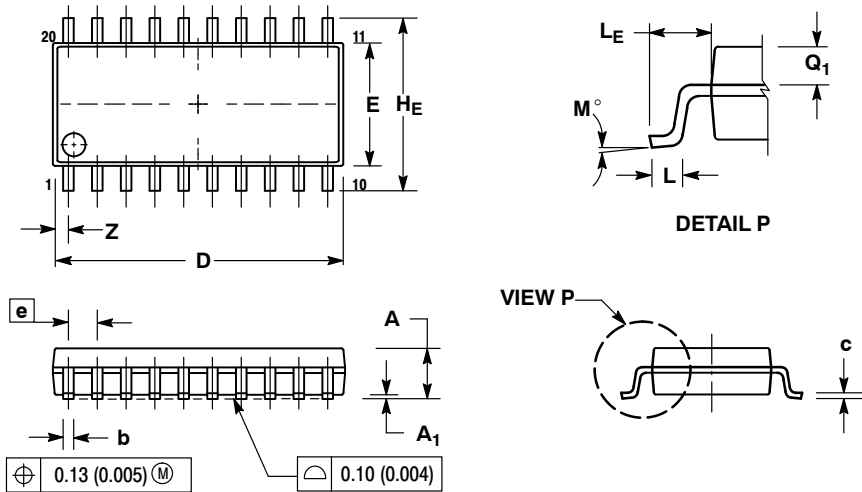
### SOLDERING FOOTPRINT



# MC74HC573A

## PACKAGE DIMENSIONS

SOEIAJ-20  
F SUFFIX  
CASE 967-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.15        | 0.25  | 0.006     | 0.010 |
| D              | 12.35       | 12.80 | 0.486     | 0.504 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| HE             | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| LE             | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.81  | ---       | 0.032 |

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