

# NBSG86A

## 2.5V/3.3V SiGe Differential Smart Gate with Output Level Select

The NBSG86A is a multi-function differential Logic Gate which can be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1 MUX. This device is part of the GigaComm™ family of high performance Silicon Germanium products. The device is housed in a low profile 4x4 mm, 16-pin, flip-chip LGA or a 3x3 mm 16 pin QFN package.

Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The Output Level Select (OLS) input is used to program the peak-to-peak output amplitude between 0 and 800 mV in five discrete steps.

The NBSG86A employs input default circuitry so that under open input conditions ( $D_x$ ,  $\overline{D}_x$ ,  $\overline{VTD}_x$ ,  $VTD_x$ , VTSEL) the outputs of the device will remain stable.

### Features

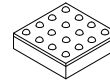
- Maximum Input Clock Frequency > 8 GHz Typical
- Maximum Input Data Rate > 8 Gb/s Typical
- 165 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- Selectable Swing PECL Output with Operating Range:  $V_{CC} = 2.375 \text{ V}$  to  $3.465 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- Selectable Swing NECL Output with NECL Inputs with Operating Range:  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -2.375 \text{ V}$  to  $-3.465 \text{ V}$
- Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak-to-Peak Output)
- 50 Ω Internal Input Termination Resistors
- Pb-Free Packages are Available



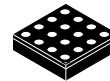
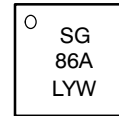
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<http://onsemi.com>

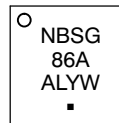
### MARKING DIAGRAMS\*



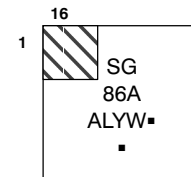
FCBGA-16  
BA SUFFIX  
CASE 489



FCLGA-16  
MA SUFFIX  
CASE 526



QFN-16  
MN SUFFIX  
CASE 485G



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

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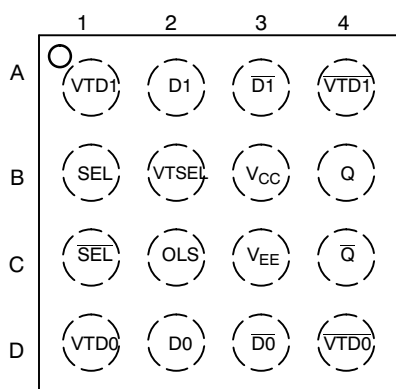


Figure 1. BGA-16 and LGA-16 Pinout (Top View)

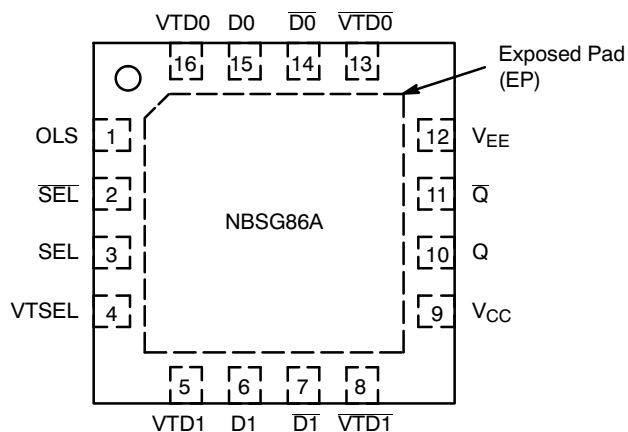


Figure 2. QFN-16 Pinout (Top View)

Table 1. Pin Description

| Pin |     | Name            | I/O  | Description   |
|-----|-----|-----------------|--|---|
| BGA | QFN |                 |  |   |
| C2  | 1   | OLS<br>(Note 3) | Input                                      | Input Pin for the Output Level Select (OLS). See Table 2.   |
| C1  | 2   | SEL-bar         | ECL, CML,<br>LVCMOS, LVDS,<br>LVTTTL Input | Inverted Differential Select Logic Input.   |
| B1  | 3   | SEL             | ECL, CML,<br>LVCMOS, LVDS,<br>LVTTTL Input | Noninverted Differential Select Logic Input.  |
| B2  | 4   | VTSEL           | -  | Common Internal 50 $\Omega$ Termination Pin for SEL/SEL-bar. See Table 7. (Note 1)  |
| A1  | 5   | VTD1            | -  | Internal 50 $\Omega$ termination pin. See Table 7. (Note 1)   |
| A2  | 6   | D1              | ECL, CML,<br>LVCMOS, LVDS,<br>LVTTTL Input | Noninverted Differential Input 1. Internal 75 k $\Omega$ to V <sub>EE</sub> .   |
| A3  | 7   | D1-bar          | ECL, CML,<br>LVCMOS, LVDS,<br>LVTTTL Input | Inverted Differential Input 1. Internal 75 k $\Omega$ to V <sub>EE</sub> and 36.5 k $\Omega$ to V <sub>CC</sub> .           |
| A4  | 8   | VTD1-bar        | -  | Internal 50 $\Omega$ Termination Pin. See Table 7. (Note 1)   |
| B3  | 9   | V <sub>CC</sub> | -  | Positive Supply Voltage (Note 2)  |
| B4  | 10  | Q               | RSECL Output                               | Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to V <sub>TT</sub> = V <sub>CC</sub> - 2 V. |
| C4  | 11  | Q-bar           | RSECL Output                               | Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to V <sub>TT</sub> = V <sub>CC</sub> - 2 V     |
| C3  | 12  | V <sub>EE</sub> | -  | Negative Supply Voltage (Note 2)  |
| D4  | 13  | VTD0-bar        | -  | Internal 50 $\Omega$ Termination Pin. See Table 7. (Note 1)   |
| D3  | 14  | D0-bar          | ECL, CML,<br>LVCMOS, LVDS,<br>LVTTTL Input | Inverted Differential Input 0. Internal 75 k $\Omega$ to V <sub>EE</sub> and 36.5 k $\Omega$ to V <sub>CC</sub> .           |
| D2  | 15  | D0              | ECL, CML,<br>LVCMOS, LVDS,<br>LVTTTL Input | Noninverted Differential Input 0. Internal 75 k $\Omega$ to V <sub>EE</sub> .   |
| D1  | 16  | VTD0            | -  | Internal 50 $\Omega$ Termination Pin. See Table 7. (Note 1)   |
| N/A | -   | EP              | -  | Exposed Pad. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat-sinking conduit.     |

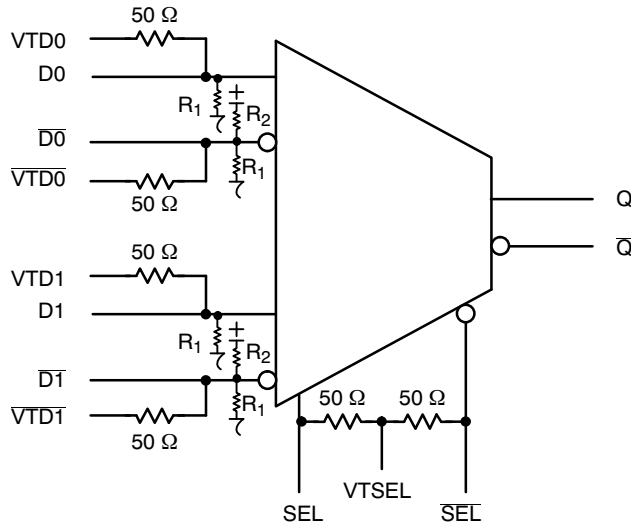
1. In the differential configuration when the input termination pins (VTDx, VTDx-bar, VTSEL) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.
2. All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.
3. When an output level of 400 mV is desired and V<sub>CC</sub> - V<sub>EE</sub> > 3.0 V, 2 k $\Omega$  resistor should be connected from OLS pin to V<sub>EE</sub>.

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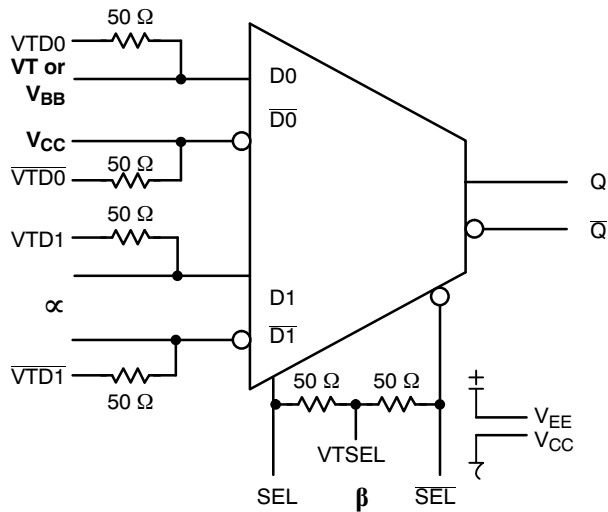
**Table 2. OUTPUT LEVEL SELECT OLS**

| OLS               | Q/Q VPP | OLS Sensitivity  |
|-------------------|---------|------------------|
| $V_{CC}$          | 800 mV  | OLS - 75 mV      |
| $V_{CC} - 0.4 V$  | 200 mV  | OLS $\pm$ 150 mV |
| $V_{CC} - 0.8 V$  | 600 mV  | OLS $\pm$ 100 mV |
| $V_{CC} - 1.2 V$  | 0       | OLS $\pm$ 75 mV  |
| $V_{EE}$ (Note 4) | 400 mV  | OLS $\pm$ 100 mV |
| Float             | 600 mV  | N/A              |

4. When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0 V$ , 2.0 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .



**Figure 3. Logic Diagram**



**Figure 4. Configuration for AND/NAND Function**

**Table 3. AND/NAND TRUTH TABLE (Note 5)**

|    | $\alpha$ | $\beta$ | $\alpha * \beta$ |
|----|----------|---------|------------------|
| D0 | D1       | SEL     | Q                |
| 0  | 0        | 0       | 0                |
| 0  | 0        | 1       | 0                |
| 0  | 1        | 0       | 0                |
| 0  | 1        | 1       | 1                |

5.  $\overline{D0}$ ,  $\overline{D1}$ ,  $\overline{SEL}$  are inverse of D0, D1, SEL unless specified otherwise.

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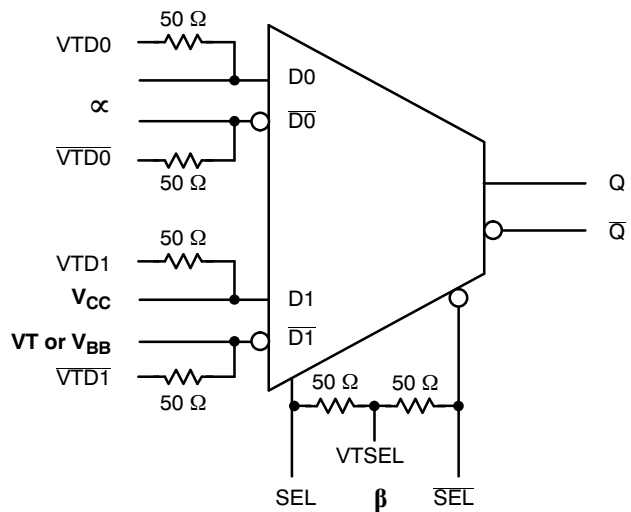


Figure 5. Configuration for OR/NOR Function

Table 4. OR/NOR TRUTH TABLE\*\*

| $\alpha$ |    | $\beta$ | $\alpha$ or $\beta$ |
|----------|----|---------|---------------------|
| D0       | D1 | SEL     | Q                   |
| 0        | 1  | 0       | 0                   |
| 0        | 1  | 1       | 1                   |
| 1        | 1  | 0       | 1                   |
| 1        | 1  | 1       | 1                   |

\*\* D0, D1, SEL are inverse of D0, D1, SEL unless specified otherwise.

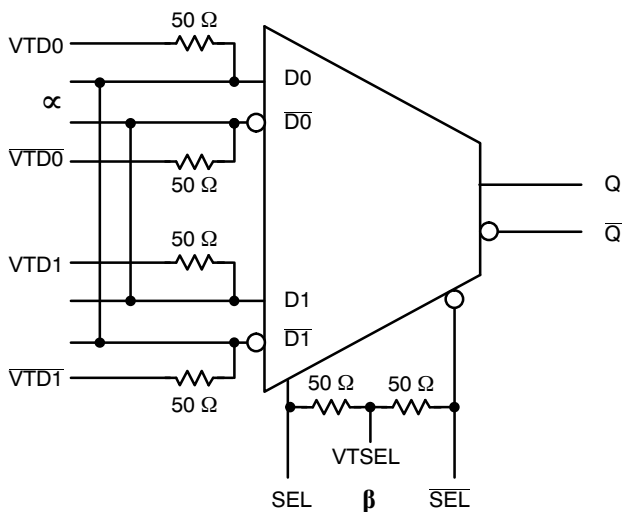


Figure 6. Configuration for XOR/XNOR Function

Table 5. XOR/XNOR TRUTH TABLE\*\*

| $\alpha$ |    | $\beta$ | $\alpha$ XOR $\beta$ |
|----------|----|---------|----------------------|
| D0       | D1 | SEL     | Q                    |
| 0        | 1  | 0       | 0                    |
| 0        | 1  | 1       | 1                    |
| 1        | 0  | 0       | 1                    |
| 1        | 0  | 1       | 0                    |

\*\* D0, D1, SEL are inverse of D0, D1, SEL unless specified otherwise.

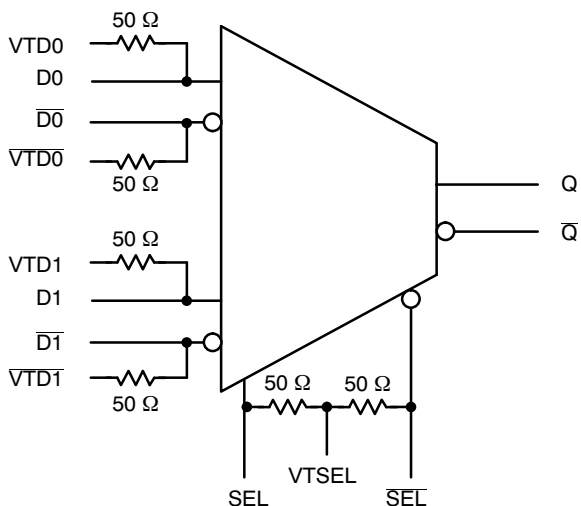


Figure 7. Configuration for 2:1 MUX Function

Table 6. 2:1 MUX TRUTH TABLE\*\*

| SEL | Q  |
|-----|----|
| 1   | D1 |
| 0   | D0 |

\*\* D0, D1, SEL are inverse of D0, D1, SEL unless specified otherwise.

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**Table 7. Interfacing Options**

| INTERFACING OPTIONS | CONNECTIONS  |
|---------------------|--|
| CML                 | Connect VTD0, VTD1, VTSEL and $\overline{\text{VTD0}}$ , $\overline{\text{VTD1}}$ to $V_{CC}$  |
| LVDS                | Connect VTD0, VTD1, $\overline{\text{VTD0}}$ and $\overline{\text{VTD1}}$ together. Leave VTSEL open.  |
| AC-COUPLED          | Bias VTD0, VTD1, VTSEL and $\overline{\text{VTD0}}$ , $\overline{\text{VTD1}}$ Inputs within (VIHCMR) Common Mode Range                                  |
| RSECL, PECL, NECL   | Standard ECL Termination Techniques  |
| LVTTTL, LVCMOS      | An external voltage should be applied to the unused complementary differential input. Nominal voltage 1.5 V for LVTTTL and $V_{CC}/2$ for LVCMOS inputs. |

**Table 8. ATTRIBUTES**

| Characteristics  | Value   |                            |
|--|---|----------------------------|
| Internal Input Pulldown Resistors ( $R_1$ )            | 75 k $\Omega$   |                            |
| Internal Input Pullup Resistor ( $R_2$ )               | 37.5 k $\Omega$   |                            |
| ESD Protection   | Human Body Model<br>Machine Model<br>Charged Device Model | > 1 KV<br>> 50 V<br>> 4 KV |
| Moisture Sensitivity (Note 6)                          | Pb Pkg  | Pb-Free Pkg                |
|  | FCBGA-16, FCLGA-16<br>16-QFN                              | Level 3<br>Level 1         |
| Flammability Rating                                    | Oxygen Index: 28 to 34                                    | UL 94 V-0 @ 0.125 in       |
| Transistor Count                                       | 364   |                            |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |   |                            |

6. For additional information, see Application Note AND8003/D.

**Table 9. MAXIMUM RATINGS** (Note 7)

| Symbol        | Parameter  | Condition 1   | Condition 2  | Rating                     | Units  |
|---------------|--|---|--|----------------------------|--|
| $V_{CC}$      | Positive Power Supply                                | $V_{EE} = 0 \text{ V}$  |  | 3.6                        | V  |
| $V_{EE}$      | Negative Power Supply                                | $V_{CC} = 0 \text{ V}$  |  | -3.6                       | V  |
| $V_I$         | Positive Input<br>Negative Input                     | $V_{EE} = 0 \text{ V}$<br>$V_{CC} = 0 \text{ V}$                          | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$                 | 3.6<br>-3.6                | V<br>V   |
| $V_{INPP}$    | Differential Input Voltage $ D_n - \overline{D_n} $  | $V_{CC} - V_{EE} \geq 2.8 \text{ V}$<br>$V_{CC} - V_{EE} < 2.8 \text{ V}$ |  | 2.8<br>$ V_{CC} - V_{EE} $ | V<br>V   |
| $I_{IN}$      | Input Current Through $R_T$ (50 $\Omega$ Resistor)   | Static<br>Surge   |  | 45<br>80                   | mA<br>mA   |
| $I_{out}$     | Output Current                                       | Continuous<br>Surge   |  | 25<br>50                   | mA<br>mA   |
| $T_A$         | Operating Temperature Range                          | 16-FCBGA, FCLGA<br>16-QFN   |  | -40 to +70<br>-40 to +85   | $^{\circ}\text{C}$<br>$^{\circ}\text{C}$   |
| $T_{stg}$     | Storage Temperature Range                            |   |  | -65 to +150                | $^{\circ}\text{C}$   |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)<br>(Note 8) | 0 lfpm<br>500 lfpm<br>0 lfpm<br>500 lfpm                                  | 16 FCBGA, FCLGA<br>16 FCBGA, FCLGA<br>16 QFN<br>16 QFN | 108<br>86<br>41.6<br>35.2  | $^{\circ}\text{C}/\text{W}$<br>$^{\circ}\text{C}/\text{W}$<br>$^{\circ}\text{C}/\text{W}$<br>$^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)                | 2S2P (Note 8)<br>2S2P (Note 9)  | 16 FCBGA, FCLGA<br>16 QFN                              | 5.0<br>4.0                 | $^{\circ}\text{C}/\text{W}$<br>$^{\circ}\text{C}/\text{W}$   |
| $T_{sol}$     | Wave Solder  | Pb (BGA)<br>Pb-Free   | < 15 sec<br>< 3 sec @ 260 $^{\circ}\text{C}$           | 225<br>265                 | $^{\circ}\text{C}$   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

7. Maximum Ratings are those values beyond which device damage may occur.

8. JEDEC standard multilayer board - 2S2P (2 signal, 2 power).

9. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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**Table 10. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT**  $V_{CC} = 2.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 10)

| Symbol      | Characteristic   | -40°C           |                   |                | 25°C            |                   |                | 70°C(LGA)/85°C(QFN)** |                   |                | Unit          |
|-------------|--|-----------------|-------------------|----------------|-----------------|-------------------|----------------|-----------------------|-------------------|----------------|---------------|
|             |  | Min             | Typ               | Max            | Min             | Typ               | Max            | Min                   | Typ               | Max            |               |
| $I_{EE}$    | Negative Power Supply Current  | 23              | 30                | 39             | 23              | 30                | 39             | 23                    | 30                | 39             | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 11)  | 1460            | 1510              | 1560           | 1490            | 1540              | 1590           | 1515                  | 1565              | 1615           | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 11)   |                 |                   |                |                 |                   |                |                       |                   |                | mV            |
|             | (OLS = $V_{CC}$ )  | 555             | 705               | 855            | 595             | 745               | 895            | 625                   | 775               | 925            |               |
|             | (OLS = $V_{CC} - 0.4\text{ V}$ )   | 1235            | 1295              | 1385           | 1270            | 1330              | 1420           | 1295                  | 1355              | 1445           |               |
|             | (OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)                                  | 775             | 895               | 1015           | 810             | 930               | 1050           | 840                   | 960               | 1080           |               |
|             | (OLS = $V_{CC} - 1.2\text{ V}$ )   | 1455            | 1505              | 1585           | 1490            | 1540              | 1620           | 1510                  | 1560              | 1640           |               |
|             | (OLS = $V_{EE}$ )  | 1005            | 1095              | 1215           | 1040            | 1130              | 1250           | 1065                  | 1155              | 1275           |               |
| $V_{OUTPP}$ | Output Voltage Amplitude   |                 |                   |                |                 |                   |                |                       |                   |                | mV            |
|             | (OLS = $V_{CC}$ )  | 670             | 800               |                | 660             | 795               |                | 655                   | 790               |                |               |
|             | (OLS = $V_{CC} - 0.4\text{ V}$ )   | 125             | 215               |                | 120             | 210               |                | 120                   | 210               |                |               |
|             | (OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)                                  | 510             | 615               |                | 505             | 610               |                | 500                   | 605               |                |               |
|             | (OLS = $V_{CC} - 1.2\text{ V}$ )   | 0               | 5                 |                | 0               | 0                 |                | 0                     | 5                 |                |               |
|             | (OLS = $V_{EE}$ )  | 325             | 415               |                | 320             | 410               |                | 320                   | 410               |                |               |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)<br>(Note 13) D, $\bar{D}$                    | $V_{EE} + 1275$ | $V_{CC} - 1000^*$ | $V_{CC}$       | $V_{EE} + 1275$ | $V_{CC} - 1000^*$ | $V_{CC}$       | $V_{EE} + 1275$       | $V_{CC} - 1000^*$ | $V_{CC}$       | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)<br>(Note 14) D, $\bar{D}$                     | $V_{EE}$        | $V_{CC} - 1400^*$ | $V_{IH} - 150$ | $V_{EE}$        | $V_{CC} - 1400^*$ | $V_{IH} - 150$ | $V_{EE}$              | $V_{CC} - 1400^*$ | $V_{IH} - 150$ | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration)<br>(Note 12) | 1.2             |                   | 2.5            | 1.2             |                   | 2.5            | 1.2                   |                   | 2.5            | V             |
| $R_{TIN}$   | Internal Input Termination Resistor  | 45              | 50                | 55             | 45              | 50                | 55             | 45                    | 50                | 55             | $\Omega$      |
| $I_{IH}$    | Input HIGH Current (@ $V_{IH}$ )<br>D, $\bar{D}$<br>SEL                        |                 | 30<br>5           | 100<br>50      |                 | 30<br>5           | 100<br>50      |                       | 30<br>5           | 100<br>50      | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current (@ $V_{IL}$ )<br>D, $\bar{D}$<br>SEL                         |                 | 20<br>5           | 100<br>50      |                 | 20<br>5           | 100<br>50      |                       | 20<br>5           | 100<br>50      | $\mu\text{A}$ |

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

10. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.125 V to -0.965 V.

11. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

12.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

13.  $V_{IH}$  cannot exceed  $V_{CC}$ .

14.  $V_{IL}$  always  $\geq V_{EE}$ .

\*Typicals used for testing purposes.

\*\*The device packaged in FCLGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.

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**Table 11. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 15)

| Symbol      | Characteristic  | -40°C                                |                                      |                                      | 25°C                                 |                                      |                                      | 70°C(LGA)/85°C(QFN)***               |                                      |                                      | Unit          |
|-------------|---|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|---------------|
|             |   | Min                                  | Typ                                  | Max                                  | Min                                  | Typ                                  | Max                                  | Min                                  | Typ                                  | Max                                  |               |
| $I_{EE}$    | Negative Power Supply Current   | 23                                   | 30                                   | 39                                   | 23                                   | 30                                   | 39                                   | 23                                   | 30                                   | 39                                   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 16)   | 2260                                 | 2310                                 | 2360                                 | 2290                                 | 2340                                 | 2390                                 | 2315                                 | 2365                                 | 2415                                 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 16)<br>(OLS = $V_{CC}$ )<br>(OLS = $V_{CC} - 0.4\text{ V}$ )<br>(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)<br>(OLS = $V_{CC} - 1.2\text{ V}$ )<br>**(OLS = $V_{EE}$ ) | 1320<br>2030<br>1550<br>2260<br>1785 | 1470<br>2090<br>1670<br>2310<br>1875 | 1620<br>2180<br>1790<br>2390<br>1995 | 1360<br>2065<br>1585<br>2290<br>1820 | 1510<br>2125<br>1705<br>2340<br>1910 | 1660<br>2215<br>1825<br>2420<br>2030 | 1390<br>2090<br>1615<br>2315<br>1850 | 1540<br>2150<br>1735<br>2365<br>1940 | 1690<br>2240<br>1855<br>2445<br>2060 | mV            |
| $V_{OUTPP}$ | Output Amplitude Voltage<br>(OLS = $V_{CC}$ )<br>(OLS = $V_{CC} - 0.4\text{ V}$ )<br>(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)<br>(OLS = $V_{CC} - 1.2\text{ V}$ )<br>**(OLS = $V_{EE}$ )     | 705<br>130<br>535<br>0<br>345        | 815<br>220<br>640<br>0<br>435        |                                      | 695<br>125<br>530<br>0<br>340        | 805<br>215<br>635<br>0<br>430        |                                      | 690<br>125<br>525<br>0<br>335        | 800<br>215<br>630<br>0<br>425        |                                      | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)<br>(Note 18)<br>D, $\bar{D}$  | $V_{EE} + 1275$                      | $V_{CC} - 1000^*$                    | $V_{CC}$                             | $V_{EE} + 1275$                      | $V_{CC} - 1000^*$                    | $V_{CC}$                             | $V_{EE} + 1275$                      | $V_{CC} - 1000^*$                    | $V_{CC}$                             | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)<br>(Note 19)<br>D, $\bar{D}$   | $V_{IH} - 2600$                      | $V_{CC} - 1400^*$                    | $V_{IH} - 150$                       | $V_{IH} - 2600$                      | $V_{CC} - 1400^*$                    | $V_{IH} - 150$                       | $V_{IH} - 2600$                      | $V_{CC} - 1400^*$                    | $V_{IH} - 150$                       | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration)<br>(Note 17)  | 1.2                                  |                                      | 3.3                                  | 1.2                                  |                                      | 3.3                                  | 1.2                                  |                                      | 3.3                                  | V             |
| $R_{TIN}$   | Internal Input Termination Resistor   | 45                                   | 50                                   | 55                                   | 45                                   | 50                                   | 55                                   | 45                                   | 50                                   | 55                                   | $\Omega$      |
| $I_{IH}$    | Input HIGH Current (@ $V_{IH}$ )<br>D, $\bar{D}$<br>SEL   |                                      | 30<br>5                              | 100<br>50                            |                                      | 30<br>5                              | 100<br>50                            |                                      | 30<br>5                              | 100<br>50                            | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current (@ $V_{IL}$ )<br>D, $\bar{D}$<br>SEL  |                                      | 20<br>5                              | 100<br>50                            |                                      | 20<br>5                              | 100<br>50                            |                                      | 20<br>5                              | 100<br>50                            | $\mu\text{A}$ |

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

15. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925 V to -0.165 V.

16. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

17.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

18.  $V_{IH}$  cannot exceed  $V_{CC}$ .

19.  $V_{IL}$  always  $\geq V_{EE}$ .

\*Typicals used for testing purposes.

\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

\*\*\*The device packaged in FCLGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.

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**Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  (Note 20)

| Symbol      | Characteristic  | -40°C  |  |  | 25°C   |  |  | 70°C(LGA)/85°C(QFN)***   |  |  | Unit          |
|-------------|---|--|--|--|--|--|--|--|--|--|---------------|
|             |   | Min  | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Negative Power Supply Current   | 23   | 30   | 39   | 23   | 30   | 39   | 23   | 30   | 39   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 21)   | -1040  | -990   | -940   | -1010  | -960   | -910   | -985   | -935   | -885   | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 21)<br>-3.465 V $\leq$ $V_{EE} \leq$ -3.0 V<br>(OLS = $V_{CC}$ )<br>(OLS = $V_{CC} - 0.4\text{ V}$ )<br>(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)<br>(OLS = $V_{CC} - 1.2\text{ V}$ )<br>**(OLS = $V_{EE}$ )<br>-3.0 V < $V_{EE} \leq$ -2.375 V<br>(OLS = $V_{CC}$ )<br>(OLS = $V_{CC} - 0.4\text{ V}$ )<br>(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)<br>(OLS = $V_{CC} - 1.2\text{ V}$ )<br>(OLS = $V_{EE}$ ) | -1980<br>-1270<br>-1750<br>-1040<br>-1515<br>-1945<br>-1265<br>-1725<br>-1045<br>-1495 | -1830<br>-1210<br>-1630<br>-990<br>-1425<br>-1795<br>-1205<br>-1605<br>-995<br>-1405 | -1680<br>-1120<br>-1510<br>-910<br>-1305<br>-1645<br>-1115<br>-1485<br>-915<br>-1285 | -1940<br>-1235<br>-1715<br>-1010<br>-1480<br>-1905<br>-1230<br>-1690<br>-1010<br>-1460 | -1790<br>-1175<br>-1595<br>-960<br>-1390<br>-1755<br>-1170<br>-1570<br>-960<br>-1370 | -1640<br>-1085<br>-1475<br>-880<br>-1270<br>-1605<br>-1080<br>-1450<br>-880<br>-1250 | -1910<br>-1210<br>-1685<br>-985<br>-1450<br>-1875<br>-1205<br>-1660<br>-990<br>-1435 | -1760<br>-1150<br>-1565<br>-935<br>-1360<br>-1725<br>-1145<br>-1540<br>-940<br>-1345 | -1610<br>-1060<br>-1445<br>-855<br>-1240<br>-1575<br>-1055<br>-1420<br>-860<br>-1225 | mV            |
| $V_{OUTPP}$ | Output Voltage Amplitude<br>-3.465 V $\leq$ $V_{EE} \leq$ -3.0 V<br>(OLS = $V_{CC}$ )<br>(OLS = $V_{CC} - 0.4\text{ V}$ )<br>(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)<br>(OLS = $V_{CC} - 1.2\text{ V}$ )<br>**(OLS = $V_{EE}$ )<br>-3.0 V < $V_{EE} \leq$ -2.375 V<br>(OLS = $V_{CC}$ )<br>(OLS = $V_{CC} - 0.4\text{ V}$ )<br>(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)<br>(OLS = $V_{CC} - 1.2\text{ V}$ )<br>(OLS = $V_{EE}$ )     | 705<br>130<br>535<br>0<br>345<br>670<br>125<br>510<br>0<br>325                         | 815<br>220<br>640<br>0<br>435<br>800<br>215<br>615<br>5<br>415                       |  | 695<br>125<br>530<br>0<br>340<br>660<br>120<br>505<br>0<br>320                         | 805<br>215<br>635<br>0<br>430<br>795<br>210<br>610<br>0<br>410                       |  | 690<br>125<br>525<br>0<br>335<br>655<br>120<br>500<br>0<br>320                       | 800<br>215<br>630<br>0<br>425<br>790<br>210<br>605<br>5<br>410                       |  | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)<br>(Note 23)<br>D, $\bar{D}$  | $V_{EE} + 1275$  | $V_{CC} - 1000^*$  | $V_{CC}$   | $V_{EE} + 1275$  | $V_{CC} - 1000^*$  | $V_{CC}$   | $V_{EE} + 1275$  | $V_{CC} - 1000^*$  | $V_{CC}$   | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)<br>(Note 24)<br>D, $\bar{D}$   | $V_{IH}^- - 2600$  | $V_{CC}^- - 1400^*$  | $V_{IH}^- - 150$   | $V_{IH}^- - 2600$  | $V_{CC}^- - 1400^*$  | $V_{IH}^- - 150$   | $V_{IH}^- - 2600$  | $V_{CC}^- - 1400^*$  | $V_{IH}^- - 150$   | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration)<br>(Note 22)  | $V_{EE} + 1.2$   |  | 0.0  | $V_{EE} + 1.2$   |  | 0.0  | $V_{EE} + 1.2$   |  | 0.0  | V             |
| $R_{TIN}$   | Internal Input Termination Resistor   | 45   | 50   | 55   | 45   | 50   | 55   | 45   | 50   | 55   | $\Omega$      |
| $I_{IH}$    | Input HIGH Current (@ $V_{IH}$ )<br>D, $\bar{D}$<br>SEL   |  | 30<br>5  | 100<br>50  |  | 30<br>5  | 100<br>50  |  | 30<br>5  | 100<br>50  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current (@ $V_{IL}$ )<br>D, $\bar{D}$<br>SEL  |  | 20<br>5  | 100<br>50  |  | 20<br>5  | 100<br>50  |  | 20<br>5  | 100<br>50  | $\mu\text{A}$ |

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

20. Input and output parameters vary 1:1 with  $V_{CC}$ .

21. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

22.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

23.  $V_{IH}$  cannot exceed  $V_{CC}$ .

24.  $V_{IL}$  always  $\geq V_{EE}$ .

\*Typicals used for testing purposes.

\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

\*\*\*The device packaged in FCLGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.



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**Table 13. AC CHARACTERISTICS for FCLGA-16**

$V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V}$  to  $3.465\text{ V}$ ;  $V_{EE} = 0\text{ V}$

| Symbol                   | Characteristic   | -40°C |     |      | 25°C |     |      | 70°C |     |      | Unit |
|--------------------------|--|-------|-----|------|------|-----|------|------|-----|------|------|
|                          |  | Min   | Typ | Max  | Min  | Typ | Max  | Min  | Typ | Max  |      |
| $f_{max}$                | Maximum Frequency<br>(See Figure 8) (Note 25)  | 7     | 8   |      | 7    | 8   |      | 7    | 8   |      | GHz  |
| $V_{OUTPP}$              | Output Voltage Amplitude<br>(OLS = $V_{CC}$ ) $f_{in} \leq 7\text{ GHz}$   | 550   | 740 |      | 500  | 720 |      | 450  | 700 |      | mV   |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to Output Differential<br>D/SEL → Q  | 110   | 160 | 210  | 115  | 165 | 215  | 120  | 170 | 220  | ps   |
| $t_{SKEW}$               | Duty Cycle Skew (Note 26)  |       | 5   | 15   |      | 5   | 15   |      | 5   | 15   | ps   |
| $t_{SKEW}$               | Channel Skew Q → D/SEL   |       | 5   | 20   |      | 5   | 20   |      | 5   | 20   | ps   |
| $t_{JITTER}$             | RMS Random Clock Jitter<br>(See Figure 8) (Note 25)<br>$f_{in} \leq 7\text{ GHz}$<br>Peak-to-Peak Data Dependent Jitter<br>$f_{in} \leq 7\text{ Gb/s}$ |       | 0.5 | 1.5  |      | 0.5 | 1.5  |      | 0.5 | 1.5  | ps   |
| $V_{INPP}$               | Input Voltage Swing/Sensitivity<br>(Differential Configuration) (Note 27)  | 75    |     | 2600 | 75   |     | 2600 | 75   |     | 2600 | mV   |
| $t_r$<br>$t_f$           | Output Rise/Fall Times (20% - 80%)<br>(Q, $\bar{Q}$ )<br>@ 1 GHz   | 20    | 40  | 65   | 20   | 40  | 65   | 20   | 40  | 65   | ps   |

25. Measured using a 500 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ . Input edge rates 40 ps (20% - 80%).

26.  $t_{SKEW} = |t_{PLH} - t_{PHL}|$  for a nominal 50% differential clock input waveform. See Figure 12.

27.  $V_{INPP}$  (max) cannot exceed  $V_{CC} - V_{EE}$ .

**Table 14. AC CHARACTERISTICS for QFN-16**

$V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V}$  to  $3.465\text{ V}$ ;  $V_{EE} = 0\text{ V}$

| Symbol                   | Characteristic  | -40°C    |          |          | 25°C     |          |          | 85°C     |          |          | Unit     |
|--------------------------|---|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
|                          |   | Min      | Typ      | Max      | Min      | Typ      | Max      | Min      | Typ      | Max      |          |
| $f_{max}$                | Maximum Frequency<br>(See Figure 8) (Note 28)   | 7        | 8        |          | 7        | 8        |          | 7        | 8        |          | GHz      |
| $V_{OUTPP}$              | Output Voltage Amplitude<br>(OLS = $V_{CC}$ ) $f_{in} \leq 7\text{ GHz}$<br>$f_{in} = 8\text{ GHz}$   | 590      | 730      |          | 470      | 720      |          | 540      | 700      |          | mV<br>mV |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to Output Differential<br>D/SEL → Q   | 110      | 160      | 210      | 115      | 165      | 215      | 120      | 170      | 220      | ps       |
| $t_{SKEW}$               | Duty Cycle Skew (Note 29)   |          | 5        | 15       |          | 5        | 15       |          | 5        | 15       | ps       |
| $t_{SKEW}$               | Channel Skew Q → D/SEL  |          | 5        | 20       |          | 5        | 20       |          | 5        | 20       | ps       |
| $t_{JITTER}$             | RMS Random Clock Jitter<br>(See Figure 8) (Note 31)<br>$f_{in} \leq 7\text{ GHz}$<br>Peak-to-Peak Data Dependent Jitter<br>(Note 32)<br>$f_{in} \leq 7\text{ Gb/s}$ |          | 0.5      | 1.5      |          | 0.5      | 1.5      |          | 0.5      | 1.5      | ps       |
| $V_{INPP}$               | Input Voltage Swing/Sensitivity<br>(Differential Configuration) (Note 30)   | 75       |          | 2600     | 75       |          | 2600     | 75       |          | 2600     | mV       |
| $t_r$<br>$t_f$           | Output Rise/Fall Times (20% - 80%)<br>(Q, $\bar{Q}$ )<br>@ 1 GHz  | 30<br>17 | 45<br>35 | 60<br>65 | 30<br>17 | 45<br>35 | 60<br>65 | 30<br>17 | 45<br>35 | 60<br>65 | ps       |

28. Measured using a 500 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ . Input edge rates 40 ps (20% - 80%).

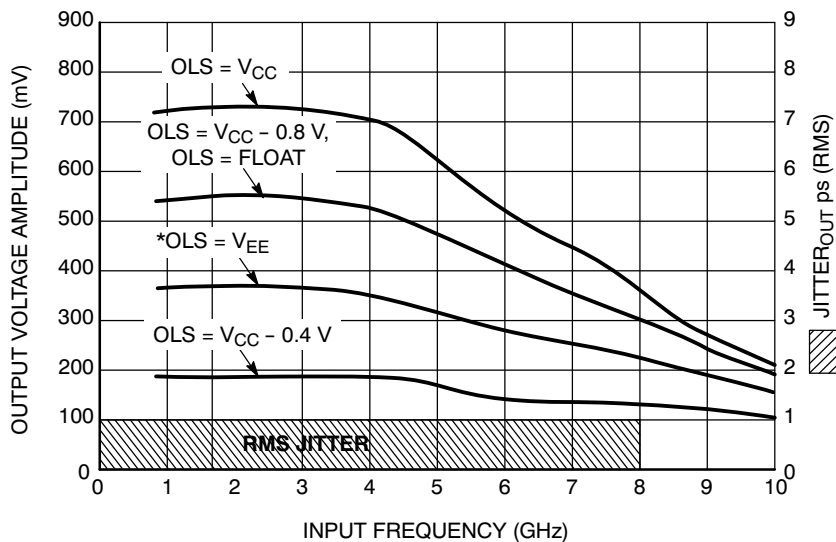
29.  $t_{SKEW} = |t_{PLH} - t_{PHL}|$  for a nominal 50% differential clock input waveform. See Figure 12.

30.  $V_{INPP}$  (max) cannot exceed  $V_{CC} - V_{EE}$ .

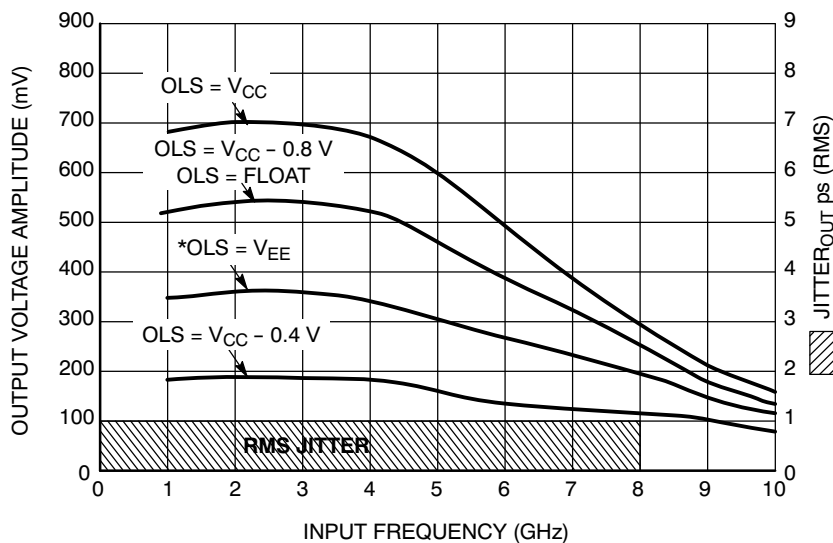
31. Additive RMS jitter with 50% duty cycle clock signal at 7 GHz.

32. Additive Peak-to-Peak data dependent jitter with NRZ PRBS  $2^{31}-1$  data rate at 7 Gb/s.

# NBSG86A



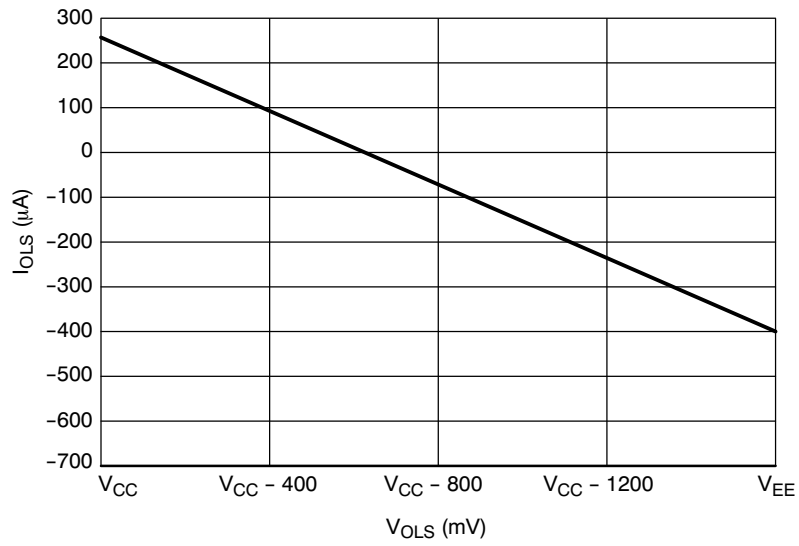
**Figure 8. Output Voltage Amplitude ( $V_{OUTPP}$ ) / RMS Jitter vs. Input Frequency ( $f_{in}$ ) for 2:1 MUX Mode ( $V_{CC} - V_{EE} = 2.5\text{ V}$  @  $25^\circ\text{C}$ ; Repetitive 1010 Input Data Pattern)**



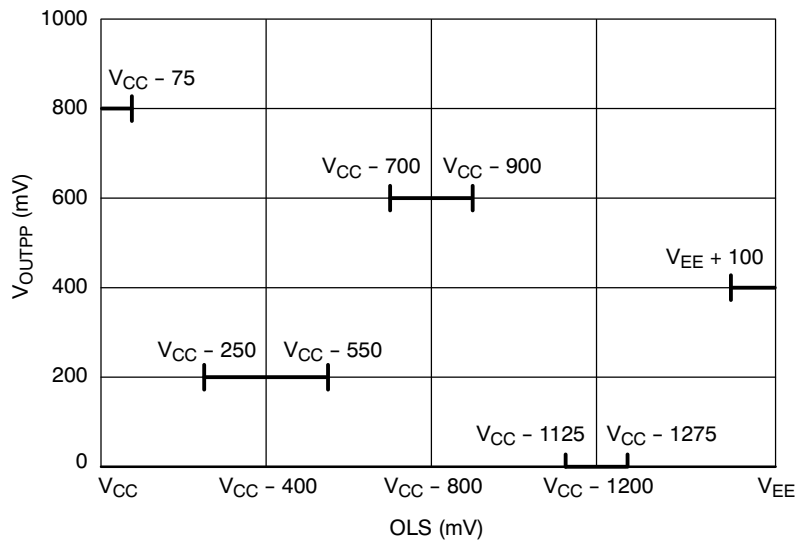
**Figure 9. Output Voltage Amplitude ( $V_{OUTPP}$ ) / RMS Jitter vs. Input Frequency ( $f_{in}$ ) for 2:1 MUX Mode ( $V_{CC} - V_{EE} = 3.3\text{ V}$  @  $25^\circ\text{C}$ ; Repetitive 1010 Input Data Pattern)**

\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a  $2\text{ k}\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

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**Figure 10. Typical OLS Input Current vs. OLS Input Voltage**  
( $V_{CC} - V_{EE} = 3.3 V @ 25^{\circ}C$ )



**Figure 11. OLS Operating Area**

## NBSG86A

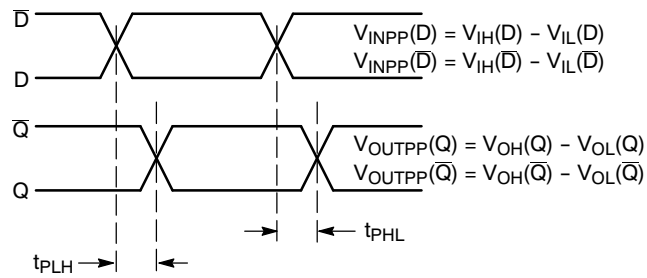


Figure 12. AC Reference Measurement

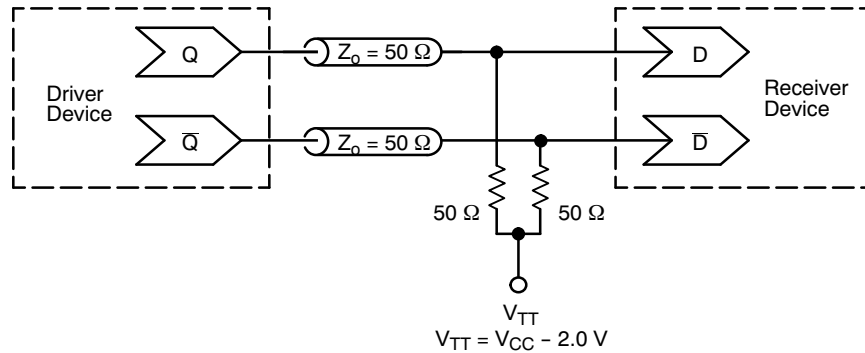


Figure 13. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

| Device        | Package Type                  | Shipping <sup>†</sup>                            |
|---------------|-------------------------------|--|
| NBSG86ABA     | 4x4 mm<br>FCBGA-16            | 100 Units / Tray (Contact Sales Representative)  |
| NBSG86ABAR2   | 4x4 mm<br>FCBGA-16            | 100 / Tape & Reel (Contact Sales Representative) |
| NBSG86AMAG    | FCLGA-16, 4x4 mm<br>(Pb-Free) | 100 Units / Tray (Contact Sales Representative)  |
| NBSG86AMAHTBG | FCLGA-16, 4x4 mm<br>(Pb-Free) | 100 / Tape & Reel                                |
| NBSG86AMN     | 3x3 mm<br>QFN-16              | 123 Units / Rail                                 |
| NBSG86AMNG    | 3x3 mm<br>QFN-16<br>(Pb-Free) | 123 Units / Rail                                 |
| NBSG86AMNR2G  | 3x3 mm<br>QFN-16<br>(Pb-Free) | 3000 / Tape & Reel                               |

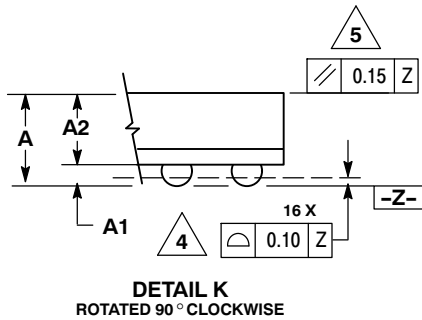
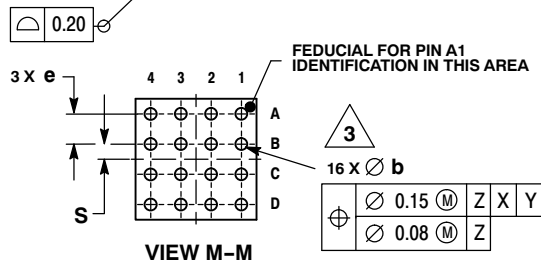
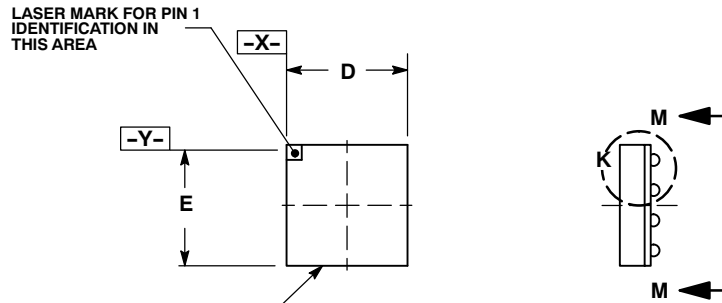
| Board        | Description                |
|--------------|----------------------------|
| NBSG86ABAEVB | NBSG86ABA Evaluation Board |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NBSG86A

## PACKAGE DIMENSIONS

FCBGA-16  
 BA SUFFIX  
 PLASTIC 4 X 4 (mm) BGA FLIP CHIP PACKAGE  
 CASE 489-01  
 ISSUE O



### NOTES:

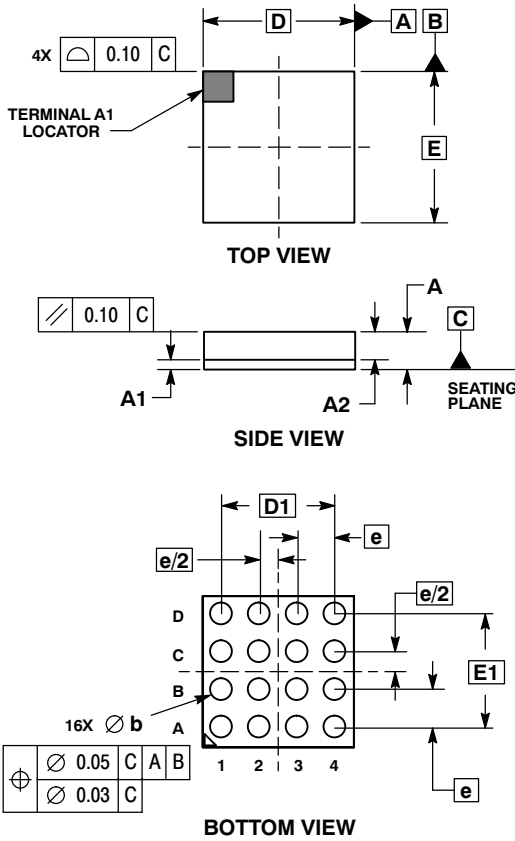
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 1.40        | MAX  |
| A1  | 0.25        | 0.35 |
| A2  | 1.20        | REF  |
| b   | 0.30        | 0.50 |
| D   | 4.00        | BSC  |
| E   | 4.00        | BSC  |
| e   | 1.00        | BSC  |
| S   | 0.50        | BSC  |

# NBSG86A

## PACKAGE DIMENSIONS

16 PIN LGA 4x4, 1.0P  
CASE 526AB-01  
ISSUE C

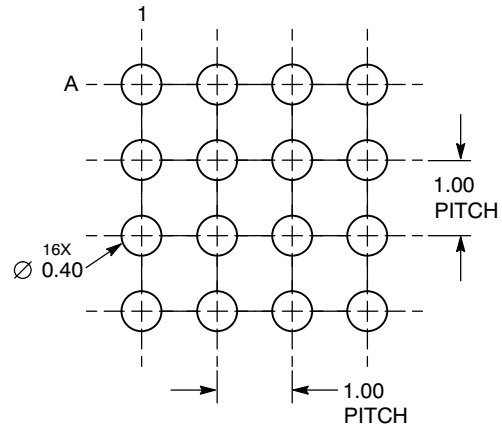


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

| MILLIMETERS |          |      |      |
|-------------|----------|------|------|
| DIM         | MIN      | TYP  | MAX  |
| A           | 0.89     | 0.96 | 1.03 |
| A1          | 0.22     | 0.26 | 0.30 |
| A2          | 0.67     | 0.70 | 0.73 |
| b           | 0.30     | 0.40 | 0.50 |
| D           | 4.00 BSC |      |      |
| D1          | 3.00 BSC |      |      |
| E           | 4.00 BSC |      |      |
| E1          | 3.00 BSC |      |      |
| e           | 1.00 BSC |      |      |

### SOLDERING FOOTPRINT\*

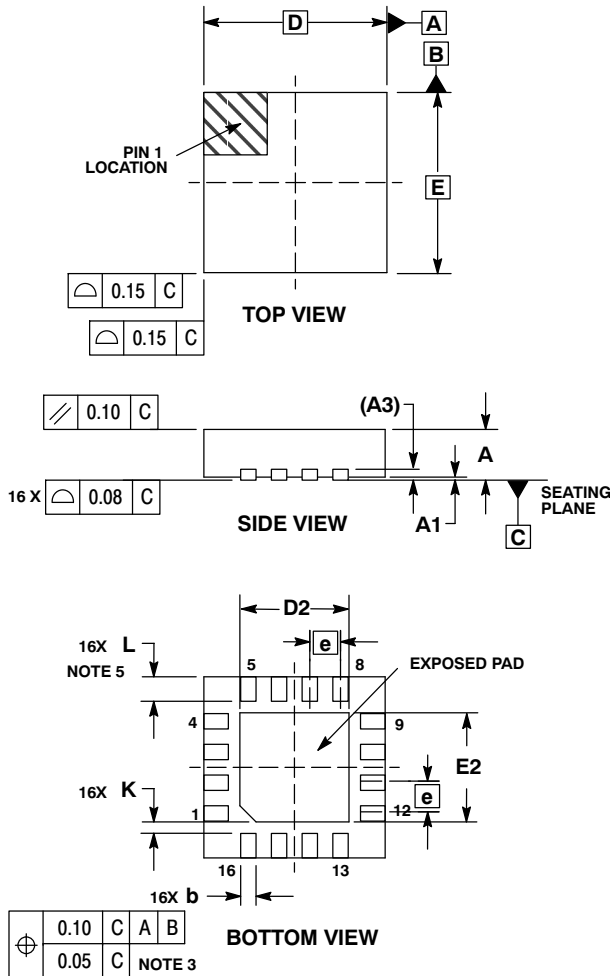


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NBSG86A

## PACKAGE DIMENSIONS

16 PIN QFN  
CASE 485G-01  
ISSUE C

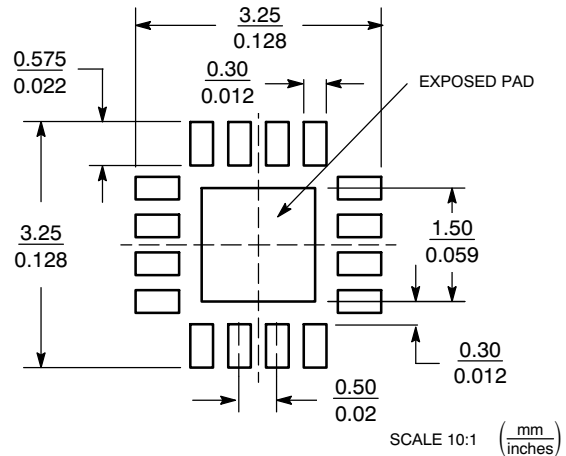


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L<sub>max</sub> CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| MILLIMETERS |          |      |
|-------------|----------|------|
| DIM         | MIN      | MAX  |
| A           | 0.80     | 1.00 |
| A1          | 0.00     | 0.05 |
| A3          | 0.20 REF |      |
| b           | 0.18     | 0.30 |
| D           | 3.00 BSC |      |
| D2          | 1.65     | 1.85 |
| E           | 3.00 BSC |      |
| E2          | 1.65     | 1.85 |
| e           | 0.50 BSC |      |
| K           | 0.18 TYP |      |
| L           | 0.30     | 0.50 |

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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