FAIRCHILD SEMICONDUCTOR™

October 2001
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# NC7SP57 • NC7SP58
# TinyLogic® ULP Universal Configurable 2-Input Logic Gates

## General Description

The NC7SP57 and the NC7SP58 are Universal Configurable 2-Input Logic Gates from Fairchild's Ultra Low Power (ULP) Series of TinyLogic®. Ideal for applications where battery life is critical, this product is designed for ultra low power consumption within the $V_{CC}$ operating range of 0.9V to 3.6V. Each device is capable of being configured for 1 of 5 unique 2-input logic functions. Any possible 2-input combinatorial logic function can be implemented as shown in the Function Selection Table. Device functionality is selected by how the device is wired at the board level. Figure 1 through Figure 10 illustrate how to connect the NC7SP57 and NC7SP58 respectively for the desired logic function. All inputs have been implemented with hysteresis.

The internal circuit is composed of a minimum of inverter stages including the output buffer, to enable ultra low dynamic power.

The NC7SP57 and NC7SP58, for lower drive requirements, are uniquely designed for optimized power and speed, and are fabricated with an advanced CMOS technology to achieve best in class operation while maintaining extremely low CMOS power dissipation.

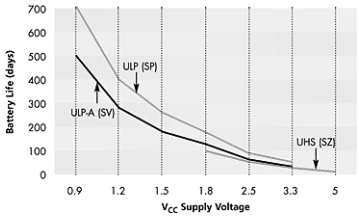
## Features

- 0.9V to 3.6V $V_{CC}$ supply operation
- 3.6V overvoltage tolerant I/O's at $V_{CC}$ from 0.9V to 3.6V
- $t_{PD}$
  - 5 ns typ for 3.0V to 3.6V $V_{CC}$
  - 6 ns typ for 2.3V to 2.7V $V_{CC}$
  - 8 ns typ for 1.65V to 1.95V $V_{CC}$
  - 10 ns typ for 1.40V to 1.60V $V_{CC}$
  - 14 ns typ for 1.10V to 1.30V $V_{CC}$
  - 40 ns typ for 0.90V $V_{CC}$
- Power-Off high impedance inputs and outputs
- Static Drive ($I_{OH}/I_{OL}$)
  - ±2.6 mA @ 3.00V $V_{CC}$
  - ±2.1 mA @ 2.30V $V_{CC}$
  - ±1.5 mA @ 1.65V $V_{CC}$
  - ±1.0 mA @ 1.40V $V_{CC}$
  - ±0.5 mA @ 1.10V $V_{CC}$
  - ±20 μA @ 0.9V $V_{CC}$
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Ultra small MicroPak™ leadfree package
- Ultra low dynamic power

## Ordering Code:

| Order Number | Package Number | Product Code Top Mark | Package Description | Supplied As |
|---|---|---|---|---|
| NC7SP57P6X | MAA06A | P57 | 6-Lead SC70, EIAJ SC88, 1.25mm Wide | 3k Units on Tape and Reel |
| NC7SP57L6X | MAC06A | K9 | 6-Lead MicroPak, 1.0mm Wide | 5k Units on Tape and Reel |
| NC7SP58P6X | MAA06A | P58 | 6-Lead SC70, EIAJ SC88, 1.25mm Wide | 3k Units on Tape and Reel |
| NC7SP58L6X | MAC06A | L3 | 6-Lead MicroPak, 1.0mm Wide | 5k Units on Tape and Reel |

## Battery Life vs. $V_{CC}$ Supply Voltage




TinyLogic ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly.

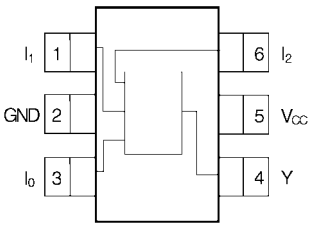
Battery Life = $(V_{battery} * I_{battery} * .9)/(P_{device})/24hrs/day$

Where, $P_{device} = (I_{CC} * V_{CC}) + (C_{PD} + C_L) * V_{CC}^2 * f$

Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with $C_L$ = 15 pF load

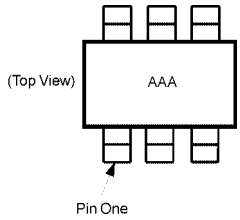
## Connection Diagrams

**Pin Assignments for SC70**




**(Top View)**
**NC7SP57 and NC7SP58**

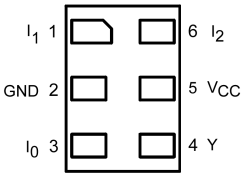
**Pin One Orientation Diagram**




AAA = Product Code Top Mark - see ordering code

**Note:** Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

**Pad Assignments for MicroPak**




**(Top Thru View)**

## Pin Descriptions

| Pin Name | Description |
|---|---|
| $I_0$, $I_1$, $I_2$ | Data Input |
| Y | Output |

## Function Table

| Input | | | NC7SP57 | NC7SP58 |
|---|---|---|---|---|
| $I_2$ | $I_1$ | $I_0$ | $Y = \overline{(I_0)} \cdot \overline{(I_2)} + (I_1) \cdot (I_2)$ | $Y = \overline{(I_0)} \cdot \overline{(I_2)} + \overline{(I_1)} \cdot (I_2)$ |
| L | L | L | H | L |
| L | L | H | L | H |
| L | H | L | H | L |
| L | H | H | L | H |
| H | L | L | L | H |
| H | L | H | L | H |
| H | H | L | H | L |
| H | H | H | H | L |

H = HIGH Logic Level  L = LOW Logic Level

## Function Selection Table

| 2-Input Logic Function | Device Selection | Connection Configuration |
|---|---|---|
| 2-Input AND | NC7SP57 | Figure 1 |
| 2-Input AND with inverted input | NC7SP58 | Figures 7, 8 |
| 2-Input AND with both inputs inverted | NC7SP57 | Figure 4 |
| 2-Input NAND | NC7SP58 | Figure 6 |
| 2-Input NAND with inverted input | NC7SP57 | Figures 2, 3 |
| 2-Input NAND with both inputs inverted | NC7SP58 | Figure 9 |
| 2-Input OR | NC7SP58 | Figure 9 |
| 2-Input OR with inverted input | NC7SP57 | Figures 2, 3 |
| 2-Input OR with both inputs inverted | NC7SP58 | Figure 6 |
| 2-Input NOR | NC7SP57 | Figure 4 |
| 2-Input NOR with inverted input | NC7SP58 | Figures 7, 8 |
| 2-Input NOR with both inputs inverted | NC7SP57 | Figure 1 |
| 2-Input XOR | NC7SP58 | Figure 10 |
| 2-Input XNOR | NC7SP57 | Figure 5 |

## Logic Configurations NC7SP57

Figure 1 through Figure 5 show the logical functions that can be implemented using the NC7SP57. The diagrams show the DeMorgan's equivalent logic duals for a given 2-input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

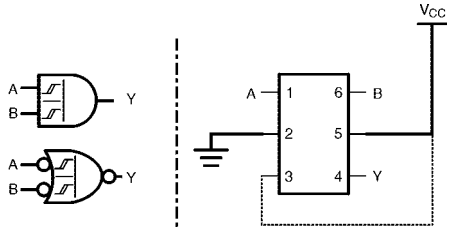



**FIGURE 1. 2-Input AND Gate**

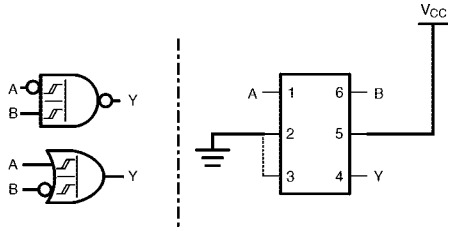



**FIGURE 2. 2-Input NAND with Inverted A Input**

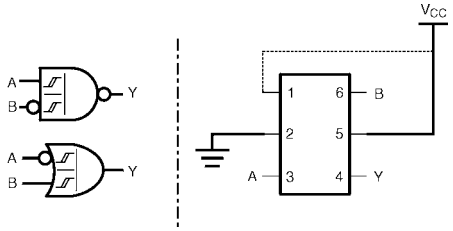



**FIGURE 3. 2-Input NAND with Inverted B Input**

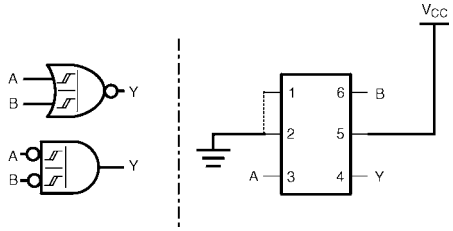



**FIGURE 4. 2-Input NOR Gate**

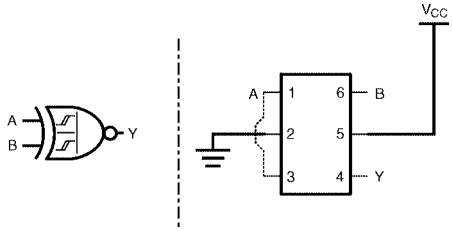



**FIGURE 5. 2-Input XNOR Gate**

## Logic Configurations NC7SP58

Figure 6 through Figure 10 show the logical functions that can be implemented using the NC7SP58. The diagrams show the DeMorgan's equivalent logic duals for a given 2-input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

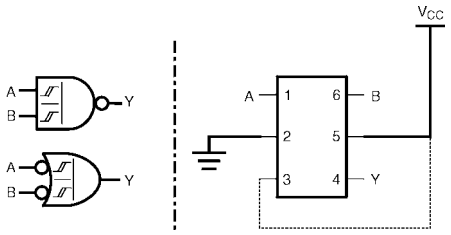



**FIGURE 6. 2-Input NAND Gate**

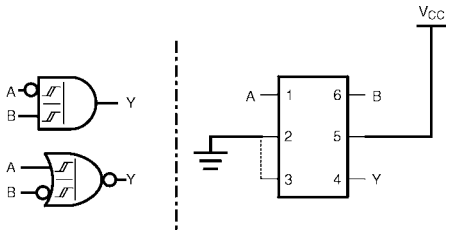



**FIGURE 7. 2-Input AND with Inverted A Input**

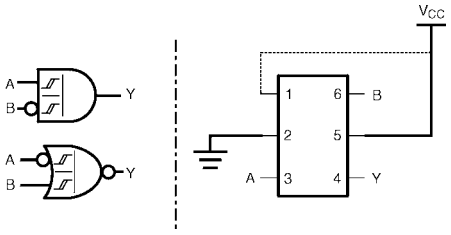



**FIGURE 8. 2-Input AND with Inverted B Input**

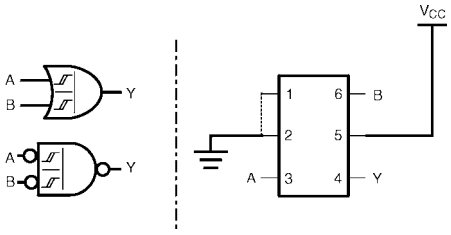



**FIGURE 9. 2-Input OR Gate**

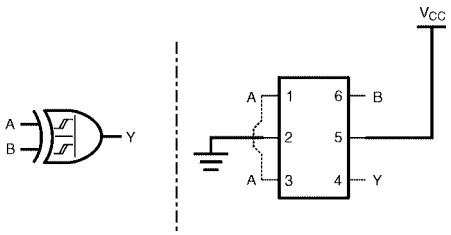



**FIGURE 10. 2-Input XOR Gate**

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +4.6V |
| DC Input Voltage ($V_{IN}$) | −0.5V to +4.6V |
| DC Output Voltage ($V_{OUT}$) | |
| HIGH or LOW State (Note 2) | −0.5V to $V_{CC}$ +0.5V |
| $V_{CC}$ = 0V | −0.5V to 4.6V |
| DC Input Diode Current ($I_{IK}$) $V_{IN}$ < 0V | ±50 mA |
| DC Output Diode Current ($I_{OK}$) | |
| $V_{OUT}$ < 0V | −50 mA |
| $V_{OUT}$ > $V_{CC}$ | +50 mA |
| DC Output Source/Sink Current ($I_{OH}/I_{OL}$) | ± 50 mA |
| DC $V_{CC}$ or Ground Current per | |
| Supply Pin ($I_{CC}$ or Ground) | ± 50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |

## Recommended Operating Conditions (Note 3)

| | |
|---|---|
| Supply Voltage | 0.9V to 3.6V |
| Input Voltage ($V_{IN}$) | 0V to 3.6V |
| Output Voltage ($V_{OUT}$) | |
| HIGH or LOW State | 0V to $V_{CC}$ |
| $V_{CC}$ = 0V | 0V to 3.6V |
| Output Current in $I_{OH}/I_{OL}$ | |
| $V_{CC}$ = 3.0V to 3.6V | ±2.6 mA |
| $V_{CC}$ = 2.3V to 2.7V | ± 2.1 mA |
| $V_{CC}$ = 1.65V to 1.95V | ± 1.5 mA |
| $V_{CC}$ = 1.40V to 1.60V | ± 1 mA |
| $V_{CC}$ = 1.10V to 1.30V | ±0.5 mA |
| $V_{CC}$ = 0.9V | ±20 µA |
| Free Air Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate ($\Delta t/\Delta V$) | |
| $V_{IN}$ = 0.8V to 2.0V, $V_{CC}$ = 3.0V | 10 ns/V |

**Note 1:** Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** $I_O$ Absolute Maximum Rating must be observed.

**Note 3:** Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C | | $T_A$ = −40°C to +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | |
| $V_P$ | Positive Threshold Voltage | 0.90 | 0.3 | 0.6 | 0.3 | 0.6 | V | |
| | | 1.10 | 0.4 | 1.0 | 0.4 | 1.0 | | |
| | | 1.40 | 0.5 | 1.2 | 0.5 | 1.2 | | |
| | | 1.65 | 0.7 | 1.5 | 0.7 | 1.5 | | |
| | | 2.30 | 1.0 | 1.9 | 1.0 | 1.9 | | |
| | | 3.0 | 1.5 | 2.6 | 1.5 | 2.6 | | |
| $V_N$ | Negative Threshold Voltage | 0.90 | 0.10 | 0.6 | 0.10 | 0.6 | V | |
| | | 1.10 | 0.15 | 0.7 | 0.15 | 0.7 | | |
| | | 1.40 | 0.20 | 0.8 | 0.20 | 0.8 | | |
| | | 1.65 | 0.25 | 0.9 | 0.25 | 0.9 | | |
| | | 2.30 | 0.4 | 1.15 | 0.4 | 1.15 | | |
| | | 3.0 | 0.6 | 1.5 | 0.6 | 1.5 | | |
| $V_H$ | Hysteresis Voltage | 0.90 | 0.07 | 0.5 | 0.07 | 0.5 | V | |
| | | 1.10 | 0.08 | 0.6 | 0.08 | 0.6 | | |
| | | 1.40 | 0.09 | 0.8 | 0.09 | 0.8 | | |
| | | 1.65 | 0.10 | 1.0 | 0.10 | 1.0 | | |
| | | 2.30 | 0.25 | 1.1 | 0.25 | 1.1 | | |
| | | 3.0 | 0.60 | 1.8 | 0.60 | 1.8 | | |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ Min | $T_A = +25°C$ Max | $T_A = -40°C$ to $+85°C$ Min | $T_A = -40°C$ to $+85°C$ Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH Level Output Voltage | 0.90 | $V_{CC}$ – 0.1 | | $V_{CC}$ – 0.1 | | V | $I_{OH}$ = –20 μA |
| | | 1.10 ≤ $V_{CC}$ ≤ 1.30 | $V_{CC}$ – 0.1 | | $V_{CC}$ – 0.1 | | | |
| | | 1.40 ≤ $V_{CC}$ ≤ 1.60 | $V_{CC}$ – 0.1 | | $V_{CC}$ – 0.1 | | | |
| | | 1.65 ≤ $V_{CC}$ ≤ 1.95 | $V_{CC}$ – 0.1 | | $V_{CC}$ – 0.1 | | | |
| | | 2.30 ≤ $V_{CC}$ ≤ 2.70 | $V_{CC}$ – 0.1 | | $V_{CC}$ – 0.1 | | | |
| | | 3.00 ≤ $V_{CC}$ ≤ 3.60 | $V_{CC}$ – 0.1 | | $V_{CC}$ – 0.1 | | | |
| | | 1.10 ≤ $V_{CC}$ ≤ 1.30 | 0.75 x $V_{CC}$ | | 0.70 x $V_{CC}$ | | | $I_{OH}$ = –0.5 mA |
| | | 1.40 ≤ $V_{CC}$ ≤ 1.60 | 1.07 | | 0.99 | | | $I_{OH}$ = –1 mA |
| | | 1.65 ≤ $V_{CC}$ ≤ 1.95 | 1.24 | | 1.22 | | | $I_{OH}$ = –1.5 mA |
| | | 2.30 ≤ $V_{CC}$ ≤ 2.70 | 1.95 | | 1.87 | | | $I_{OH}$ = –2.1 mA |
| | | 3.00 ≤ $V_{CC}$ ≤ 3.60 | 2.61 | | 2.55 | | | $I_{OH}$ = –2.6 mA |
| $V_{OL}$ | LOW Level Output Voltage | 0.90 | | 0.1 | | 0.1 | V | $I_{OL}$ = 20 μA |
| | | 1.10 ≤ $V_{CC}$ ≤ 1.30 | | 0.1 | | 0.1 | | |
| | | 1.40 ≤ $V_{CC}$ ≤ 1.60 | | 0.1 | | 0.1 | | |
| | | 1.65 ≤ $V_{CC}$ ≤ 1.95 | | 0.1 | | 0.1 | | |
| | | 2.30 ≤ $V_{CC}$ ≤ 2.70 | | 0.1 | | 0.1 | | |
| | | 3.00 ≤ $V_{CC}$ ≤ 3.60 | | 0.1 | | 0.1 | | |
| | | 1.10 ≤ $V_{CC}$ ≤ 1.30 | | 0.30 x $V_{CC}$ | | 0.30 x $V_{CC}$ | | $I_{OL}$ = 0.5 mA |
| | | 1.40 ≤ $V_{CC}$ ≤ 1.60 | | 0.31 | | 0.37 | | $I_{OL}$ = 1 mA |
| | | 1.65 ≤ $V_{CC}$ ≤ 1.95 | | 0.31 | | 0.35 | | $I_{OL}$ = 1.5 mA |
| | | 2.30 ≤ $V_{CC}$ ≤ 2.70 | | 0.31 | | 0.33 | | $I_{OL}$ = 2.1 mA |
| | | 3.00 ≤ $V_{CC}$ ≤ 3.60 | | 0.31 | | 0.33 | | $I_{OL}$ = 2.6 mA |
| $I_{IN}$ | Input Leakage Current | 0.90 to 3.60 | | ±0.1 | | ±0.5 | μA | 0 ≤ $V_I$ ≤ 3.6V |
| $I_{OFF}$ | Power Off Leakage Current | 0 | | 0.5 | | 0.5 | μA | 0 ≤ ($V_I$, $V_O$) ≤ 3.6V |
| $I_{CC}$ | Quiescent Supply Current | 0.90 to 3.60 | | 0.5 | | 0.9 | μA | $V_I$ = $V_{CC}$ or GND |

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ Min | $T_A = +25°C$ Typ | $T_A = +25°C$ Max | $T_A = -40°C$ to $+85°C$ Min | $T_A = -40°C$ to $+85°C$ Max | Units | Conditions | Figure Number |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay | 0.90 | | 40 | | | | ns | $C_L$ = 10 pF, $R_L$ = 1 MΩ | Figures 11, 12 |
| | | 1.10 ≤ $V_{CC}$ ≤ 1.30 | 5.5 | 14 | 28.0 | 5.0 | 51.0 | | | |
| | | 1.40 ≤ $V_{CC}$ ≤ 1.60 | 4.5 | 10 | 17.0 | 4.0 | 21.0 | | | |
| | | 1.65 ≤ $V_{CC}$ ≤ 1.95 | 3.5 | 8 | 14.0 | 3.0 | 17.0 | | | |
| | | 2.30 ≤ $V_{CC}$ ≤ 2.70 | 2.5 | 6 | 10.0 | 2.0 | 13.0 | | | |
| | | 3.00 ≤ $V_{CC}$ ≤ 3.60 | 1.5 | 5 | 8.0 | 1.0 | 12.0 | | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay | 0.90 | | 41 | | | | ns | $C_L$ = 15 pF, $R_L$ = 1 MΩ | Figures 11, 12 |
| | | 1.10 ≤ $V_{CC}$ ≤ 1.30 | 6.5 | 15 | 29.0 | 6.0 | 52.0 | | | |
| | | 1.40 ≤ $V_{CC}$ ≤ 1.60 | 5.0 | 10 | 18.0 | 4.5 | 22.0 | | | |
| | | 1.65 ≤ $V_{CC}$ ≤ 1.95 | 4.0 | 8 | 15.0 | 3.5 | 18.0 | | | |
| | | 2.30 ≤ $V_{CC}$ ≤ 2.70 | 3.0 | 6 | 11.0 | 2.5 | 14.0 | | | |
| | | 3.00 ≤ $V_{CC}$ ≤ 3.60 | 2.0 | 5 | 9.0 | 1.5 | 12.0 | | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay | 0.90 | | 46 | | | | ns | $C_L$ = 30 pF, $R_L$ = 1 MΩ | Figures 11, 12 |
| | | 1.10 ≤ $V_{CC}$ ≤ 1.30 | 7.0 | 17 | 32.0 | 6.5 | 55.0 | | | |
| | | 1.40 ≤ $V_{CC}$ ≤ 1.60 | 5.5 | 11 | 20.0 | 5.0 | 24.0 | | | |
| | | 1.65 ≤ $V_{CC}$ ≤ 1.95 | 4.5 | 9 | 17.0 | 4.0 | 20.0 | | | |
| | | 2.30 ≤ $V_{CC}$ ≤ 2.70 | 3.5 | 7 | 12.0 | 3.0 | 15.0 | | | |
| | | 3.00 ≤ $V_{CC}$ ≤ 3.60 | 2.5 | 6 | 11.0 | 2.0 | 14.0 | | | |
| $C_{IN}$ | Input Capacitance | 0 | | 2.0 | | | | pF | | |
| $C_{OUT}$ | Output Capacitance | 0 | | 4.0 | | | | pF | | |
| $C_{PD}$ | Power Dissipation Capacitance | 0.9 to 3.60 | | 8 | | | | pF | $V_I$ = 0V or $V_{CC}$, f = 10 MHz | |

## AC Loading and Waveforms

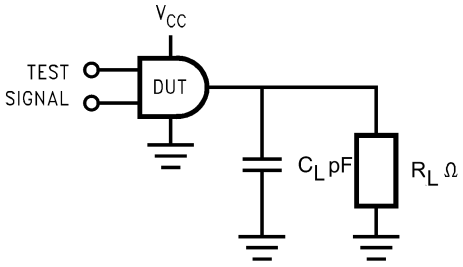



**FIGURE 11. AC Test Circuit**

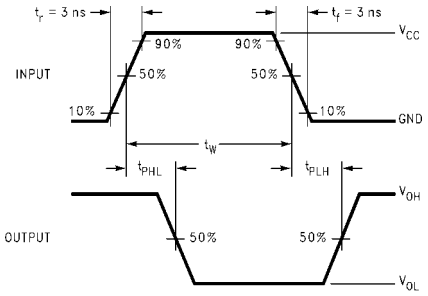



**FIGURE 12. AC Waveforms**

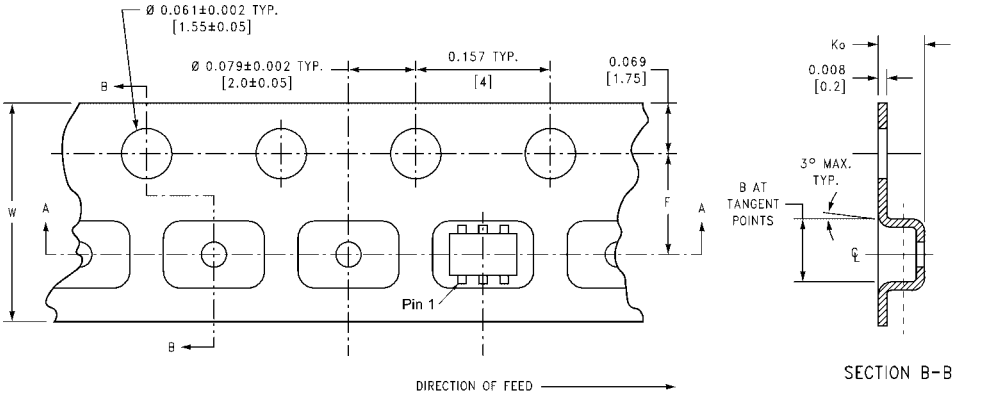
| Symbol | $V_{CC}$ | | | | | |
|---|---|---|---|---|---|---|
| | **3.3V ± 0.3V** | **2.5V ± 0.2V** | **1.8V ± 0.15V** | **1.5V ± 0.10V** | **1.2V ± 0.10V** | **0.9V** |
| $V_{mi}$ | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_{mo}$ | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |

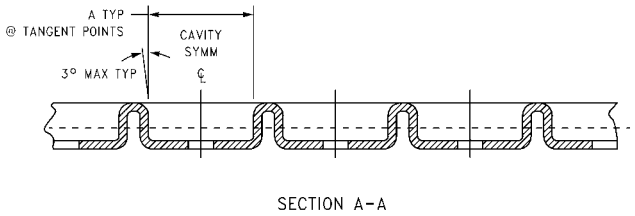
## Tape and Reel Specification

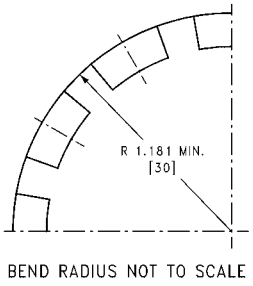
**TAPE FORMAT for SC70**

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|---|---|---|---|---|
| P6X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

**TAPE DIMENSIONS** inches (millimeters)



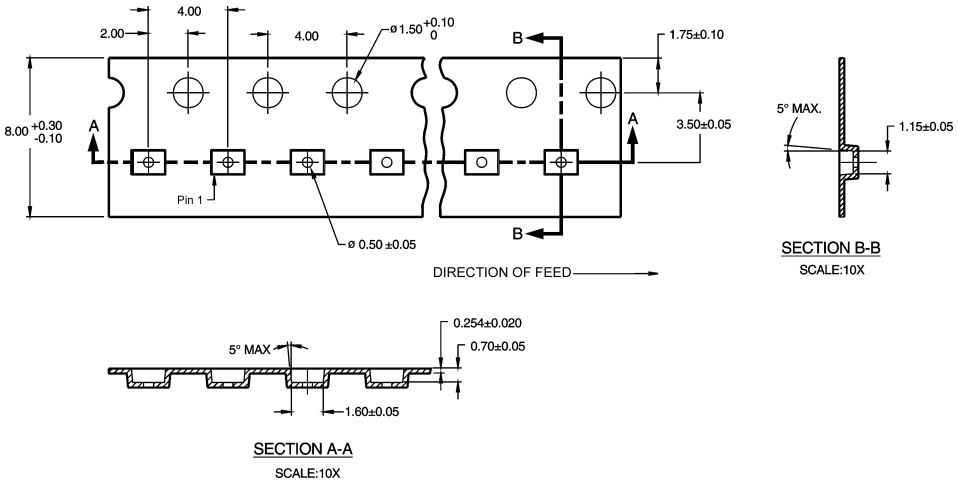




| Package | Tape Size | DIM A | DIM B | DIM F | DIM $K_o$ | DIM P1 | DIM W |
|---|---|---|---|---|---|---|---|
| SC70-6 | 8 mm | 0.093<br>(2.35) | 0.096<br>(2.45) | 0.138 ± 0.004<br>(3.5 ± 0.10) | 0.053 ± 0.004<br>(1.35 ± 0.10) | 0.157<br>(4) | 0.315 ± 0.004<br>(8 ± 0.1) |

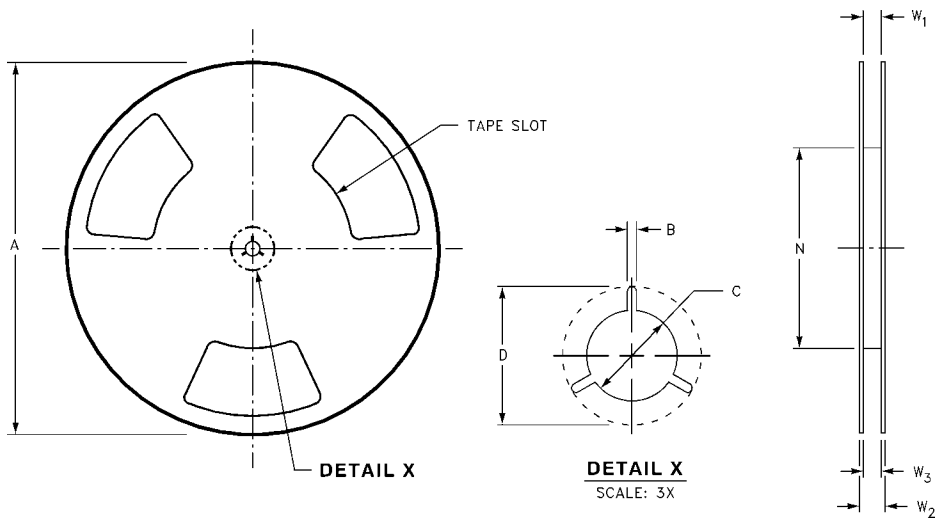
## Tape and Reel Specification (Continued)

**TAPE FORMAT for MicroPak**

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|---|---|---|---|---|
| L6X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 5000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

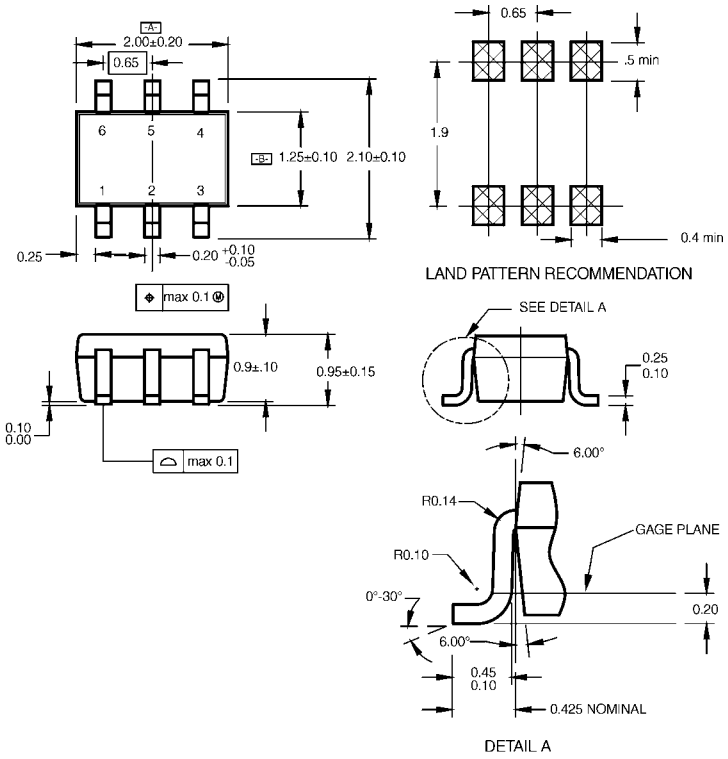



**REEL DIMENSIONS** inches (millimeters)




| Tape Size | A | B | C | D | N | W1 | W2 | W3 |
|---|---|---|---|---|---|---|---|---|
| 8 mm | 7.0 (177.8) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00) | 0.567 (14.40) | W1 + 0.078/–0.039 (W1 + 2.00/–1.00) |

## Physical Dimensions inches (millimeters) unless otherwise noted



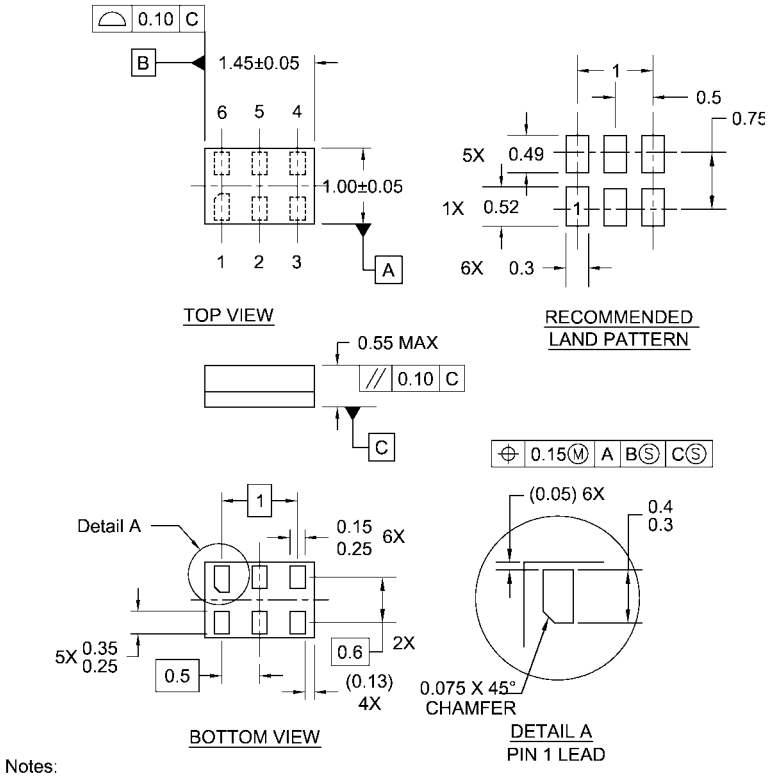

NOTES:

A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

**6-Lead SC70, EIAJ SC88, 1.25mm Wide**
**Package Number MAA06A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**6-Lead MicroPak, 1.0mm Wide**
**Package Number MAC06A**



**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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