

# 74ALVC32

## Low Voltage Quad 2-Input OR Gate with 3.6V Tolerant Inputs and Outputs

### Features

- 1.65V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$ :
  - 2.8ns max for 3.0V to 3.6V  $V_{CC}$
  - 3.1ns max for 2.3V to 2.7V  $V_{CC}$
  - 4.7ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model > 250V

### General Description

The ALVC32 contains four 2-input OR gates. This product is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The ALVC32 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

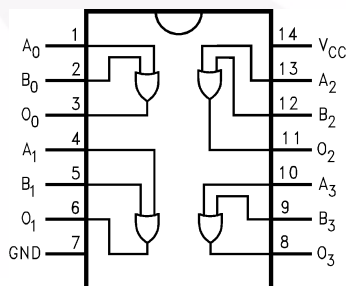
### Ordering Information

Order Number	Package Number	Package Description
74ALVC32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ALVC32MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

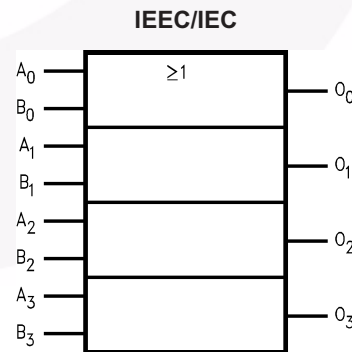
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram



### Logic Symbol



### Pin Description

Pin Names	Description
$A_n, B_n$	Inputs
$O_n$	Outputs

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +4.6V
$V_I$	DC Input Voltage	-0.5V to 4.6V
$V_O$	Output Voltage <sup>(1)</sup>	-0.5V to $V_{CC}$ +0.5V
$I_{IK}$	DC Input Diode Current, $V_I < 0V$	-50mA
$I_{OK}$	DC Output Diode Current, $V_O < 0V$	-50mA
$I_{OH}/I_{OL}$	DC Output Source/Sink Current	$\pm 50mA$
$I_{CC}$ or GND	DC $V_{CC}$ or GND Current per Supply Pin	$\pm 100mA$
$T_{STG}$	Storage Temperature Range	-65°C to +150°C

### Note:

1.  $I_O$  Absolute Maximum Rating must be observed, limited to 4.6V.

## Recommended Operating Conditions<sup>(2)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	1.65V to 3.6V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Free Air Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: $V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	5ns/V

### Note:

2. Floating or unused control inputs must be held HIGH or LOW.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	Min.	Max.	Units
V <sub>IH</sub>	HIGH Level Input Voltage	1.65–1.95		0.65 x V <sub>CC</sub>		V
		2.3–2.7		1.7		
		2.7–3.6		2.0		
V <sub>IL</sub>	LOW Level Input Voltage	1.65–1.95			0.35 x V <sub>CC</sub>	V
		2.3–2.7			0.7	
		2.7–3.6			0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	1.65–3.6	I <sub>OH</sub> = –100μA	V <sub>CC</sub> – 0.2		V
		1.65	I <sub>OH</sub> = –4mA	1.2		
		2.3	I <sub>OH</sub> = –6mA	2.0		
		2.3	I <sub>OH</sub> = –12mA	1.7		
		2.7		2.2		
		3.0		2.4		
		3.0	I <sub>OH</sub> = –24mA	2		
V <sub>OL</sub>	LOW Level Output Voltage	1.65–3.6	I <sub>OL</sub> = 100μA		0.2	V
		1.65	I <sub>OL</sub> = 4mA		0.45	
		2.3	I <sub>OL</sub> = 6mA		0.4	
		2.3	I <sub>OL</sub> = 12mA		0.7	
		2.7			0.4	
		3.0	I <sub>OL</sub> = 24mA		0.55	
I <sub>I</sub>	Input Leakage Current	3.6	0 ≤ V <sub>I</sub> ≤ 3.6V		±5.0	μA
I <sub>CC</sub>	Quiescent Supply Current	3.6	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	3–3.6	V <sub>IH</sub> = V <sub>CC</sub> – 0.6V		750	μA

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = –40°C to +85°C, R <sub>L</sub> = 500Ω								Units
		C <sub>L</sub> = 50pF				C <sub>L</sub> = 30pF				
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 1.8V ± 0.15V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	1.0	2.8		2.9	1.0	3.1	1.0	4.7	ns

## Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C		Units
			V <sub>CC</sub>	Typical	
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	4	pF
C <sub>PD</sub>	Power Dissipation Capacitance	f = 10MHz, C <sub>L</sub> = 50pF	3.3	26	pF
			2.5	24	
			1.8	23	

## AC Loading and Waveforms

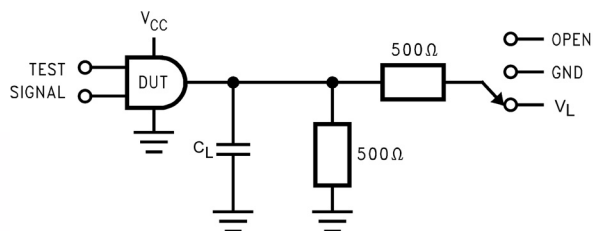


Figure 1. AC Test Circuit

Table 1. Values for Figure 1

Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open

Table 2. Variable Matrix

(Input Characteristics:  $f = 1\text{MHz}$ ;  $t_r = t_f = 2\text{ns}$ ;  $Z_0 = 50\Omega$ )

Symbol	$V_{CC}$			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
$V_{mi}$	1.5V	1.5V	$V_{CC} / 2$	$V_{CC} / 2$
$V_{mo}$	1.5V	1.5V	$V_{CC} / 2$	$V_{CC} / 2$

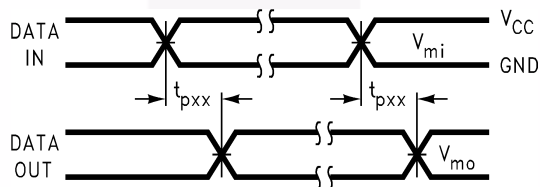
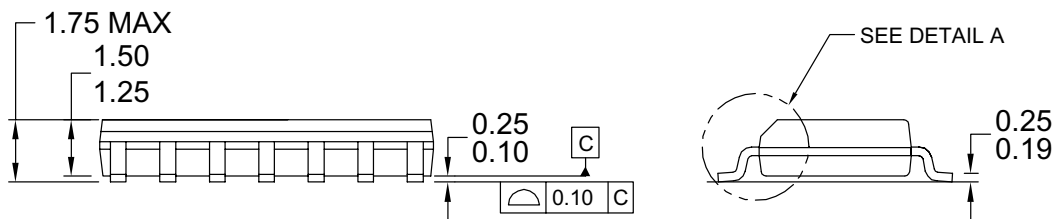
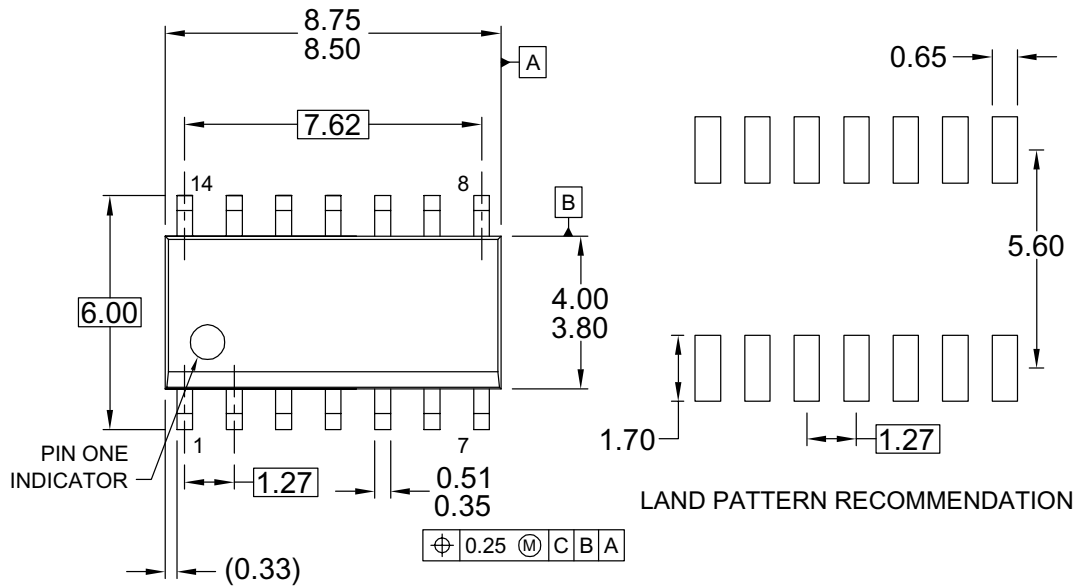
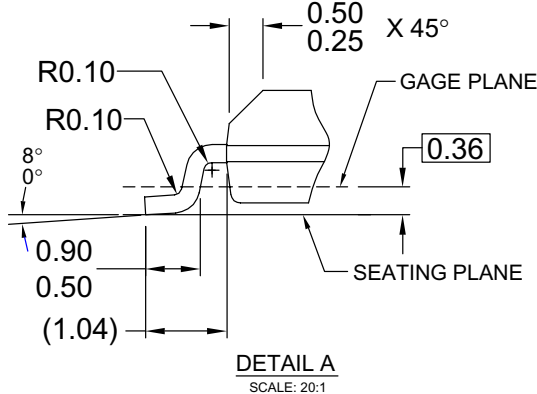


Figure 2. Waveform for Inverting and Non-inverting Functions

### Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

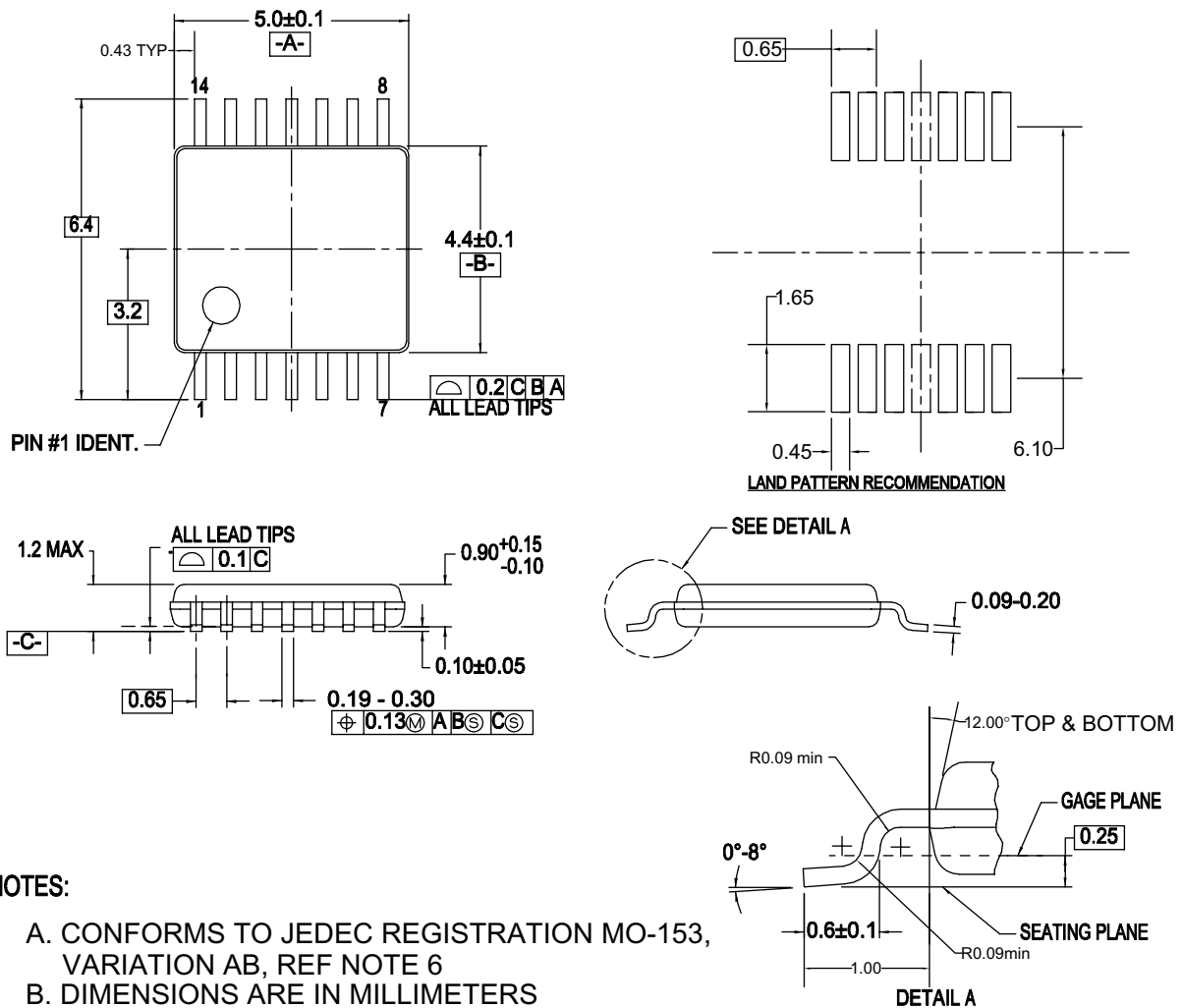
**Figure 3. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 4. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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

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|   |  | SuperSOT <sup>™</sup> -8               |                                  |

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