MC74VHC540

Octal Bus Buffer
Inverting

The MC74VHC540 is an advanced high speed CMOS inverting octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC540 features inputs and outputs on opposite sides of the package and two AND−ed active−low output enables. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features
High Speed: t_{PD} = 3.7 ns (Typ) at V_{CC} = 5.0 V
Low Power Dissipation: I_{CC} = 4.0 μA (Max) at T_A = 25°C
High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
Power Down Protection Provided on Inputs
Balanced Propagation Delays
Designed for 2.0 V to 5.5 V Operating Range
Low Noise: V_{OLP} = 1.2 V (Max)
Pin and Function Compatible with Other Standard Logic Families
Latchup Performance Exceeds 300 mA
ESD Performance: HBM > 2000 V; Machine Model > 200 V
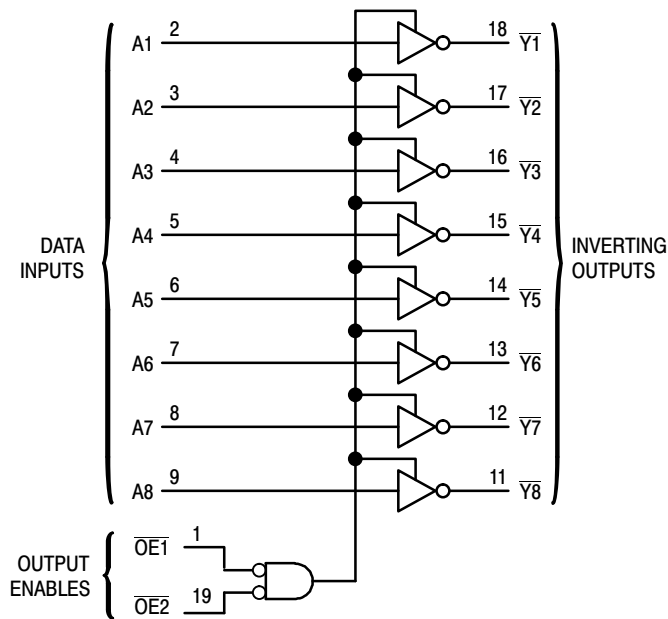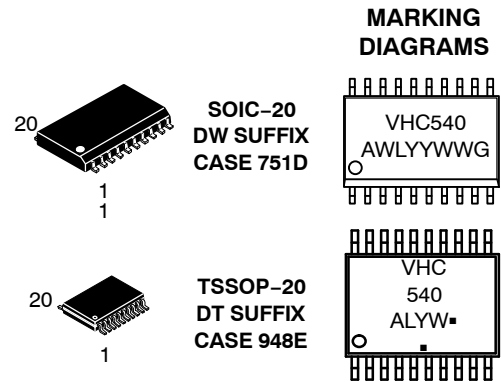Chip Complexity: 124 FETs or 31 Equivalent Gates

Figure 1. Logic Diagram

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

SOIC−20
DW SUFFIX
CASE 751D

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VHC540
AWLYYWWG
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TSSOP−20
DT SUFFIX
CASE 948E

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VHC
540
ALYW∎
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A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ∎ = Pb−Free Package

PIN ASSIGNMENT

$\overline{OE1}$	1	20	V_{CC}
A1	2	19	$\overline{OE2}$
A2	3	18	$\overline{Y1}$
A3	4	17	$\overline{Y2}$
A4	5	16	$\overline{Y3}$
A5	6	15	$\overline{Y4}$
A6	7	14	$\overline{Y5}$
A7	8	13	$\overline{Y6}$
A8	9	12	$\overline{Y7}$
GND	10	11	$\overline{Y8}$

FUNCTION TABLE

Inputs			Output $\overline{Y}$
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Publication Order Number:
MC74VHC540/D

MC74VHC540

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to $+7.0$	V
V_{in}	DC Input Voltage	-0.5 to $+7.0$	V
V_{out}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: -7 mW/°C from 65° to 125°C
            TSSOP Package: -6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25$°C			$T_A = -55$ to 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -55$ to $125°C$ Min	$T_A = -55$ to $125°C$ Max	Unit
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -55$ to $125°C$ Min	$T_A = -55$ to $125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to $\overline{Y}$ (Figures 1 and 3)	$V_{CC} = 3.3 \pm 0.3V$	C_L = 15pF C_L = 50pF		4.8 7.3	7.0 10.5	1.0 1.0	8.5 12.0	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15pF C_L = 50pF		3.7 5.2	5.0 7.0	1.0 1.0	6.0 8.0	
t_{PZL}, t_{PZH}	Output Enable TIme, $\overline{OEn}$ to $\overline{Y}$ (Figures 2 and 4)	$V_{CC} = 3.3 \pm 0.3V$ R_L = 1kΩ	C_L = 15pF C_L = 50pF		6.8 9.3	10.5 14.0	1.0 1.0	12.5 16.0	ns
		$V_{CC} = 5.0 \pm 0.5V$ R_L = 1kΩ	C_L = 15pF C_L = 50pF		4.7 6.2	7.2 9.2	1.0 1.0	8.5 10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OEn}$ to $\overline{Y}$ (Figures 2 and 4)	$V_{CC} = 3.3 \pm 0.3V$ R_L = 1kΩ	C_L = 50pF		11.2	15.4	1.0	17.5	ns
		$V_{CC} = 5.0 \pm 0.5V$ R_L = 1kΩ	C_L = 50pF		6.0	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3V$ (Note 1)	C_L = 50pF			1.5			ns
		$V_{CC} = 5.0 \pm 0.5V$ (Note 1)	C_L = 50pF			1.0			ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2)	17	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.9	− 1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

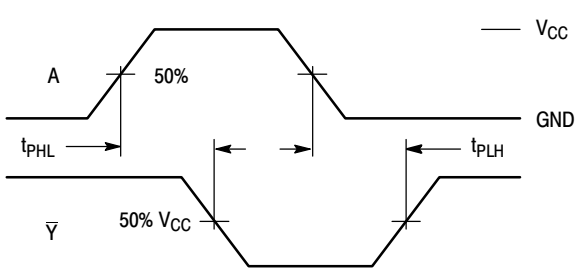# MC74VHC540

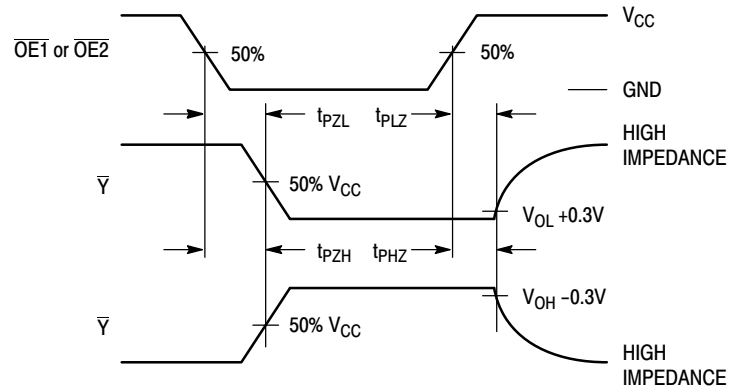## SWITCHING WAVEFORMS

Figure 2.
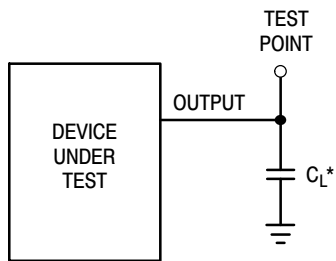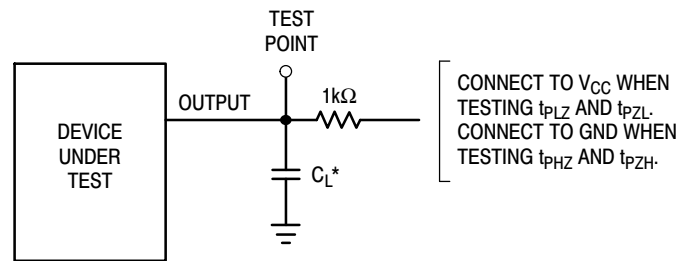

Figure 3.

TEST CIRCUITS

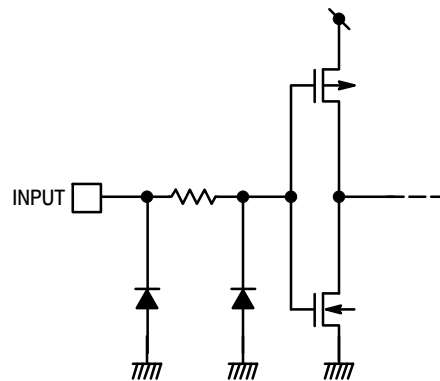*Includes all probe and jig capacitance

Figure 4.

CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}.
CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.

*Includes all probe and jig capacitance

Figure 5.

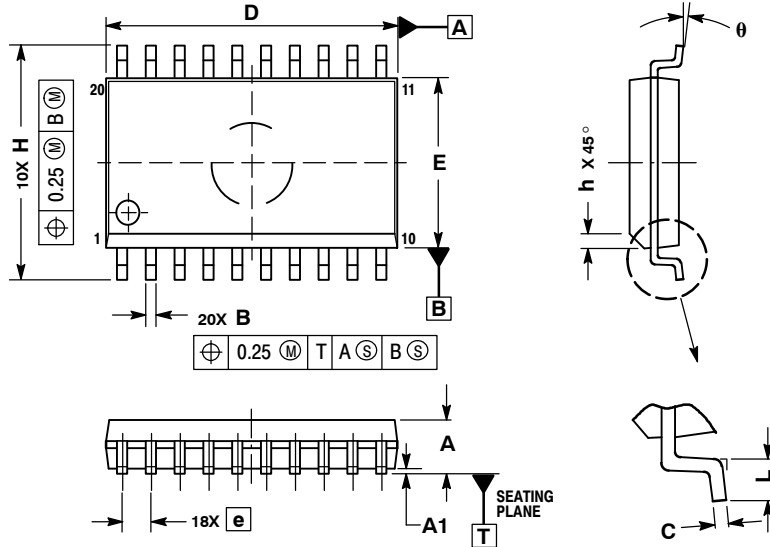## INPUT EQUIVALENT CIRCUIT

MC74VHC540

ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC540DW	SOIC−20	38 Units / Rail
MC74VHC540DWR2	SOIC−20	1000 Units / Tape & Reel
MC74VHC540DWR2G	SOIC−20 (Pb−Free)	
MC74VHC540DT	TSSOP−20	75 Units / Rail
MC74VHC540DTR2	TSSOP−20	2500 Units / Tape & Reel
MC74VHC540DTR2G	TSSOP−20 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MC74VHC540

PACKAGE DIMENSIONS

TSSOP−20
DT SUFFIX
CASE 948E−02
ISSUE C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SECTION N−N

DETAIL E

SEATING PLANE

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

MC74VHC540

PACKAGE DIMENSIONS

SOIC−20
DW SUFFIX
CASE 751D−05
ISSUE G

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

MC74VHC540/D