

# Octal Bus Buffer/Line Driver Inverting with 3-State Outputs

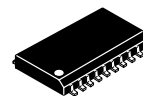
The MC74VHC240 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC240 is an inverting 3-state buffer, and has two active-low output enables. This device is designed to drive bus lines or buffer memory address registers.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed:  $t_{PD} = 3.6ns$  (Typ) at  $V_{CC} = 5V$
- Low Power Dissipation:  $I_{CC} = 4\mu A$  (Max) at  $T_A = 25^\circ C$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise:  $V_{OLP} = 0.9V$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 120 FETs or 30 Equivalent Gates
- **These devices are available in Pb-free package(s). Specifications herein apply to both standard and Pb-free devices. Please see our website at [www.onsemi.com](http://www.onsemi.com) for specific Pb-free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

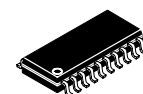
## MC74VHC240



**DW SUFFIX**  
20-LEAD SOIC WIDE PACKAGE  
CASE 751D-05



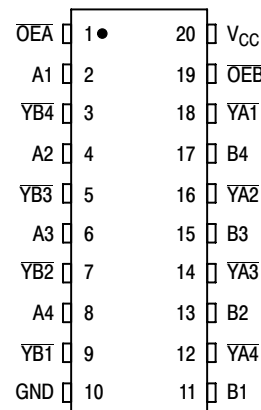
**DT SUFFIX**  
20-LEAD TSSOP PACKAGE  
CASE 948E-02



**M SUFFIX**  
20-LEAD SOIC EIAJ PACKAGE  
CASE 967-01

### ORDERING INFORMATION

|              |           |
|--------------|-----------|
| MC74VHCXXXDW | SOIC WIDE |
| MC74VHCXXXDT | TSSOP     |
| MC74VHCXXXM  | SOIC EIAJ |



### PIN ASSIGNMENT

### FUNCTION TABLE

| INPUTS   |      | OUTPUTS |
|----------|------|---------|
| OEA, OEB | A, B | YA, YB  |
| L        | L    | H       |
| L        | H    | L       |
| H        | X    | Z       |

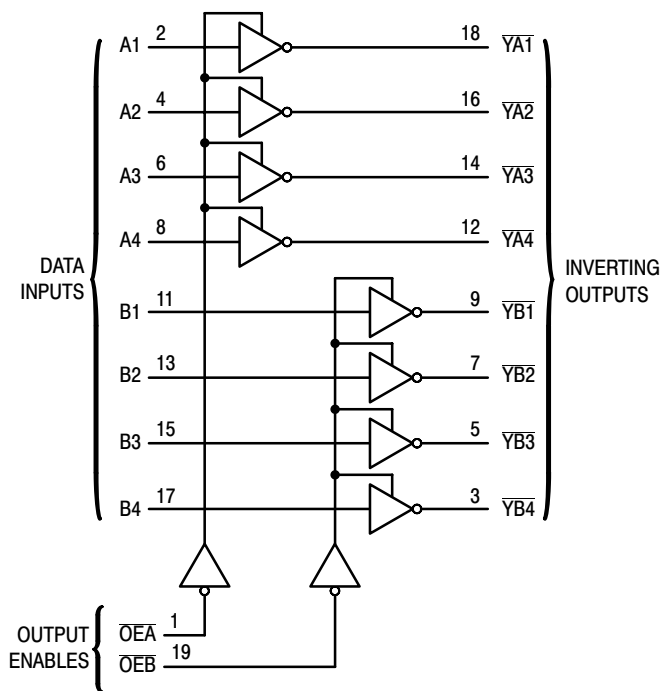


Figure 1. LOGIC DIAGRAM

**MAXIMUM RATINGS\***

| Symbol    | Parameter   | Value                   | Unit |
|-----------|---|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage   | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage  | - 0.5 to + 7.0          | V    |
| $V_{out}$ | DC Output Voltage   | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{IK}$  | Input Diode Current   | - 20                    | mA   |
| $I_{OK}$  | Output Diode Current  | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin                                    | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                      | $\pm 75$                | mA   |
| $P_D$     | Power Dissipation in Still Air, SOIC Packages† TSSOP Package† | 500<br>450              | mW   |
| $T_{stg}$ | Storage Temperature   | - 65 to + 150           | °C   |

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

†Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

| Symbol     | Parameter                                | Min  | Max            | Unit |
|------------|--|--|----------------|------|
| $V_{CC}$   | DC Supply Voltage                        | 2.0  | 5.5            | V    |
| $V_{in}$   | DC Input Voltage                         | 0  | 5.5            | V    |
| $V_{out}$  | DC Output Voltage                        | 0  | $V_{CC}$       | V    |
| $T_A$      | Operating Temperature, All Package Types | - 40   | + 85           | °C   |
| $t_r, t_f$ | Input Rise and Fall Time                 | $V_{CC} = 3.3V \pm 0.3V$<br>$V_{CC} = 5.0V \pm 0.5V$ | 0<br>100<br>20 | ns/V |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

| Symbol          | Parameter                           | Test Conditions  | V <sub>CC</sub><br>V | T <sub>A</sub> = 25°C         |                   |                               | T <sub>A</sub> = - 40 to 85°C |                               | Unit |
|-----------------|-------------------------------------|--|----------------------|-------------------------------|-------------------|-------------------------------|-------------------------------|-------------------------------|------|
|                 |                                     |  |                      | Min                           | Typ               | Max                           | Min                           | Max                           |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage    |  | 2.0<br>3.0 to<br>5.5 | 1.50<br>V <sub>CC</sub> x 0.7 |                   |                               | 1.50<br>V <sub>CC</sub> x 0.7 |                               | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage     |  | 2.0<br>3.0 to<br>5.5 |                               |                   | 0.50<br>V <sub>CC</sub> x 0.3 |                               | 0.50<br>V <sub>CC</sub> x 0.3 | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OH</sub> = - 50μA                           | 2.0<br>3.0<br>4.5    | 1.9<br>2.9<br>4.4             | 2.0<br>3.0<br>4.5 |                               | 1.9<br>2.9<br>4.4             |                               | V    |
|                 |                                     | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OH</sub> = - 4mA<br>I <sub>OH</sub> = - 8mA | 3.0<br>4.5           | 2.58<br>3.94                  |                   |                               | 2.48<br>3.80                  |                               |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage    | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OL</sub> = 50μA                             | 2.0<br>3.0<br>4.5    |                               | 0.0<br>0.0<br>0.0 | 0.1<br>0.1<br>0.1             |                               | 0.1<br>0.1<br>0.1             | V    |
|                 |                                     | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OL</sub> = 4mA<br>I <sub>OL</sub> = 8mA     | 3.0<br>4.5           |                               |                   | 0.36<br>0.36                  | 0.44<br>0.44                  |                               |      |
| I <sub>in</sub> | Maximum Input Leakage Current       | V <sub>in</sub> = 5.5V or GND  | 0 to 5.5             |                               |                   | ±0.1                          |                               | ±1.0                          | μA   |
| I <sub>oz</sub> | Maximum Three-State Leakage Current | V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND          | 5.5                  |                               |                   | ±0.25                         |                               | ±2.5                          | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current    | V <sub>in</sub> = V <sub>CC</sub> or GND   | 5.5                  |                               |                   | 4.0                           |                               | 40.0                          | μA   |

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r = t_f = 3.0\text{ns}$ )

| Symbol                     | Parameter   | Test Conditions                                    | $T_A = 25^\circ\text{C}$ |      |      | $T_A = -40 \text{ to } 85^\circ\text{C}$ |      | Unit |
|----------------------------|---|--|--------------------------|------|------|--|------|------|
|                            |   |  | Min                      | Typ  | Max  | Min                                      | Max  |      |
| $t_{PLH}$ ,<br>$t_{PHL}$   | Maximum Propagation Delay,<br>A to $\overline{Y_A}$ or B to $\overline{Y_B}$                          | $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ |                          | 5.3  | 7.5  | 1.0                                      | 9.0  | ns   |
|                            |   | $C_L = 50\text{pF}$                                |                          | 7.8  | 11.0 | 1.0                                      | 12.5 |      |
| $t_{PZL}$ ,<br>$t_{PZH}$   | Output Enable Time<br>$\overline{OE_A}$ to $\overline{Y_A}$ or $\overline{OE_B}$ to $\overline{Y_B}$  | $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ |                          | 6.6  | 10.6 | 1.0                                      | 12.5 | ns   |
|                            |   | $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$        |                          | 9.1  | 14.1 | 1.0                                      | 16.0 |      |
| $t_{PLZ}$ ,<br>$t_{PHZ}$   | Output Disable Time<br>$\overline{OE_A}$ to $\overline{Y_A}$ or $\overline{OE_B}$ to $\overline{Y_B}$ | $V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$ |                          | 4.7  | 7.3  | 1.0                                      | 8.5  | ns   |
|                            |   | $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$        |                          | 6.2  | 9.3  | 1.0                                      | 10.5 |      |
| $t_{PLZ}$ ,<br>$t_{PHZ}$   | Output Disable Time<br>$\overline{OE_A}$ to $\overline{Y_A}$ or $\overline{OE_B}$ to $\overline{Y_B}$ | $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$ |                          | 10.3 | 14.0 | 1.0                                      | 16.0 | ns   |
|                            |   | $R_L = 1\text{k}\Omega$                            |                          | 6.7  | 9.2  | 1.0                                      | 10.5 |      |
| $t_{OSLH}$ ,<br>$t_{OSHL}$ | Output to Output Skew   | $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$ |                          |      | 1.5  |  | 1.5  | ns   |
|                            |   | (Note 1.)  |                          |      | 1.0  |  | 1.0  |      |
| $C_{in}$                   | Maximum Input Capacitance   |  |                          | 4    | 10   |  | 10   | pF   |
| $C_{out}$                  | Maximum Three-State Output Capacitance (Output in High-Impedance State)                               |  |                          | 6    |      |  |      | pF   |

|          |   |   |    |
|----------|---|---|----|
| $C_{PD}$ | Power Dissipation Capacitance (Note 2.) | <b>Typical @ <math>25^\circ\text{C}</math>, <math>V_{CC} = 5.0\text{V}</math></b> | pF |
|          |   | 17  |    |

- Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$ .
- $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$  (per bit).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

**NOISE CHARACTERISTICS** (Input  $t_r = t_f = 3.0\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $V_{CC} = 5.0\text{V}$ )

| Symbol    | Parameter                                | $T_A = 25^\circ\text{C}$ |      | Unit |
|-----------|--|--------------------------|------|------|
|           |  | Typ                      | Max  |      |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$    | 0.6                      | 0.9  | V    |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$    | -0.6                     | -0.9 | V    |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage |                          | 3.5  | V    |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage  |                          | 1.5  | V    |

## SWITCHING WAVEFORMS

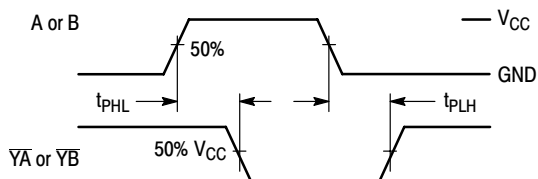


Figure 2.

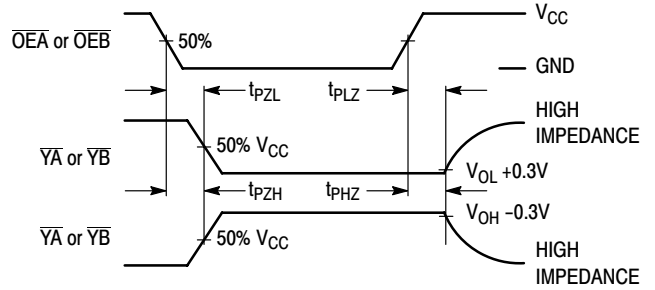
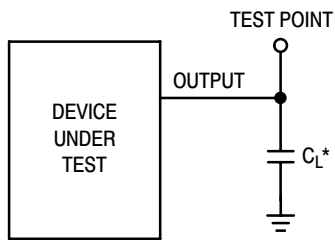


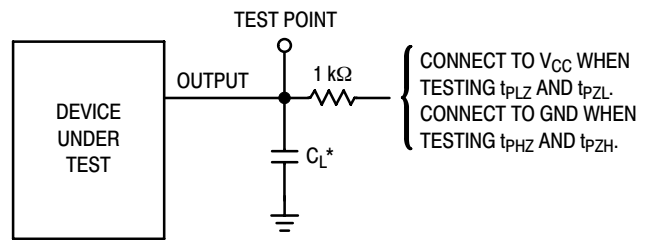
Figure 3.

## TEST CIRCUITS



\*Includes all probe and jig capacitance

Figure 4. Test Circuit



\*Includes all probe and jig capacitance

Figure 5. Test Circuit

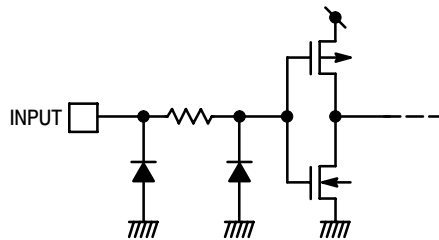
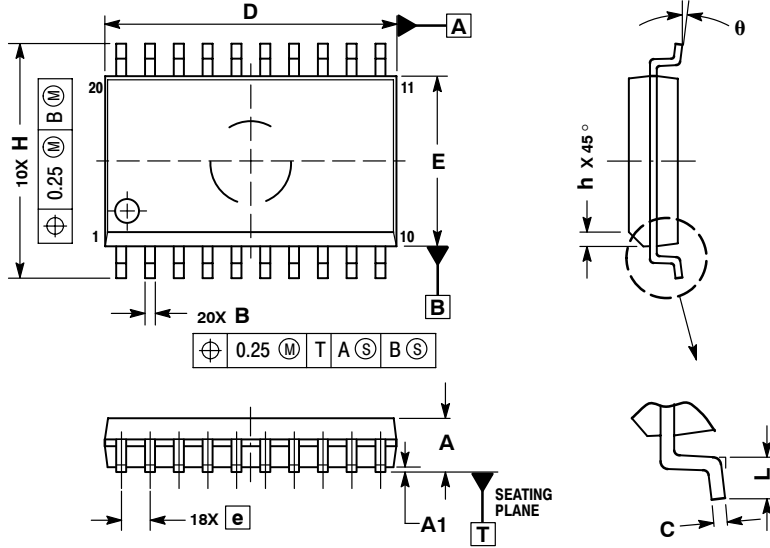


Figure 6. Input Equivalent Circuit

# OUTLINE DIMENSIONS

## DW SUFFIX SOIC CASE 751D-05 ISSUE F



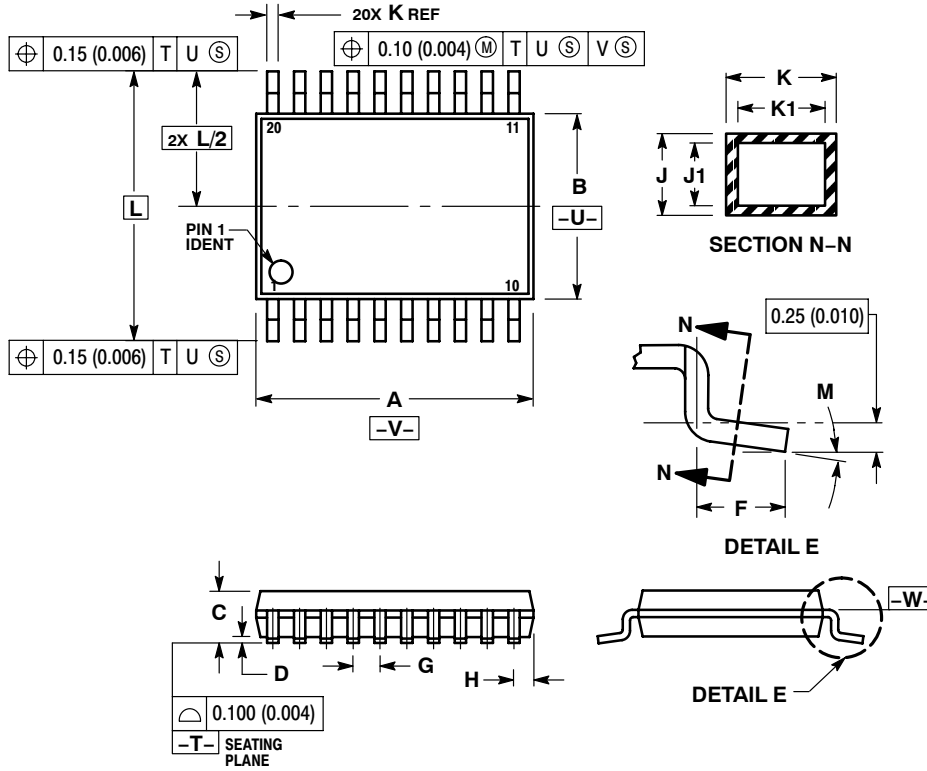
### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN         | MAX   |
| A   | 2.35        | 2.65  |
| A1  | 0.10        | 0.25  |
| B   | 0.35        | 0.49  |
| C   | 0.23        | 0.32  |
| D   | 12.65       | 12.95 |
| E   | 7.40        | 7.60  |
| e   | 1.27 BSC    |       |
| H   | 10.05       | 10.55 |
| h   | 0.25        | 0.75  |
| L   | 0.50        | 0.90  |
| θ   | 0°          | 7°    |

# OUTLINE DIMENSIONS

## DT SUFFIX TSSOP CASE 948E-02 ISSUE A



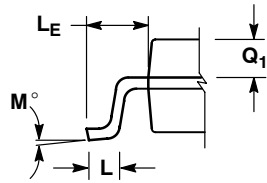
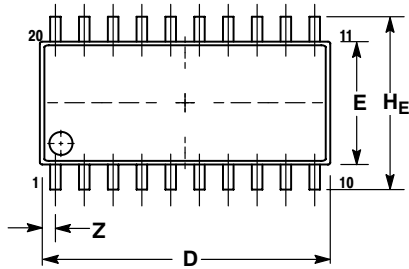
### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

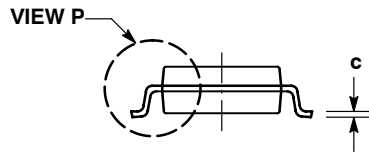
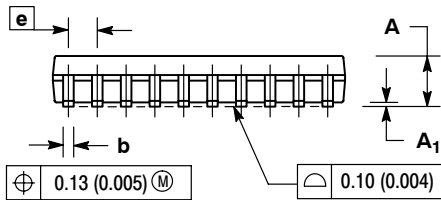
| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 6.40        | 6.60 | 0.252     | 0.260 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.27        | 0.37 | 0.011     | 0.015 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

# OUTLINE DIMENSIONS

## M SUFFIX SOIC EIAJ CASE 967-01 ISSUE O



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.18        | 0.27  | 0.007     | 0.011 |
| D              | 12.35       | 12.80 | 0.486     | 0.504 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.81  | ---       | 0.032 |

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.

**MC74VHC240/D**