3-Input OR Gate

The NLX1G332 is an advanced high-speed 3-input CMOS OR gate in ultra-small footprint.

The NLX1G332 input structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 2.4 \text{ ns} (Typ) @ V_{CC} = 5.0 \text{ V}$
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: $I_{CC} = 1 \mu A$ (Max) at $T_A = 25^{\circ}C$
- 24 mA Balanced Output Source and Sink Capability
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- Ultra-Small Packages
- These are Pb–Free Devices

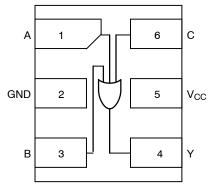




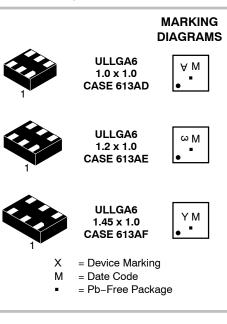


Figure 2. Logic Symbol



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PIN ASSIGNMENT

Pin	Function
1	A
2	GND
3	В
4	Y
5	V _{CC}
6	С

FUNCTION TABLE

	Output		
Α	В	С	Y
н	Х	Х	Н
X	Н	Х	Н
X	Х	Н	Н
L	L	L	L

H – HIGH Logic Level

L – LOW Logic Level

X = Either LOW or HIGH Logic Level

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-50	mA
Ι _{ΟΚ}	DC Output Diode Current V _{OUT} < GND	-50	mA
Ι _Ο	DC Output Source/Sink Current	±50	mA
I _{CC}	DC Supply Current Per Supply Pin	±100	mA
I _{GND}	DC Ground Current per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
ΤL	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
TJ	Junction Temperature Under Bias	150	°C
θ_{JA}	Thermal Resistance (Note 1)	496	°C/W
PD	Power Dissipation in Still Air @ 85°C	252	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
ILATCHUP	Latchup Performance Above V $_{CC}$ and Below GND at 125 $^\circ \! C$ (Note 5)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability. 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

2. Tested to EIA/JESD22-A114-A.

3. Tested to EIA/JESD22-A115-A.

4. Tested to JESD22-C101-A.

5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Paramet	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _{IN}	N Digital Input Voltage (Note 6)		0	5.5	V
V _{OUT}	Output Voltage		0	5.5	V
T _A	Operating Free-Air Temperature		-55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	$\begin{array}{l} V_{CC} = 1.8 \ V \pm 0.15 \ V \\ V_{CC} = 2.5 \ V \pm 0.2 \ V \\ V_{CC} = 3.3 \ V \pm 0.3 \ V \\ V_{CC} = 5.0 \ V \pm 0.5 \ V \end{array}$	0 0 0 0	20 20 10 5	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high or low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

			Vcc	l 1	A = 25 °	С	T _A = -55°C	c to +125°C	
Symbol	Parameter	Conditions	(V)	Min	Тур	Max	Min	Мах	Unit
V _{IH}	Low-Level		1.65	$0.75 ext{ v}_{CC}$			0.75 x V _{CC}		V
	Input Voltage		2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}		
V _{IL}	Low-Level		1.65			0.25 x V _{CC}		0.25 x V _{CC}	V
	Input Voltage		2.3 – 5.5			$0.30 \times V_{CC}$		$0.30 \times V_{CC}$	
V _{OH}	High– Level Output	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -100 \ \mu A$	1.65 – 5.5	V _{CC} -0.1	V _{CC}		V _{CC} -0.1		V
	Voltage		1.65 2.3 2.7 3.0 3.0 4.5	1.29 1.9 2.2 2.4 2.3 3.8	1.52 2.15 2.4 2.8 2.68 4.2		1.29 1.9 2.2 2.4 2.3 3.8		
V _{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 100 \ \mu A$	1.65 – 5.5			0.1		0.1	V
	voltage		1.65 2.3 2.7 3.0 3.0 4.5		0.08 0.1 0.12 0.15 0.22 0.22	0.24 0.3 0.4 0.4 0.55 0.55		0.24 0.3 0.4 0.4 0.55 0.55	
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5V$	0 to 5.5			±0.1		±1.0	μΑ
I _{OFF}	Power-Off Output Leakage Current	V _{IN} or V _{OUT} = 5.5 V	0			1.0		10	μΑ
I _{CC}	Quiescent Supply Current	$0 \le V_{IN} \le V_{CC}$	5.5			1.0		10	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 2.5 \text{ nS}$)

		V _{CC}	Test	1	Γ _A = 25 °C	;	T _A = -5 +12	5°C to 5°C	
Symbol	Parameter	(V)	Condition	Min	Тур	Мах	Min	Мах	Unit
t _{PLH} ,	Propagation Delay,	1.65–1.95	R_L = 1 M Ω , C_L = 15 pF	2.0	5.5	18.5	2.0	19	ns
^t PHL	Input to Output	2.3–2.7	R_L = 1 M Ω , C_L = 15 pF	0.8	3.0	11	0.8	11.5	
		3.0–3.6	R_L = 1 M Ω , C_L = 15 pF	0.5	2.6	7.5	0.5	8.0	
			$R_L = 500 \Omega, C_L = 50 pF$	1.5	3.0	8.5	1.5	9.0	
		4.5–5.5	R_L = 1 M Ω , C_L = 15 pF	0.5	2.2	5.5	0.5	6.0	
			$R_L = 500 \Omega, C_L = 50 pF$	0.8	2.4	7.0	0.8	7.5	
C _{IN}	Input Capacitance	5.5	$V_{IN} = 0 V \text{ or } V_{CC}$		4.0				pF
C _{PD}	Power Dissipation Capacitance (Note 7)	3.3 5.5	$\begin{array}{c} 10 \text{ MHz} \\ V_{\text{IN}} = 0 \text{ V or } V_{\text{CC}} \end{array}$		20 26				pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

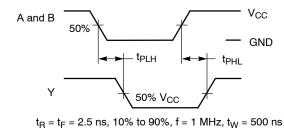
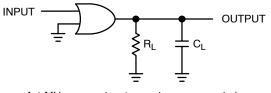


Figure 3. Switching Waveforms



A 1 MHz square input wave is recommended for propagation delay tests

Figure 4. Test Circuit

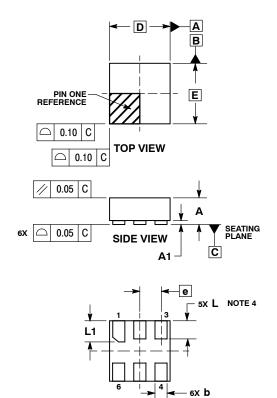
ORDERING INFORMATION

Device	Package	Shipping [†]
NLX1G332AMX1TCG	ULLGA6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G332BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G332CMX1TCG	ULLGA6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

ULLGA6 1.0x1.0, 0.35P CASE 613AD-01 **ISSUE A**



BOTTOM VIEW

0.10

0.05

 \oplus

CAB

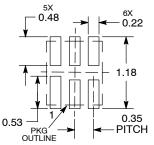
C NOTE 3

NOTES:

- NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS. 3. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
- A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE 4. PACKAGE IS ALLOWED.

	MILLIMETERS		
DIM	MIN MAX		
Α		0.40	
A1	0.00	0.05	
b	0.12	0.22	
D	1.00 BSC		
Е	1.00 BSC		
e	0.35	BSC	
L	0.25	0.35	
L1	0.30	0.40	

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

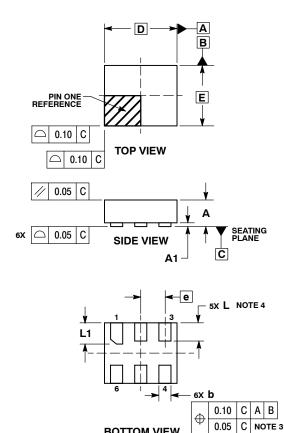


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.2x1.0, 0.4P CASE 613AE-01 **ISSUE A**



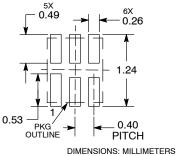
BOTTOM VIEW

NOTES:

- NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS. 3. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP. 4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS			
DIM	MIN	MAX		
Α		0.40		
A1	0.00	0.05		
b	0.15	0.25		
D	1.20 BSC			
Е	1.00 BSC			
е	0.40 BSC			
L	0.25	0.35		
L1	0.35	0.45		

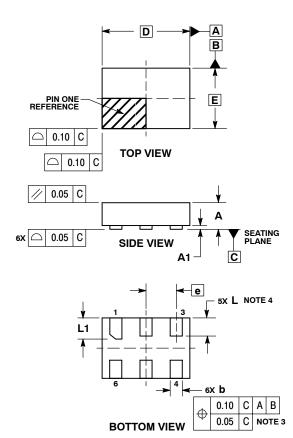
MOUNTING FOOTPRINT SOLDERMASK DEFINED*



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PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P CASE 613AF-01 **ISSUE A**

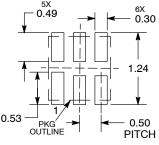


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- ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS. DIMENSION & APPLIES TO PLATED TERMINAL 2 3.
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	MILLIMETERS			
DIM	MIN	MAX		
Α		0.40		
A1	0.00	0.05		
b	0.15	0.25		
D	1.45 BSC			
Е	1.00 BSC			
е	0.50 BSC			
L	0.25	0.35		
L1	0.30	0.40		

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

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