

MC74VHC1GT00

Single 2-Input NAND Gate/ CMOS Logic Level Shifter

LSTTL-Compatible Inputs

The MC74VHC1GT00 is a single gate 2-input NAND fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high voltage power supply.

The MC74VHC1GT00 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT00 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 3.1$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2$ V
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 64
- Pb-Free Packages are Available

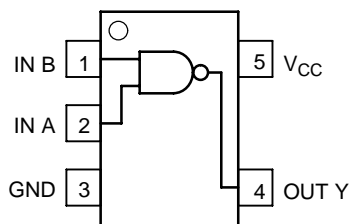


Figure 1. Pinout

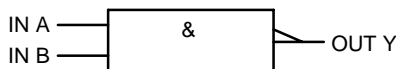


Figure 2. Logic Symbol



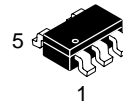
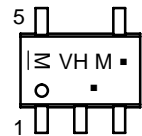
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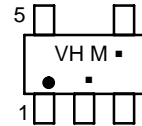
MARKING DIAGRAMS



SC-88A/SC70-5/SOT-353
DF SUFFIX
CASE 419A



TSOP-5/SOT23-5/SC59-5
DT SUFFIX
CASE 483



VH = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

| | |
|---|----------|
| 1 | IN B |
| 2 | IN A |
| 3 | GND |
| 4 | OUT Y |
| 5 | V_{CC} |

FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC1GT00

MAXIMUM RATINGS

| Symbol | Characteristics | Value | Unit |
|----------------------|---|--|------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage | -0.5 to +7.0 | V |
| V _{OUT} | DC Output Voltage V _{CC} = 0 High or Low State | -0.5 to 7.0 -0.5 to V _{CC} + 0.5 | V |
| I _{IK} | Input Diode Current | -20 | mA |
| I _{OK} | Output Diode Current V _{OUT} < GND; V _{OUT} > V _{CC} | +20 | mA |
| I _{OUT} | DC Output Current, per Pin | +25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND | +50 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | +150 | °C |
| θ _{JA} | Thermal Resistance SC70-5/SC-88A/SOT-353 (Note 1) SOT23-5/TSOP-5/SC59-5 | 350 230 | °C/W |
| P _D | Power Dissipation in Still Air at 85°C SC70-5/SC-88A/SOT-353 SOT23-5/TSOP-5/SC59-5 | 150 200 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F _R | Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) | > 2000 > 200 N/A | V |
| I _{LATCHUP} | Latchup Performance Above V _{CC} and Below GND at 125°C (Note 5) | ± 500 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|---------------------------------|--|------------|------------------------|------|
| V _{CC} | DC Supply Voltage | 3.0 | 5.5 | V |
| V _{IN} | DC Input Voltage | 0.0 | 5.5 | V |
| V _{OUT} | DC Output Voltage V _{CC} = 0 High or Low State | 0.0 0.0 | 5.5 V _{CC} | V |
| T _A | Operating Temperature Range | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V | 0 0 | 100 20 | ns/V |

Device Junction Temperature versus Time to 0.1% Bond Failures

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

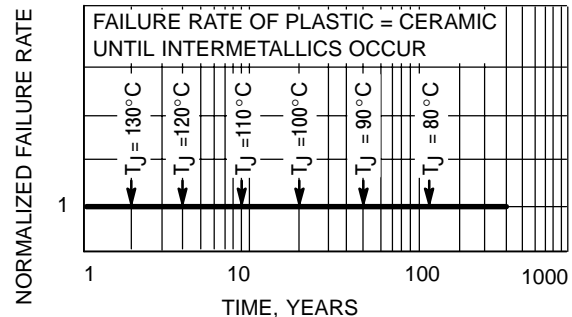


Figure 3. Failure Rate vs. Time Junction Temperature

MC74VHC1GT00

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | -55 ≤ T _A ≤ 125°C | | Unit |
|------------------|---|--|------------------------|-----------------------|------------|--------------------|-----------------------|--------------------|------------------------------|--------------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 3.0 4.5 5.5 | 1.4 2.0 2.0 | | | 1.4 2.0 2.0 | | 1.4 2.0 2.0 | | V |
| V _{IL} | Maximum Low-Level Input Voltage | | 3.0 4.5 5.5 | | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 3.0 4.5 | 2.9 4.4 | 3.0 4.5 | | 2.9 4.4 | | 2.9 4.4 | | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | 2.34 3.66 | | V |
| V _{OL} | Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 3.0 4.5 | | 0.0 0.0 | 0.1 0.1 | | 0.1 0.1 | | 0.1 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | | 0.52 0.52 | V |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 1.0 | | 20 | | 40 | μA |
| I _{CCT} | Quiescent Supply Current | Input: V _{IN} = 3.4 V | 5.5 | | | 1.35 | | 1.50 | | 1.65 | mA |
| I _{OFF} | Power Off Output Leakage Current | V _{OUT} = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |

AC ELECTRICAL CHARACTERISTICS Input t_r = t_f = 3.0 ns

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A ≤ 85°C | | -55 ≤ T _A ≤ 125°C | | Unit |
|--|--|---|-----------------------|------------|--------------|-----------------------|--------------|------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A or B to Y | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 4.1 5.5 | 10.0 13.5 | | 11.0 15.0 | | 13.0 17.5 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 3.1 3.6 | 6.9 7.9 | | 8.0 9.0 | | 9.5 10.5 | |
| C _{IN} | Maximum Input Capacitance | | | 5.5 10 | | | 10 | | 10 | pF |

| C _{PD} | Power Dissipation Capacitance (Note 6) | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
|-----------------|--|---|--|----|
| | | 11 | | |
| | | | | |

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC1GT00

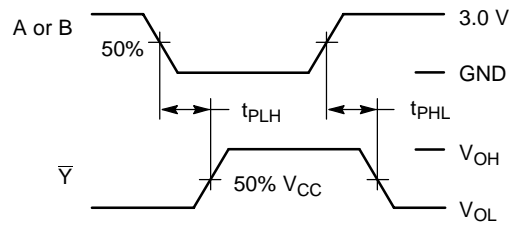
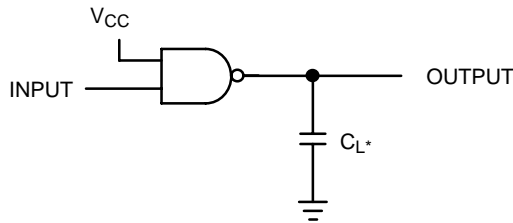


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance.

A 1-MHz square input wave is recommended for propagation delay tests.

Figure 5. Test Circuit

ORDERING INFORMATION

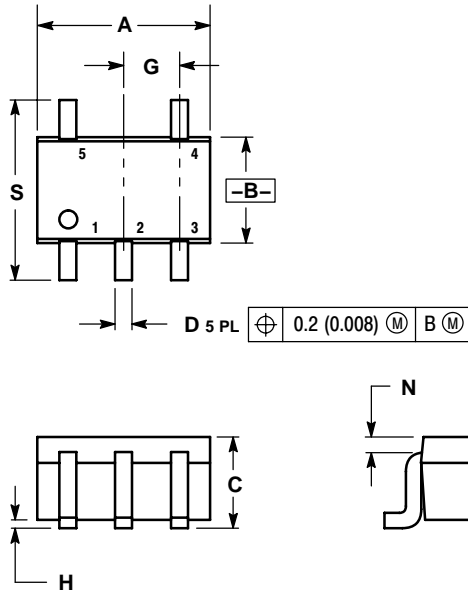
| Device | Package | Shipping† |
|------------------|------------------------------------|------------------|
| MC74VHC1GT00DFT1 | SC70-5/SC-88A/SOT-353 | 3000/Tape & Reel |
| M74VHC1GT00DFT1G | SC70-5/SC-88A/SOT-353 (Pb-Free) | |
| MC74VHC1GT00DFT2 | SC70-5/SC-88A/SOT-353 | |
| M74VHC1GT00DFT2G | SC70-5/SC-88A/SOT-353 (Pb-Free) | |
| MC74VHC1GT00DTT1 | SOT23-5/TSOP-5/SC59-5 | |
| M74VHC1GT00DTT1G | SOT23-5/TSOP-5/SC59-5 (Pb-Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC74VHC1GT00

PACKAGE DIMENSIONS

SC-88A, SOT-353, SC-70
CASE 419A-02
ISSUE J

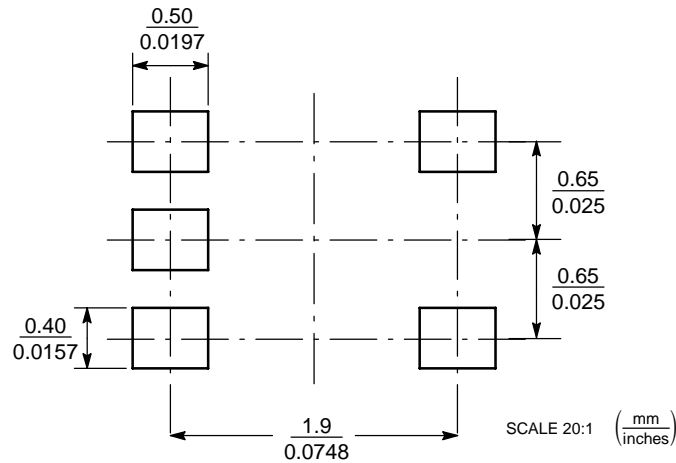


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

SOLDERING FOOTPRINT*

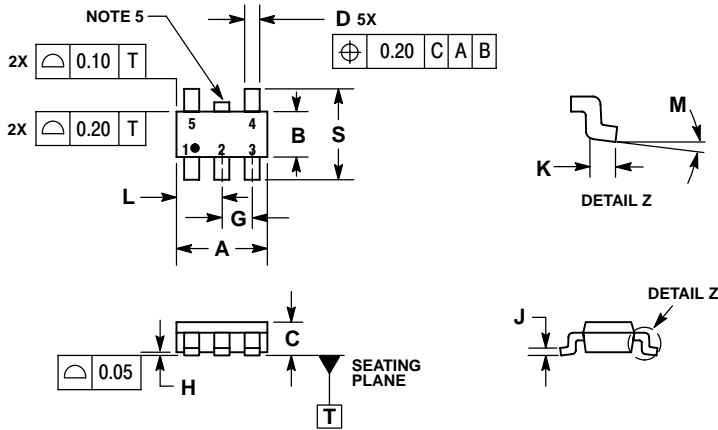


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC1GT00

PACKAGE DIMENSIONS

TSOP-5
CASE 483-02
ISSUE F

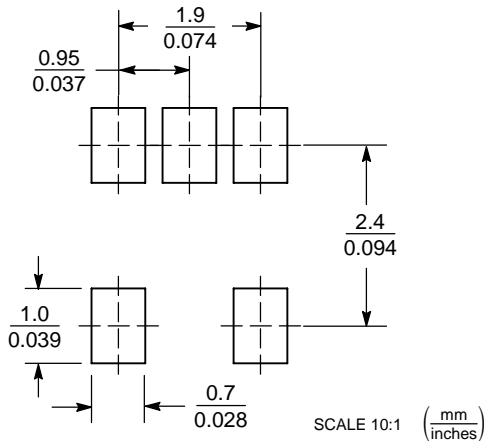


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 3.00 BSC | |
| B | 1.50 BSC | |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| L | 1.25 | 1.55 |
| M | 0° | 10° |
| S | 2.50 | 3.00 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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