

STRUCTURE Silicon Monolithic Integrated Circuit

TYPE single OR gate

PRODUCT SERIES **BU4S71G2**

FEATURES

- Low power consumption
- Wide operating power supply range(3[V]~16[V])

○ ABSOLUTE MAXIMUM RATINGS (Ta=25[°C])

Parameter	Symbol	Limit	Unit
Power Supply Voltage	VDD	(VSS-0.3)~(VSS+18)	V
Power Dissipation	Pd	540(*1)(*2)	mW
Supply current	Iin	± 10	mA
Operating temperature	Topr	-40~+85	°C
Storage temperature	Tstg	-55~+150	°C
Input Voltage	Vin	(VSS-0.3)~(VDD+0.3)	V
Maximum junction temperature	Tjmax	150	°C

• This product is designed for protection against radioactive rays.

(\*1) When used at Ta=25[°C] on above, value of above is reduced 4.32[mW] per 1[°C].

(\*2) Power dissipation is the value for mounting 70[mm]×[70mm]×1.6[mm] FR4 glass epoxy circuit board (copper foil area is 3% or less).

○ OPERATING CONDITION (Ta=-40~+85[°C])

Parameter	Symbol	Limit	Unit
Power Supply Voltage	VDD	+3.0~+16.0	V
Input voltage	VIN	0~VDD	V

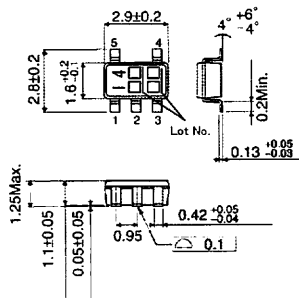
○ ELECTRICAL CHARACTERISTICS (unless otherwise noted, VSS= 0[V], Ta=25[°C])

Parameter	Symbol	Standard Value			Unit	VDD[V]	Condition
		MIN	TYP	MAX			
Input "H" voltage	VIH	3.5	—	—	V	5	IOUT <1[μA]
		7.0	—	—	V	10	
		11.0	—	—	V	15	
Input "L" voltage	VIL	—	—	1.5	V	5	IOUT <1[μA]
		—	—	3.0	V	10	
		—	—	4.0	V	15	
Input "H" current	I <sub>IH</sub>	—	—	0.3	μA	18	VIH=18[V]
Input "L" current	I <sub>IL</sub>	—	—	-0.3	μA	18	VIL=0[V]
Output "H" voltage	VOH	4.95	—	—	V	5	IOUT  <1[μA] VIN=VSS or VDD
		9.95	—	—	V	10	
		14.95	—	—	V	15	
Output "L" voltage	VOL	—	—	0.05	V	5	IOUT  <1[μA] VIN=VSS
		—	—	0.05	V	10	
		—	—	0.05	V	15	
Output "H" current	IOH	-0.51	—	—	mA	5	VOH=4.6[V]
		-2.1	—	—	mA	5	VOH=2.5[V]
		-1.3	—	—	mA	10	VOH=9.5[V]
		-3.4	—	—	mA	15	VOH=13.5[V]
Output "L" current	IOL	0.51	—	—	mA	5	VOL=0.4[V]
		1.3	—	—	mA	10	VOL=0.5[V]
		3.4	—	—	mA	15	VOL=1.5[V]
Static supply current	IDD	—	—	0.25	μA	5	VIN=VSS,VDD
		—	—	0.5	μA	10	
		—	—	1.0	μA	15	

○ Switching Characteristics (unless otherwise noted, VSS=0[V], Ta=25[°C], CL=50[pF])

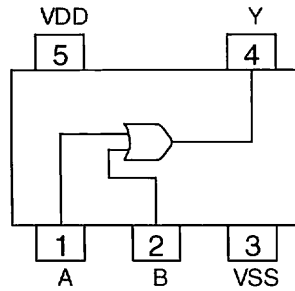
Parameter	Symbol	Standard Value			Unit	VDD[V]	Condition
		MIN	TYP	MAX			
Output rising time	t <sub>TLH</sub>	—	70	—	ns	5	—
		—	35	—	ns	10	
		—	30	—	ns	15	
Output falling time	t <sub>THL</sub>	—	70	—	ns	5	—
		—	35	—	ns	10	
		—	30	—	ns	15	
Propagation delay time	t <sub>PLH</sub>	—	90	—	ns	5	—
		—	45	—	ns	10	
		—	30	—	ns	15	
	t <sub>PHL</sub>	—	90	—	ns	5	—
		—	45	—	ns	10	
		—	30	—	ns	15	
Input capacitance	C <sub>IN</sub>	—	5	—	pF	5	—

○ PHYSICAL DIMENSIONS



BU4S71G2(SSOP5)(UNIT:[mm])

○ BLOCK DIAGRAM



○ PIN DESCRIPTION

PIN No.	PIN NAME
1	A
2	B
3	VSS
4	Y
5	VDD

○ NOTES FOR USE

(1) Absolute maximum ratings

Exceeding the absolute maximum ratings, including applied voltage and operating temperature range, may damage or destroy the IC. Since the cause of the damage cannot be conclusively identified (as, for example, a short or open mode), be sure to take appropriate physical safety measures, such as incorporating fuses, whenever a special mode anticipated to exceed absolute maximum ratings is employed.

(2) External voltage at input terminal

VDD+0.3[V], VSS-0.3[V] can be input led without characteristics deterioration and destruction. However the circuit operation is not guaranteed. Please use within recommended operating conditions.

(3) Power Dissipation

If the IC is used out of this power dissipation area, the faulty operation or reduction of current characteristics may occur due to the rise of IC temperature. Also, be sure to Use this IC within a power dissipation range while also allowing enough margins.

(4) Mounting errors

Mounting errors, such as incorrect positioning or orientation, may destroy the device.

(5) Electromagnetic fields

Use in strong electromagnetic fields may cause malfunctions. Be careful operating in electromagnetic fields.

(6) Treatment of IC

Stress (camber, bend etc) may cause characteristic change due to piezo electric effect. Pay attention to stress.

(7) Latch up

Please pay attention to the deterioration and destruction by parasitic element action and latch up that occurs when excessive noise, surge on negative voltage is loaded at the normal operation.

(8) Test with set PCB

When you connect capacitor to low impedance terminal. You should discharge to avoid stress under IC. Also at attachment and detachment to jig in testing line, its power supply should be "OFF". Moreover for static electricity, please set ground to assembly line, and pong enough attention at conveyance on storage.

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