

DATA SHEET

74ALVC02

Quad 2-input NOR gate

Product specification
Supersedes data of 2003 Feb 05

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Philips
Semiconductors



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Quad 2-input NOR gate

74ALVC02

FEATURES

- Wide supply voltage range from 1.65 to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
JESD8-7 (1.65 to 1.95 V)
JESD8-5 (2.3 to 2.7 V)
JESD8B/JESD36 (2.7 to 3.6 V).
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.

DESCRIPTION

The 74ALVC02 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

The 74ALVC02 provides the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|--|--|---------|------|
| t_{PHL}/t_{PLH} | propagation delay nA, nB to nY | $V_{CC} = 1.8\text{ V}; C_L = 30\text{ pF}; R_L = 1\text{ k}\Omega$ | 2.8 | ns |
| | | $V_{CC} = 2.5\text{ V}; C_L = 30\text{ pF}; R_L = 500\text{ }\Omega$ | 2.0 | ns |
| | | $V_{CC} = 2.7\text{ V}; C_L = 50\text{ pF}; R_L = 500\text{ }\Omega$ | 2.5 | ns |
| | | $V_{CC} = 3.3\text{ V}; C_L = 50\text{ pF}; R_L = 500\text{ }\Omega$ | 2.2 | ns |
| C_I | input capacitance | | 3.5 | pF |
| C_{PD} | power dissipation capacitance per buffer | $V_{CC} = 3.3\text{ V}$; notes 1 and 2 | 32 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_I = \text{GND}$ to V_{CC} .

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ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | |
|-------------|-------------------|------|----------|----------|----------|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE |
| 74ALVC02D | -40 to +85 °C | 14 | SO14 | plastic | SOT108-1 |
| 74ALVC02PW | -40 to +85 °C | 14 | TSSOP14 | plastic | SOT402-1 |
| 74ALVC02BQ | -40 to +85 °C | 14 | DHVQFN14 | plastic | SOT762-1 |

FUNCTION TABLE

See note 1.

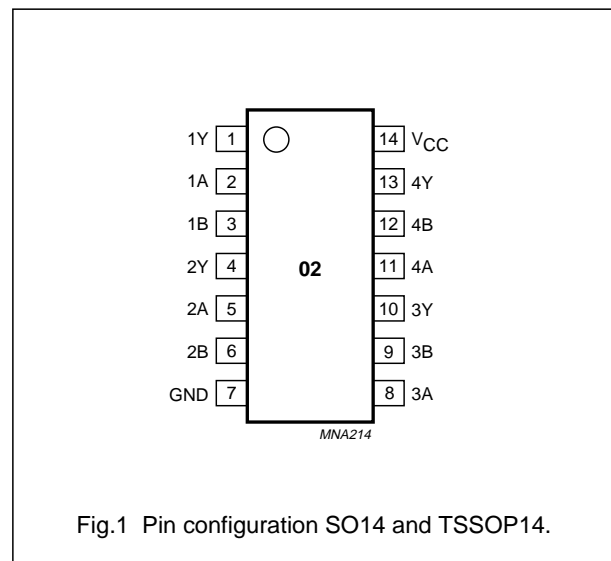
| INPUT | | OUTPUT |
|-------|----|--------|
| nA | nB | nY |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

Note

- H = HIGH voltage level;
L = LOW voltage level

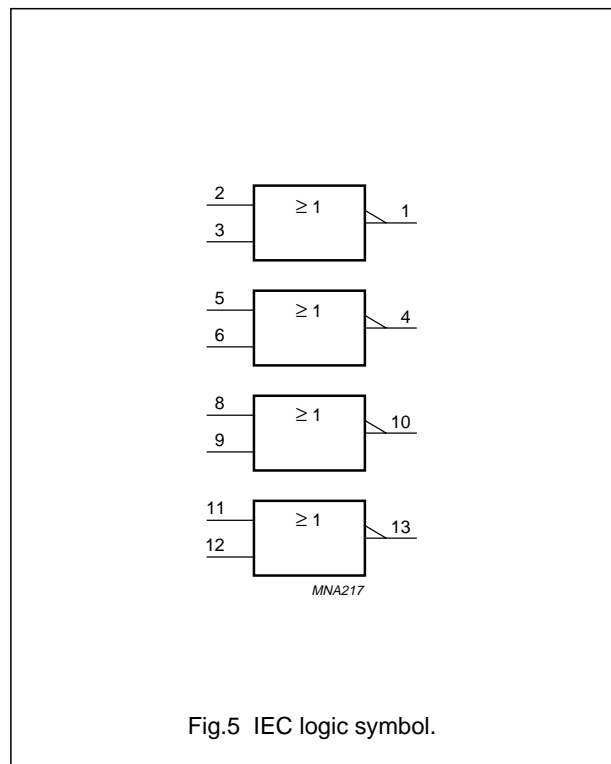
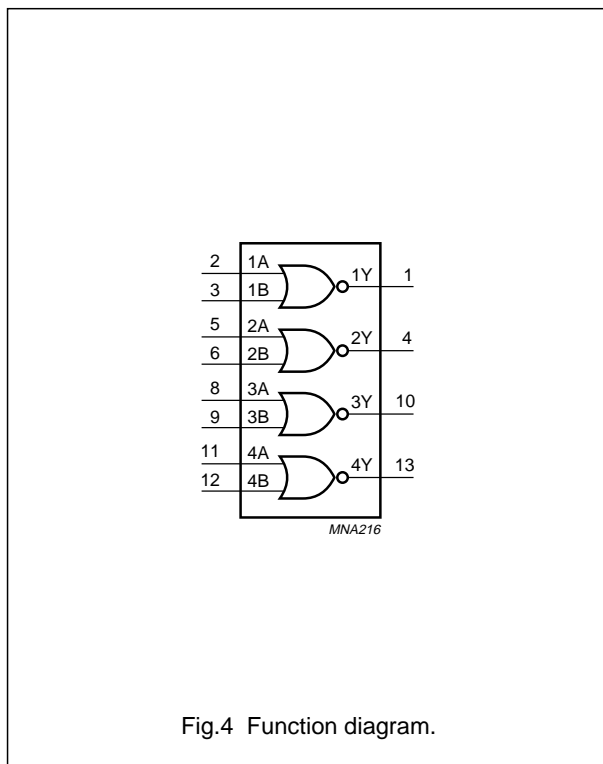
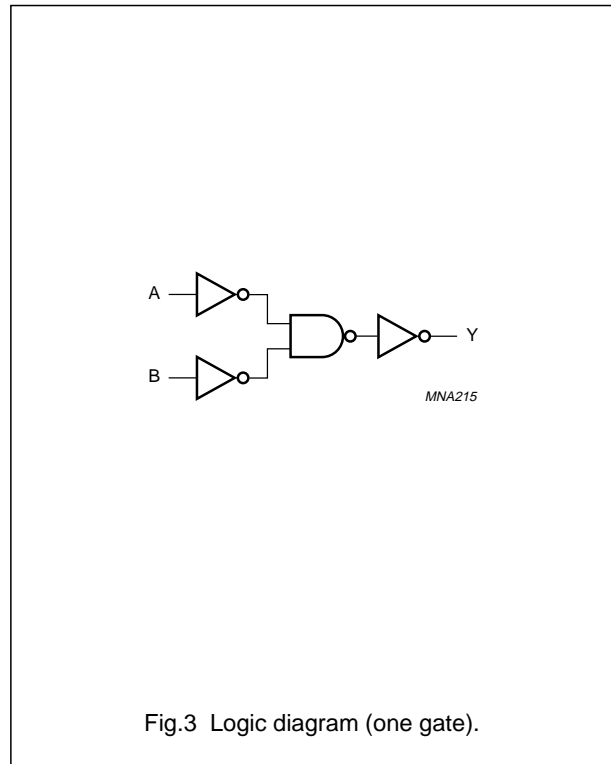
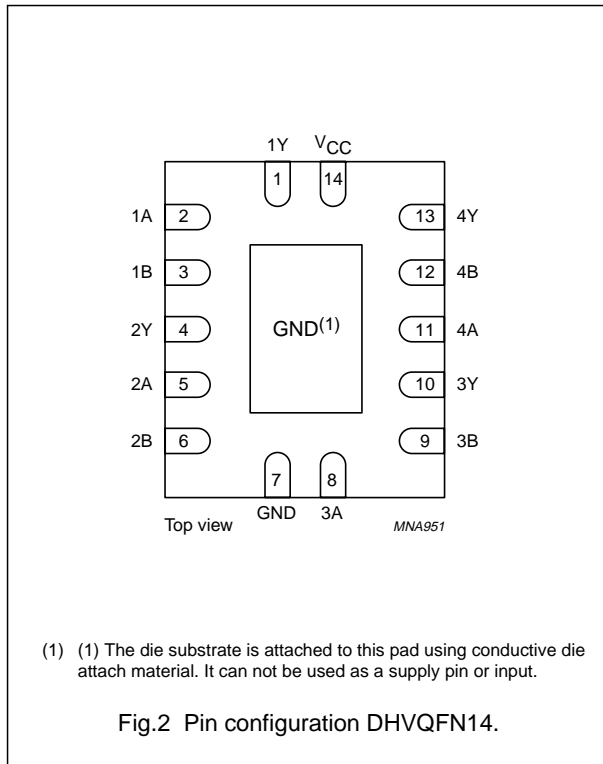
PINNING

| Pin | SYMBOL | DESCRIPTION |
|-----|-----------------|----------------|
| 1 | 1Y | data output |
| 2 | 1A | data input |
| 3 | 1B | data input |
| 4 | 2Y | data output |
| 5 | 2A | data input |
| 6 | 2B | data input |
| 7 | GND | ground (0 V) |
| 8 | 3A | data input |
| 9 | 3B | data input |
| 10 | 3Y | data output |
| 11 | 4A | data input |
| 12 | 4B | data input |
| 13 | 4Y | data output |
| 14 | V _{CC} | supply voltage |



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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------|-------------------------------|---------------------------------|------|----------|------|
| V_{CC} | supply voltage | | 1.65 | 3.6 | V |
| V_I | input voltage | | 0 | 3.6 | V |
| V_O | output voltage | $V_{CC} = 1.65$ to 3.6 V | 0 | V_{CC} | V |
| | | $V_{CC} = 0$ V; Power-down mode | 0 | 4.6 | V |
| T_{amb} | operating ambient temperature | | -40 | +85 | °C |
| t_r, t_f | input rise and fall times | $V_{CC} = 1.65$ to 2.7 V | 0 | 20 | ns/V |
| | | $V_{CC} = 2.7$ to 3.6 V | 0 | 10 | ns/V |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-------------------|-------------------------------|-------------------------------------|------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| I_{IK} | input diode current | $V_I < 0$ | - | -50 | mA |
| V_I | input voltage | | -0.5 | +4.6 | V |
| I_{OK} | output diode current | $V_O > V_{CC}$ or $V_O < 0$ | - | ± 50 | mA |
| V_O | output voltage | notes 1 and 2 | -0.5 | $V_{CC} + 0.5$ | V |
| | | Power-down mode; note 2 | -0.5 | +4.6 | V |
| I_O | output source or sink current | $V_O = 0$ to V_{CC} | - | ± 50 | mA |
| I_{CC}, I_{GND} | V_{CC} or GND current | | - | ± 100 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | power dissipation | $T_{amb} = -40$ to $+85$ °C; note 3 | - | 500 | mW |

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 3.6 V in normal operation.
- For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. ⁽¹⁾ | MAX. | UNIT |
|--|---|--|---------------------|------------------------|---------------------|------------------------|------|
| | | OTHER | V _{CC} (V) | | | | |
| T_{amb} = -40 to +85 °C | | | | | | | |
| V _{IH} | HIGH-level input voltage | | 1.65 to 1.95 | 0.65 × V _{CC} | – | – | V |
| | | | 2.3 to 2.7 | 1.7 | – | – | V |
| | | | 2.7 to 3.6 | 2 | – | – | V |
| V _{IL} | LOW-level input voltage | | 1.65 to 1.95 | – | – | 0.35 × V _{CC} | V |
| | | | 2.3 to 2.7 | – | – | 0.7 | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | 1.65 to 3.6 | – | – | 0.2 | V |
| | | I _O = 100 μA | 1.65 | – | 0.11 | 0.3 | V |
| | | I _O = 6 mA | 2.3 | – | 0.17 | 0.4 | V |
| | | I _O = 12 mA | 2.3 | – | 0.25 | 0.6 | V |
| | | I _O = 18 mA | 2.7 | – | 0.16 | 0.4 | V |
| | | I _O = 12 mA | 3.0 | – | 0.23 | 0.4 | V |
| | | I _O = 18 mA | 3.0 | – | 0.30 | 0.55 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | 1.65 to 3.6 | V _{CC} – 0.2 | – | – | V |
| | | I _O = –100 μA | 1.65 | 1.25 | 1.51 | – | V |
| | | I _O = –6 mA | 2.3 | 1.8 | 2.10 | – | V |
| | | I _O = –12 mA | 2.3 | 1.7 | 2.01 | – | V |
| | | I _O = –18 mA | 2.7 | 2.2 | 2.53 | – | V |
| | | I _O = –12 mA | 3.0 | 2.4 | 2.76 | – | V |
| | | I _O = –18 mA | 3.0 | 2.2 | 2.68 | – | V |
| I _{LI} | input leakage current | V _I = 3.6 V or GND | 3.6 | – | ±0.1 | ±5 | μA |
| I _{off} | power OFF leakage current | V _I or V _O = 3.6 V | 0.0 | – | ±0.1 | ±10 | μA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 | 3.6 | – | 0.2 | 20 | μA |
| ΔI _{CC} | additional quiescent supply current per input pin | V _I = V _{CC} – 0.6 V; I _O = 0 | 3.0 to 3.6 | – | 5 | 750 | μA |

Note1. All typical values are measured at T_{amb} = 25 °C.

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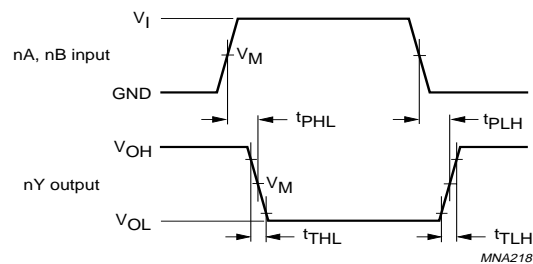
AC CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. ⁽¹⁾ | MAX. | UNIT |
|--|-----------------------------------|------------------|---------------------|------|---------------------|------|------|
| | | WAVEFORMS | V _{CC} (V) | | | | |
| T_{amb} = -40 to +85 °C | | | | | | | |
| t _{PHL} /t _{PLH} | propagation delay nA, nB to nY | see Figs 6 and 7 | 1.65 to 1.95 | 1.0 | 2.8 | 4.7 | ns |
| | | | 2.3 to 2.7 | 1.0 | 2.0 | 3.1 | ns |
| | | | 2.7 | 1.0 | 2.5 | 2.9 | ns |
| | | | 3.0 to 3.6 | 1.0 | 2.2 | 2.8 | ns |

Note

- All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS

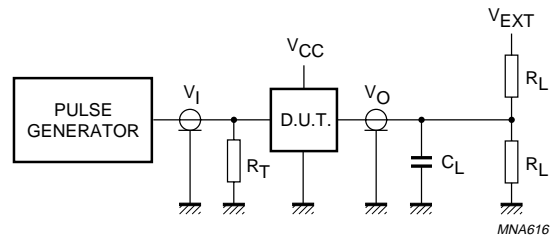


| V _{CC} | V _M | INPUT | |
|-----------------|-----------------------|-----------------|---------------------------------|
| | | V _I | t _r = t _f |
| 1.65 to 1.95 V | 0.5 × V _{CC} | V _{CC} | ≤ 2.0 ns |
| 2.3 to 2.7 V | 0.5 × V _{CC} | V _{CC} | ≤ 2.0 ns |
| 2.7 V | 1.5 V | 2.7 V | ≤ 2.5 ns |
| 3.0 to 3.6 V | 1.5 V | 2.7 V | ≤ 2.5 ns |

Fig.6 Inputs nA, nB to output nY propagation delay times.

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| V_{CC} | V_I | C_L | R_L | V_{EXT} | | |
|----------------|----------|-------|--------------|-------------------|-------------------|-------------------|
| | | | | t_{PLH}/t_{PHL} | t_{PZH}/t_{PHZ} | t_{PZL}/t_{PLZ} |
| 1.65 to 1.95 V | V_{CC} | 30 pF | 1 k Ω | open | GND | $2 \times V_{CC}$ |
| 2.3 to 2.7 V | V_{CC} | 30 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |
| 2.7 V | 2.7 V | 50 pF | 500 Ω | open | GND | 6 V |
| 3.0 to 3.6 V | 2.7 V | 50 pF | 500 Ω | open | GND | 6 V |

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

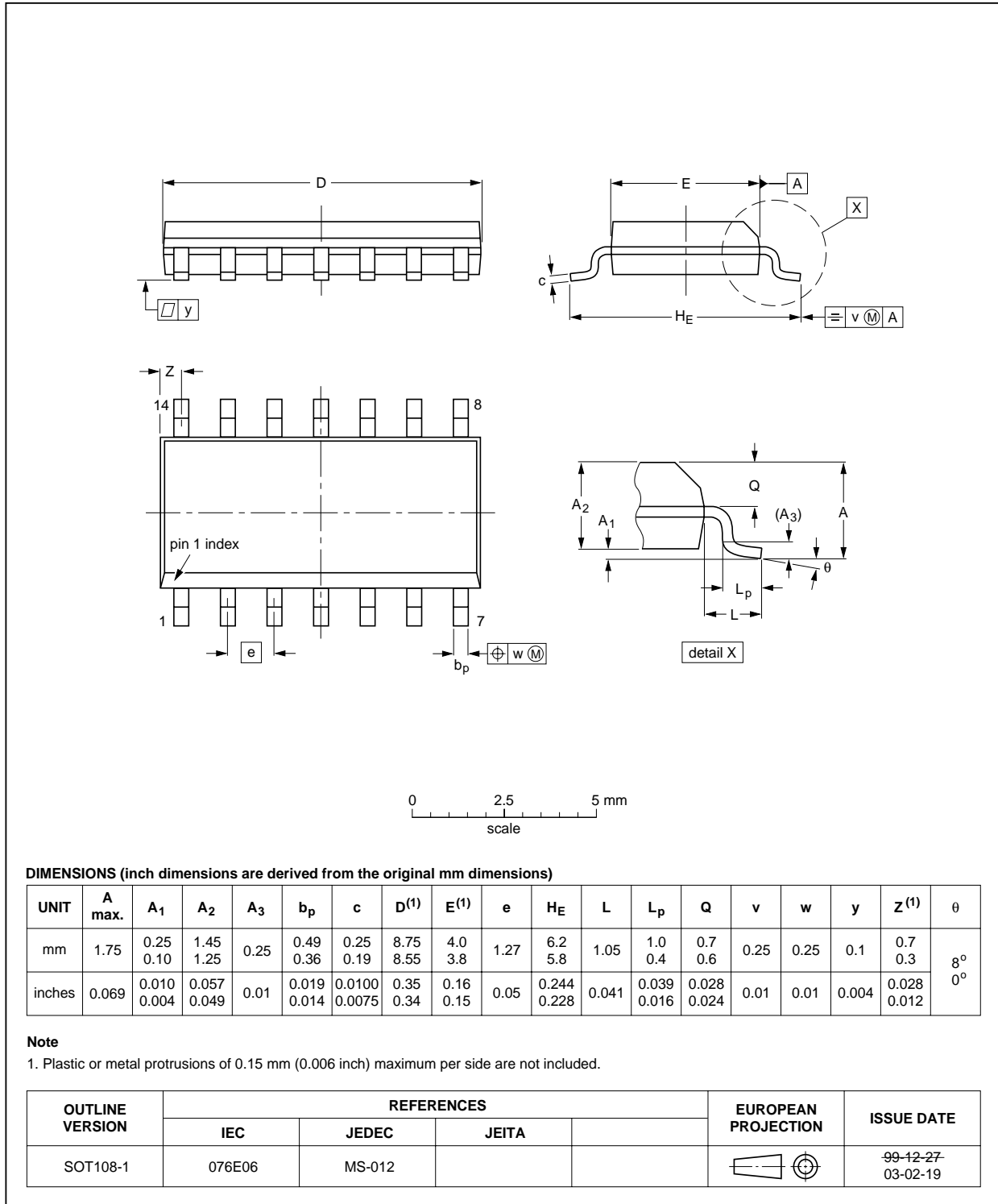
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PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

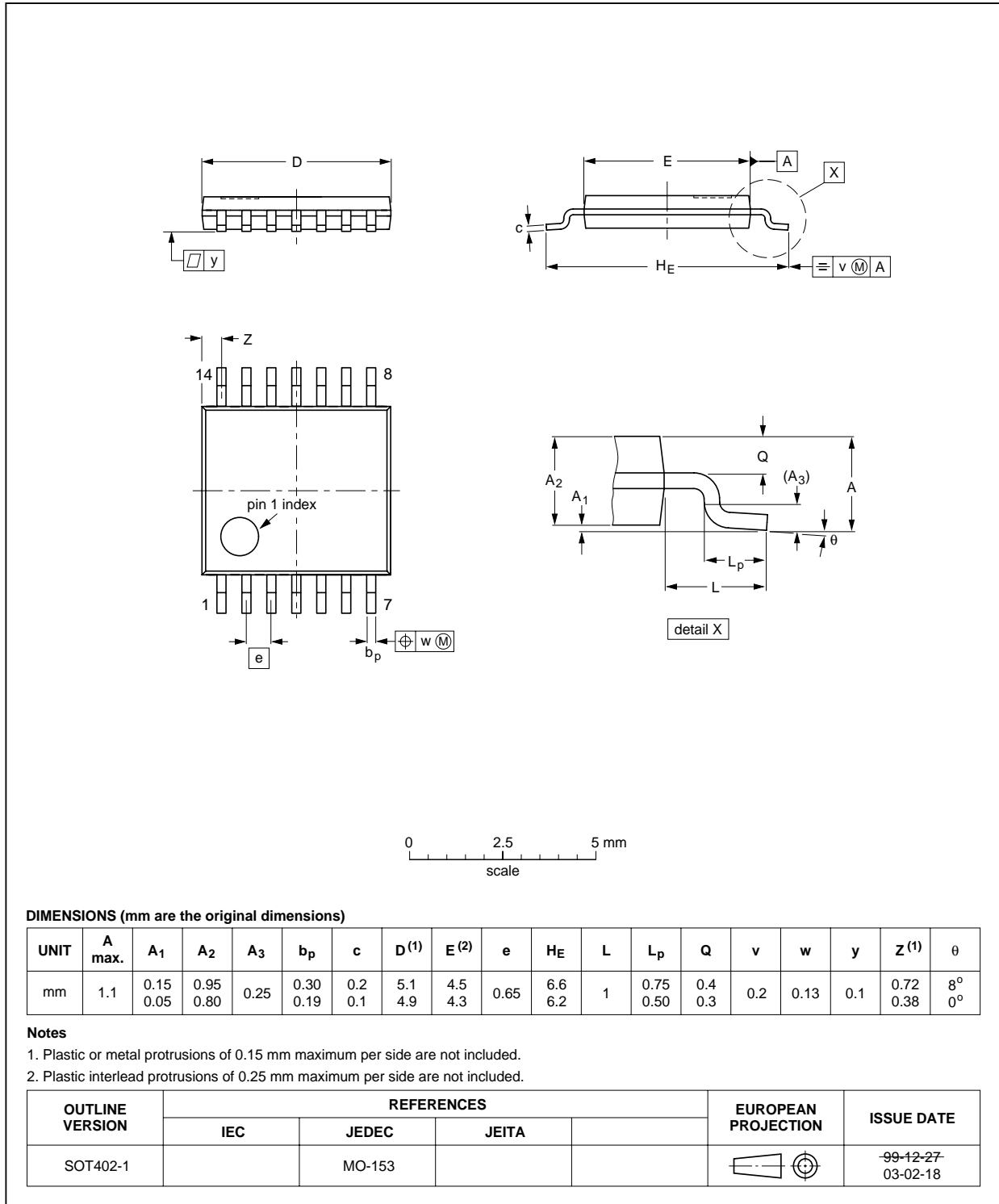


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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

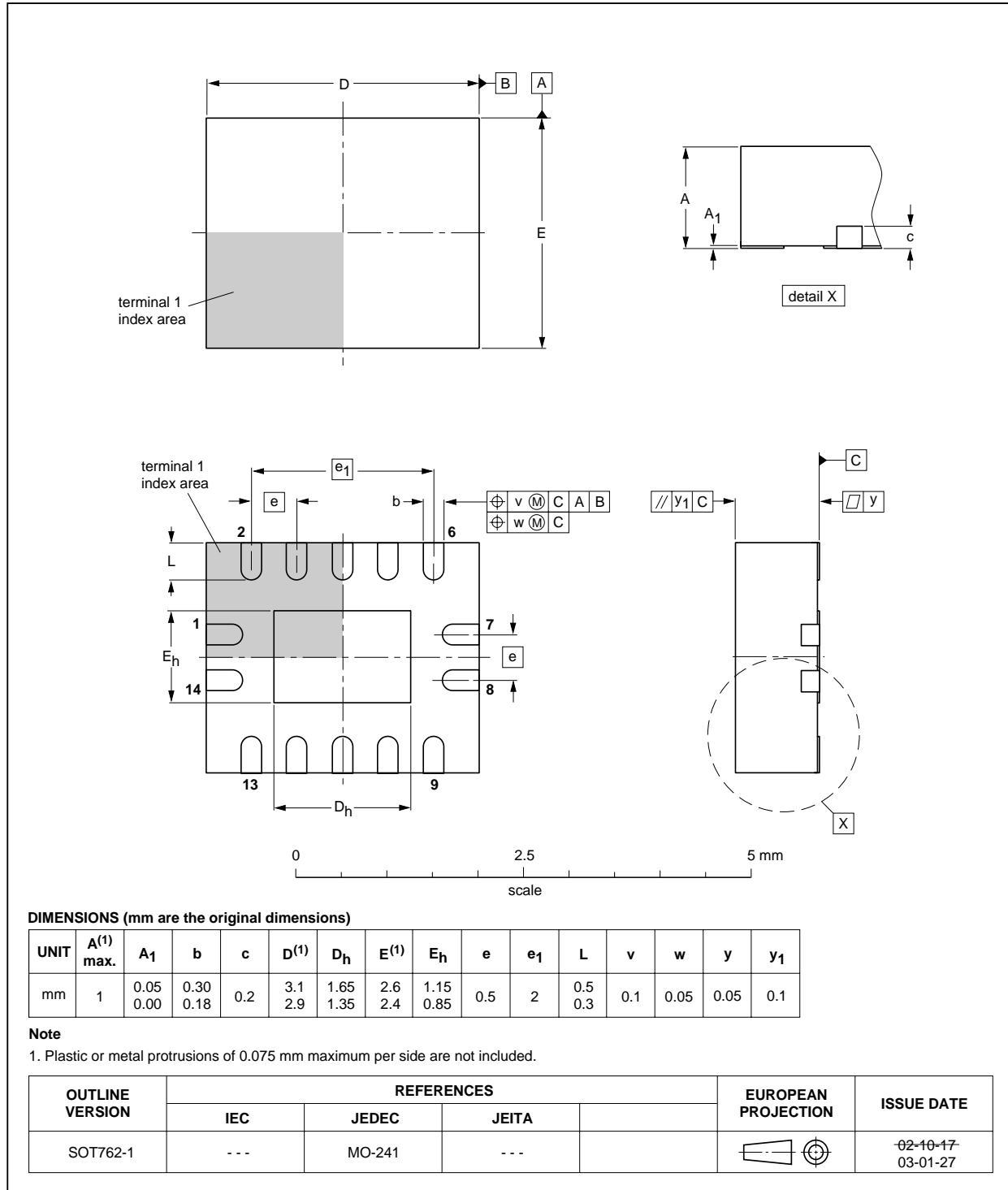


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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



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DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾⁽³⁾ | DEFINITION |
|-------|----------------------------------|----------------------------------|--|
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