NC7SZ27 TinyLogic® UHS 3-Input NOR Gate

FAIRCHILD

SEMICONDUCTOR

NC7SZ27 TinyLogic® UHS 3-Input NOR Gate

General Description

The NC7SZ27 is a single 3-Input NOR Gate from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

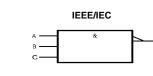
Features

- Space saving SC70 6-lead package
- Ultra small MicroPak[™] leadless package
- Ultra High Speed: t_{PD} 2.4 ns typ into 50 pF at 5V V_{CC}
- High Output Drive: ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V–5.5V
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Logic Symbol

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ27P6X	MAA06A	Z27	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ27L6X	MAC06A	E9	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel



Pin Descriptions

Pin Names	Description
A, B, C	Inputs
Y	Output

С

Х

Х

н

I.

γ

L

L

L

н

Function Table

Δ

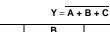
Н

Х

Х

I.

H = HIGH Logic Level L = LOW Logic Level X = Don't Care

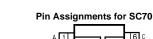


Х

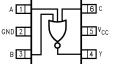
Н

Х

I.



Connection Diagrams

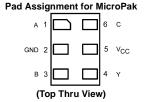


(Top View)

Pin One Orientation Diagram



AAA represents Product Code Top Mark -see ordering code Note: Orientation of Top Mark determines Pin One location. Read the Top Product Code Mark left to right, Pin One is the lower left pin (see diagram)



TinyLogic® is a registered trademark of Fairchild Semiconductor Corporation. MIcroPak™ is a trademark of Fairchild Semiconductor Corporation.

© 2004 Fairchild Semiconductor Corporation DS500466

www.fairchildsemi.com

Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Voltage (V _{IN})	-0.5V to +7.0V
DC Output Voltage (V _{OUT})	-0.5V to +7.0V
DC Input Diode Current (IIK)	
@ V _{IN} < -0.5V	–50 mA
@ V _{IN} > 6V	+20 mA
DC Output Diode Current (I _{OK})	
@ V _{OUT} < -0.5V	–50 mA
@ $V_{OUT} > 6V$, $V_{CC} = GND$	+20 mA
DC Output Current (I _{OUT})	± 50 mA
DC V _{CC} /GND Current (I _{CC} /I _{GND})	± 50 mA
Storage Temperature (T _{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (TL);	
(Soldering, 10 seconds)	260°C
Power Dissipation (P _D) @ +85°C	
SC70-5	150 mW

Recommended Operating Conditions (Note 2)

· · · · ·	
Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V _{IN})	0V to 5.5V
Output Voltage (V _{OUT})	0V to V_{CC}
Operating Temperature (T _A)	$-40^\circ C$ to $+85^\circ C$
Input Rise and Fall Time (t_r, t_f)	
V _{CC} @ 1.8V, 2.5V ±0.2V	0 ns/V to 20 ns/V
$V_{CC} @ 3.3V \pm 0.3V$	0 ns/V to 10 ns/V
$V_{CC} @ 5.0V \pm 0.5V$	0 ns to 5 ns/V
Thermal Resistance (θ_{JA})	
SC70-5	425°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter HIGH Level Input Voltage	V_{CC} $T_A = +25^{\circ}C$		$T_A=-40^\circ C$ to $+85^\circ C$		Units	Conditions			
Symbol		(V)	Min	Тур	Max	Min	Max	Units	Conditions	
VIH		1.8 ± 0.15	0.75V _{CC}		0.75V _{CC}		V			
		2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		v		
V _{IL}	LOW Level Input Voltage	1.8 ± 0.15			0.25V _{CC}		0.25V _{CC}	V		
		2.3 to 5.5			0.3 V _{CC}		0.3 V _{CC}	v		
V _{OH}	HIGH Level Output Voltage	1.65	1.55	1.65		1.55				
		2.3	2.2	2.3		2.2			V – V	I _{OH} =-100μΑ
		3.0	2.9	3.0		2.9			$V_{IN} = V_{IL}$ $I_{OH} = -$	10H=-100HA
		4.5	4.4	4.5		4.4				
		1.65	1.29	1.52		1.29		V		$I_{OH}=-4mA$
		2.3	1.9	2.15		1.9				$I_{OH} = -8mA$
		3.0	2.4	2.80		2.4				I _{OH} =-16mA
		3.0	2.3	2.68		2.3				I _{OH} =-24mA
		4.5	3.8	4.20		3.8				I _{OH} =-32mA
V _{OL}	LOW Level Output Voltage	1.65		0.0	0.1		0.1		V _{IN} =V _{IH} I _{OL} =10	
		2.3		0.0	0.1		0.1			I _{OL} =100μA
		3.0		0.0	0.1		0.1		VIN-VIH	
		4.5		0.0	0.1		0.1			
		1.65		0.08	0.24		0.24	V		I _{OL} = 4mA
		2.3		0.10	0.3		0.3			I _{OL} = 8mA
		3.0		0.15	0.4		0.4			I _{OL} =16mA
		3.0		0.22	0.55		0.55			I _{OL} =24mA
		4.5		0.22	0.55		0.55			I _{OL} =32mA
I _{IN}	Input Leakage Current	0 to 5.5			±1		±10	μA	$V_{IN} = 5.5V,$	ĠND
I _{OFF}	Power Off Leakage Current	0.0			1		10	μA	V_{IN} or V_{OU}	= 5.5V
I _{CC}	Quiescent Supply Current	1.65 to 5.5			2.0		20	μA	V _{IN} = 5.5V,	GND

www.fairchildsemi.com

Symbol	Parameter	V _{cc}	V_{CC} $T_A = +25^{\circ}C$			$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	Figure
		(V)	Min	Тур	Max	Min	Max	Units	Conditions	Number
t _{PLH} ,	Propagation Delay	1.8 ± 0.15	2.0	10.0	18.5	2.0	19.0			
t _{PHL}		2.5 ± 0.2	0.8	5.0	10.5	0.8	11.0	ns	C _L = 15 pF,	Figures
		3.3 ± 0.3	0.5	3.2	8.0	0.5	8.5	115	$R_L = 1 M\Omega$	1, 3
		5.0 ± 0.5	0.5	2.6	5.5	0.5	6.0			
t _{PLH,}	Propagation Delay	3.3 ± 0.3	1.5	3.9	8.0	1.5	8.5	ns	C _L = 50 pF, Figure	Figures
t _{PHL}		5.0 ± 0.5	0.8	2.9	5.5	0.8	6.0		$R_L = 500\Omega$	1, 3
CIN	Input Capacitance	0		4				pF		
C _{PD}	Power Dissipation	3.3		23					(1)-(-0)	Figure 0
	Capacitance	5.0		30				pF	(Note 3)	Figure 2

t_r = 3 ns ·

10%

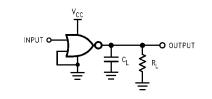
INPUT

OUTPUT

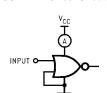
3

loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC} static).$

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz; t_w = 500 ns $\mbox{FIGURE 1. AC Test Circuit}$



Input = AC Waveform; $t_r = t_f = 1.8$ ns; PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

www.fairchildsemi.com

 $t_f = 3 \text{ ns}$

-10%

t_{PLH}

50%

90%

50%

90%

50%

 $\mathsf{t}_{\mathsf{PHL}}$

50%

FIGURE 3. AC Waveforms

-

V_{CC}

GND

√он

V_{OL}

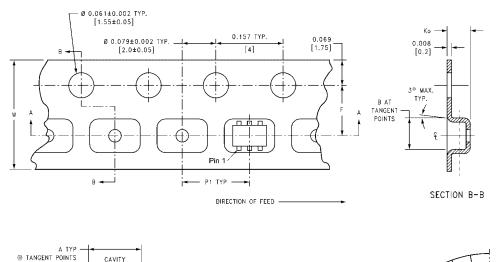


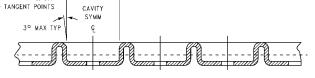
Tape and Reel Specification

TAPE FORMAT for SC70

Package	Tape	Number	Cavity	Cover Tene
Fackage	Tape	Number	Cavity	Cover Tape
Designator	Section	Cavities	Status	Status
	Leader (Start End)	125 (typ)	Empty	Sealed
P6X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)





SECTION A-A

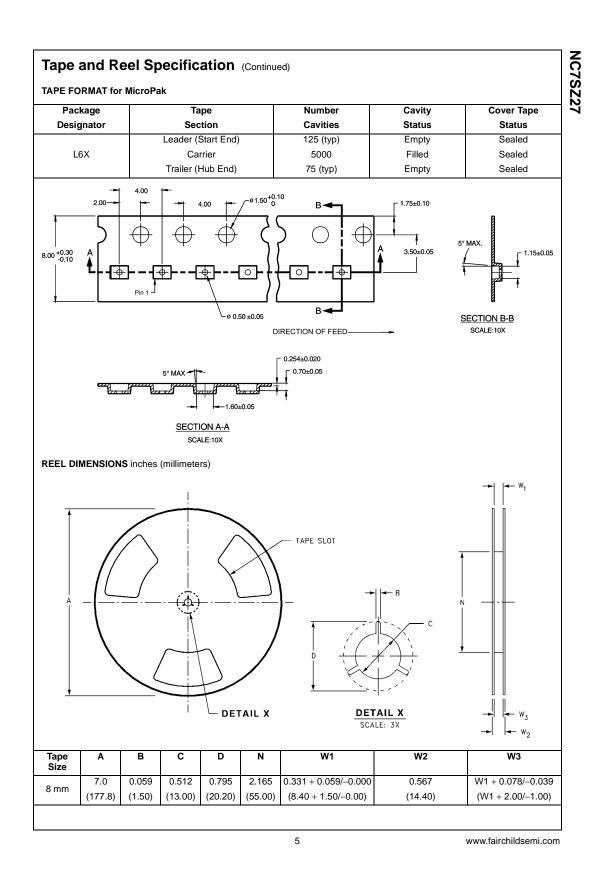


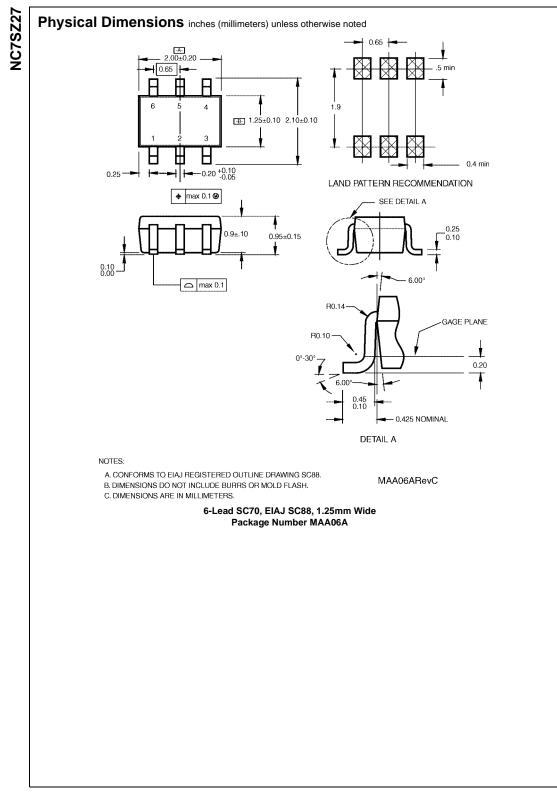
BEND RADIUS NOT TO SCALE

Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-6	8 mm	0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004
	0 11111	(2.35)	(2.45)	(3.5 ± 0.10)	(1.35 ± 0.10)	(4)	(8 ± 0.1)
			•				•

www.fairchildsemi.com

4





www.fairchildsemi.com

6

