National Semiconductor

November 12, 2008

# LM48100Q Boomer® Audio Power Amplifier Series
# Mono, 1.3W Audio Power Amplifier with Output Fault Detection and Volume Control

## General Description

The LM48100Q is a single supply, mono, bridge-tied load amplifier with I²C volume control, ideal for automotive applications. A comprehensive output fault detection system senses the load conditions, protecting the device during short circuit events, as well as detecting open circuit conditions.

Operating from a single 5V supply, the LM48100Q delivers 1.3W of continuous output power to an 8Ω load with < 1% THD+N. Flexible power supply requirements allow operation from 3.0V to 5.5V. High power supply rejection ratio (PSRR), 74dB at 1kHz, allows the device to operate in noisy environments without additional power supply conditioning.

The LM48100Q features dual audio inputs that can be mixed/multiplexed to the device output. Each input path has its own independent, 32-step volume control. The mixer, volume control and device mode select are controlled through an I²C compatible interface. An open drain $\overline{\text{FAULT}}$ output indicates when a fault has occurred. Comprehensive output short circuit and thermal overload protection prevent the device from being damaged during a fault condition.

A low power shutdown mode reduces supply current consumption to 0.01µA. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48100Q is available in an 14-pin TSSOP package

## Key Specifications

- Output Power at $V_{DD}$ = 5V, $R_L$ = 8Ω, THD+N ≤ 1% — 1.3W (typ)
- Quiescent Power Supply Current at 5V — 6mA (typ)
- PSRR at 1kHz — 74dB (typ)
- Shutdown current — 0.01µA (typ)

## Features

- Output Fault Detection
- I²C Volume and Mode Control
- Input Mixer/Multiplexer
- High PSRR
- Individual 32-Step Volume Control
- Short Circuit and Thermal Protection
- Advanced Click-and-Pop Suppression
- Low Power Shutdown Mode
- Available in 14-pin TSSOP Package

## Applications

- Automotive Instrument Clusters
- Hands-free Car Kits
- Medical

Boomer® is a registered trademark of National Semiconductor Corporation.

## Typical Application

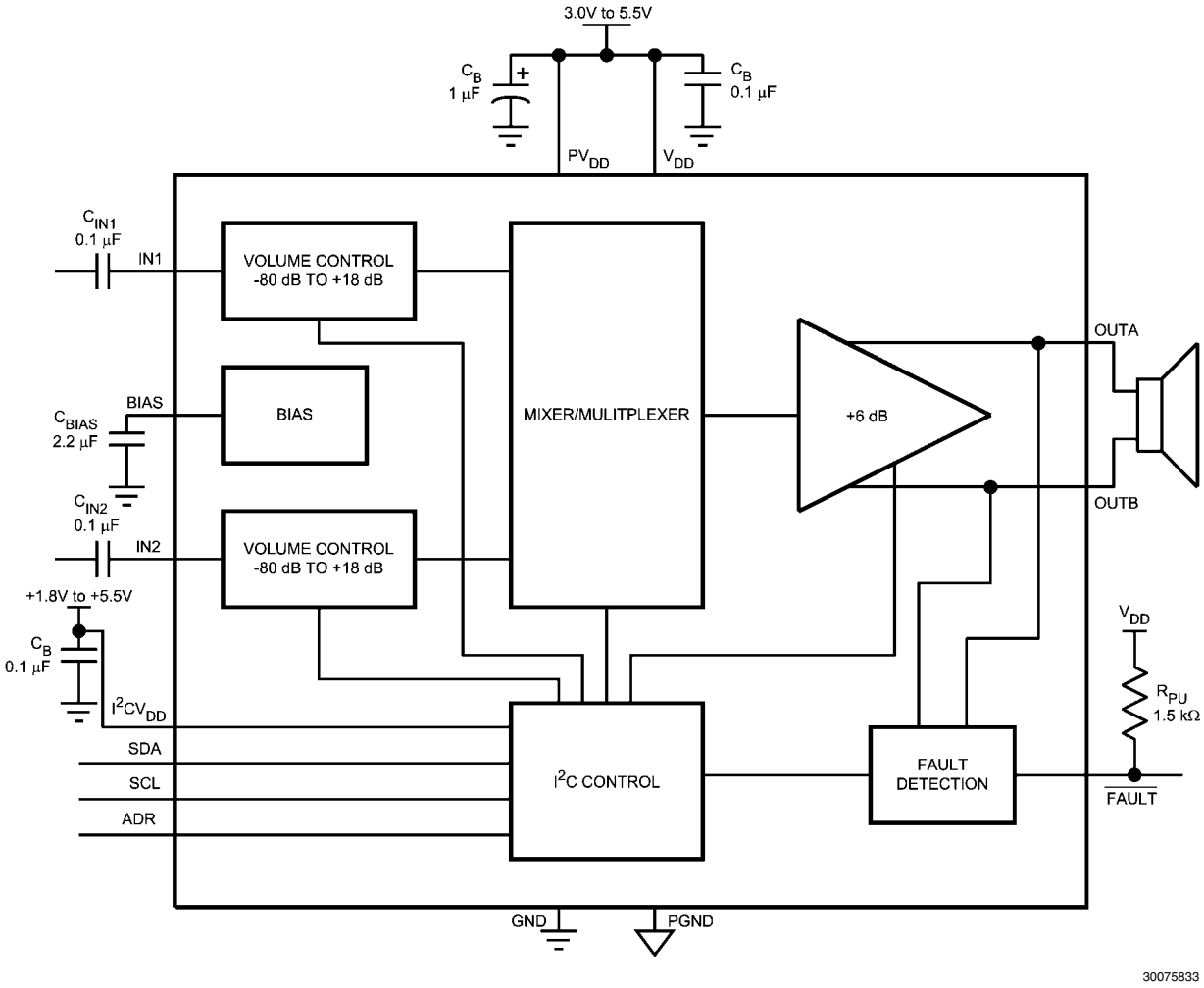
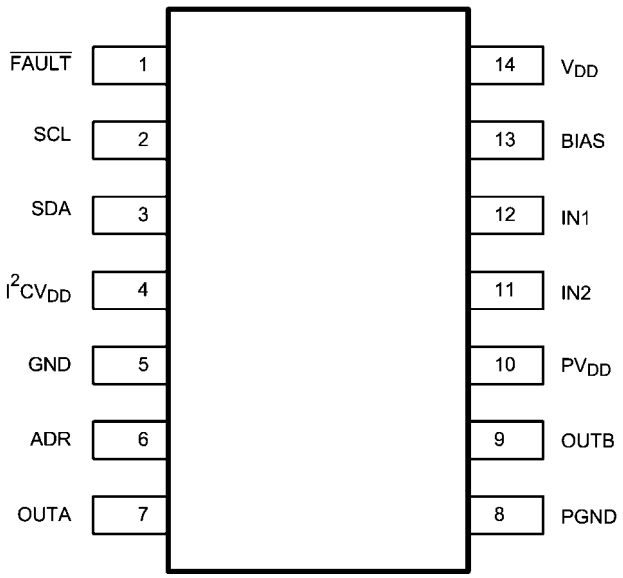



**FIGURE 1. Typical Audio Amplifier Application Circuit**

## Connection Diagrams

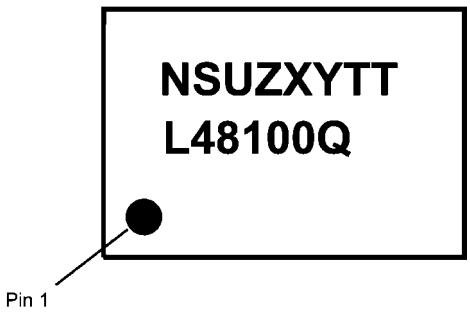
**TSSOP Package**




30075834

**Top View**
**Order Number LM48100QMH**
**See NS Package Number MXA14A**

**TSSOP Marking**




30075842

**Top View**
**NS – Standard National logo**
**U – Wafer Fab code**
**Z – Assembly plant code**
**XY – 2 digit date code**
**TT – Die traceability**
**L48100Q – LM48100QMH**

## Ordering Information

| Order Number | Package | Package DWG # | Transport Media | MSL Level | Green Status | Features |
|---|---|---|---|---|---|---|
| LM48100QMHE | 14–Lead TSSOP Exposed Pad | MXA14A | 250 units on tape and reel | 1 | NOPB | AECQ-100 grade 2 |
| LM48100QMH | 14–Lead TSSOP Exposed Pad | MXA14A | 1000 units in rails | 1 | NOPB | AECQ-100 grade 2 |
| LM48100QMHX | 14–Lead TSSOP Exposed Pad | MXA14A | 2500 units on tape and reel | 1 | NOPB | AECQ-100 grade 2 |

## Bump Descriptions

| Pin | Pin Name | Description |
|---|---|---|
| 1 | $\overline{\text{FAULT}}$ | Open-Drain output fault flag. $\overline{\text{FAULT}}$ = 0 indicates that a fault condition has occurred. |
| 2 | SCL | I²C Clock Input |
| 3 | SDA | I²C Serial Data Input |
| 4 | $I^2CV_{DD}$ | I²C Interface Power Supply |
| 5 | GND | Ground |
| 6 | ADR | I²C Address Bit. Connect to $I^2CV_{DD}$ to set address bit, B1 = 1. Connect to GND to set address bit B1 = 0 |
| 7 | OUTA | Non-Inverting Audio Output |
| 8 | PGND | Power Ground |
| 9 | OUTB | Inverting Audio Output |
| 10 | $PV_{DD}$ | Output Amplifier Power Supply |
| 11 | IN2 | Audio Input 2 |
| 12 | IN1 | Audio Input 1 |
| 13 | BIAS | Bias Bypass |
| 14 | $V_{DD}$ | Power Supply |
| — | Exposed Pad | Exposed paddle. Connect to GND. |

## Absolute Maximum Ratings (Notes 1, 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, continuous (Note 1) | 6V |
| Storage Temperature | −65°C to +150°C |
| Input Voltage | −0.3V to $V_{DD}$ + 0.3V |
| Power Dissipation (Note 3) | Internally Limited |
| ESD Rating (Note 4) | 2500V |
| ESD Rating (Note 5) | 300V |
| Junction Temperature | 150°C |
| Thermal Resistance | |
| $\theta_{JA}$ (Note 6) | 37.8°C/W |
| $\theta_{JC}$ | 5.2°C/W |
| Lead Temperature (Soldering 4 sec) | 260°C |

For detailed information on soldering plastic TSSOP and LLP packages, refer to the Packaging Data Book available from National Semiconductor Corporation.

## Operating Ratings (Notes 1, 2)

| | |
|---|---|
| Temperature Range | |
| $T_{MIN} \le T_A \le T_{MAX}$ | $-40°C \le T_A \le +105°C$ |
| Supply Voltage | |
| $V_{DD}$ and $PV_{DD}$ | $3.0V \le V_{DD} \le 5.5V$ |
| I²C Supply Voltage | |
| $I^2CV_{DD}$ | $1.8V \le I^2CV_{DD} \le 5.5V$ |
| | $I^2CV_{DD} \le V_{DD}$ |

## Audio Amplifier Electrical Characteristics $V_{DD}$ = 5.0V (Notes 1, 2)

The following specifications apply for Programmable Gain = 0dB, $R_L$ = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for $T_A$ = 25°C.

| Symbol | Parameter | Conditions | LM48100Q | | | Units (Limits) |
|---|---|---|---|---|---|---|
| | | | Typical (Note 7) | Room Temp Limits (Note 8) | Extended Temp Limits (Notes 8, 9) | |
| $I_{DD}$ | Quiescent Power Supply Current | $V_{IN}$ = 0V, Both channels active<br>$R_L$ = 8Ω<br>$R_L$ = ∞ | <br>4.4<br>4.2 | <br>9<br>6 | <br>10.8<br>7.9 | <br>mA (max)<br>mA (max) |
| $I_{DD}$ | Diagnostic Mode Quiescent Power Supply Current | Diagnostic Mode Enabled, $R_L$ = ∞ | 12.5 | 14.5 | | mA (max) |
| $I_{SD}$ | Shutdown Current | Shutdown Enabled | 0.01 | 1 | | µA (max) |
| $V_{OS}$ | Differential Output Offset Voltage | $V_{IN}$ = 0V, $R_L$ = 8Ω | 8.8 | 50 | 75 | mV (max) |
| $T_{WU}$ | Wake-Up Time | Time from shutdown to audio available | 11.6 | 50 | | ms (max) |
| $A_V$ | Gain | Minimum Gain Setting | −54 | ±1.0 | ±2.0 | dB (max)<br>dB (min) |
| | | Maximum Gain Setting | 18 | ±1.0 | ±1.0 | dB (max)<br>dB (min) |
| Mute | Mute Attenuation | | −80 | −77 | −74 | dB (max) |
| $R_{IN}$ | Input Resistance | $A_V$ = 18dB | 12.5 | 11.5<br>13.5 | | kΩ (min)<br>kΩ (max) |
| | | $A_V$ = −54dB | 110 | 98<br>120 | 89<br>130 | kΩ (min)<br>kΩ (max) |
| $P_O$ | Output Power | $R_L$ = 8Ω, f = 1kHz<br>THD+N = 10%<br>THD+N = 1% | <br>1.6<br>1.3 | <br><br>1.05 | <br><br>0.96 | <br>W<br>W (min) |
| THD+N | Total Harmonic Distortion + Noise | $P_O$ = 850mW, f = 1kHz, $R_L$ = 8Ω | 0.04 | | | % |
| PSRR | Power Supply Rejection Ratio | $V_{RIPPLE}$ = 200m$V_{P-P}$ Sine, Inputs AC GND, $C_{IN\_}$ = 1µF, input referred, $C_{BIAS}$ = 2.2µF | | | | |
| | | f = 217Hz<br>f = 1kHz | 79<br>74 | 66 | 63 | dB (min)<br>dB |
| SNR | Signal-to-Noise-Ratio | $P_{OUT}$ = TBDmW, f = 1kHz | 104 | | | dB |
| $\in_{OS}$ | Output Noise | $A_V$ = 0dB, A-weighted Filter | 12 | | | µV |
| $I_{OUT(\overline{FAULT})}$ | $\overline{FAULT}$ Output Current | $\overline{FAULT}$ = 0, $V_{OUT(\overline{FAULT})}$ = 0.4V | 3 | | | mA |

| Symbol | Parameter | Conditions | LM48100Q | | | Units (Limits) |
|---|---|---|---|---|---|---|
| | | | Typical (Note 7) | Room Temp Limits (Note 8) | Extended Temp Limits (Notes 8, 9) | |
| $R_{FAULT}$ | Output to Supply Short Circuit Detection Threshold | Short between either OUTA to $V_{DD}$ or GND, or OUTB to $V_{DD}$ or GND<br>Short Circuit<br>Open Circuit | | <br>3<br>7.5 | <br>3<br>7.5 | <br>kΩ (min)<br>kΩ (max) |
| $R_{FAULT}$ | Output to Supply Short Circuit Detection Threshold | Short between both OUTA and OUTB to $V_{DD}$ or GND<br>Short Circuit<br>Open Circuit | | <br>6<br>15 | | <br>kΩ (min)<br>kΩ (max) |
| $R_{OPEN}$ | Open Circuit Detection Threshold | Open circuit between OUTA and OUTB | | 100<br>200 | | Ω (min)<br>Ω (max) |
| $R_{SHT}$ | Output to Output Short Circuit Detection Threshold | Short circuit between OUTA and OUTB | | 2<br>6 | | Ω (min)<br>Ω (max) |
| $I_{SHTCKT}$ | Short Circuit Current Limit | | 1.47 | 1.67 | 2 | A (max) |
| $T_{SD}$ | Thermal Shutdown Threshold | | 170 | | | °C |
| $t_{DIAG}$ | Diagnostic Time | | 58 | | | ms |

## Audio Amplifier Electrical Characteristics $V_{DD}$ = 3.6V (Notes 1, 2)

The following specifications apply for Programmable Gain = 0dB, $R_L$ = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for $T_A$ = 25°C.

| Symbol | Parameter | Conditions | LM48100Q | | | Units (Limits) |
|---|---|---|---|---|---|---|
| | | | Typical (Note 7) | Room Temp Limits (Note 8) | Extended Temp Limits (Notes 8, 9) | |
| $I_{DD}$ | Quiescent Power Supply Current | $V_{IN}$ = 0V, Both channels active<br>$R_L$ = 8Ω<br>$R_L$ = ∞ | <br>3.8<br>3.6 | <br>8.5<br>5 | <br>10.8<br>7 | <br>mA (max)<br>mA (max) |
| $I_{DD}$ | Diagnostic Mode Quiescent Power Supply Current | Diagnostic Mode Enabled | 11.7 | 14.5 | | mA (max) |
| $I_{SD}$ | Shutdown Current | Shutdown Enabled | 0.01 | 1 | | µA (max) |
| $V_{OS}$ | Differential Output Offset Voltage | $V_{IN}$ = 0V, $R_L$ = 8Ω | 8.8 | 50 | 76 | mV (max) |
| $T_{WU}$ | Wake-Up Time | Time from shutdown to audio available | 11.5 | 50 | | ms (max) |
| $A_V$ | Gain | Minimum Gain Setting | –54 | ±1 | | dB (max)<br>dB (min) |
| | | Maximum Gain Setting | 18 | ±1 | | dB (max)<br>dB (min) |
| Mute | Mute Attenuation | | –79 | –77 | | dB (max) |
| $R_{IN}$ | Input Resistance | $A_V$ = 18dB | 12.5 | 11.5<br>13.5 | | kΩ (min)<br>kΩ (max) |
| | | $A_V$ = –54dB | 110 | 98<br>120 | 89<br>135 | kΩ (min)<br>kΩ (max) |
| $P_O$ | Output Power | $R_L$ = 8Ω, f = 1kHz<br>THD+N = 10%<br>THD+N = 1% | <br>820<br>660 | <br><br>480 | <br><br> | <br>mW<br>mW (min) |
| THD+N | Total Harmonic Distortion + Noise | $P_O$ = 400mW, f = 1kHz, $R_L$ = 8Ω | 0.04 | | | % (max) |

| Symbol | Parameter | Conditions | LM48100Q | | | Units (Limits) |
|---|---|---|---|---|---|---|
| | | | Typical (Note 7) | Room Temp Limits (Note 8) | Extended Temp Limits (Notes 8, 9) | |
| PSRR | Power Supply Rejection Ratio | $V_{RIPPLE}$ = 200m$V_{P-P}$ Sine, Inputs AC GND, $C_{IN\_}$ = 1µF, input referred, $C_{BIAS}$ = 2.2µF | | | | |
| | | f = 217Hz<br>f = 1kHz | 78<br>75 | 66 | 60 | dB (min)<br>dB |
| SNR | Signal-to-Noise-Ratio | $P_{OUT}$ = TBDmW, f = 1kHz | 106 | | | dB |
| $\in_{OS}$ | Output Noise | $A_V$ = 0dB, A-weighted Filter | 12.5 | | | µV |
| $I_{OUT(\overline{FAULT})}$ | $\overline{FAULT}$ Output Current | $\overline{FAULT}$ = 0, $V_{OUT(\overline{FAULT})}$ = 0.4V | 3 | | | mA |
| $R_{FAULT}$ | Output to Supply Short Circuit Detection Threshold | Short between either OUTA to $V_{DD}$ or GND, or OUTB to $V_{DD}$ or GND<br>Short Circuit<br>Open Circuit | | <br>3<br>7.5 | | <br>kΩ (min)<br>kΩ (max) |
| $R_{FAULT}$ | Output to Supply Short Circuit Detection Threshold | Short between both OUTA and OUTB to $V_{DD}$ or GND<br>Short Circuit<br>Open Circuit | | <br>6<br>15 | | <br>kΩ (min)<br>kΩ (max) |
| $R_{OPEN}$ | Open Circuit Detection Threshold | Open circuit between OUTA and OUTB | | 100<br>200 | | Ω (min)<br>Ω (max) |
| $R_{SHT}$ | Output to Output Short Circuit Detection Threshold | Short circuit between OUTA and OUTB | | 2<br>6 | | Ω (min)<br>Ω (max) |
| $I_{SHTCKT}$ | Short Circuit Current Limit | | 1.43 | | | A |
| $T_{SD}$ | | | 170 | | | °C |
| $t_{DIAG}$ | Diagnostic Time | | 63 | | | ms |

## I²C Interface Characteristics $V_{DD}$ = 5V, 2.2V ≤ I²C$V_{DD}$ ≤ 5.5V (Notes 1, 2)

The following specifications apply for $A_V$ = 0dB, $R_L$ = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for $T_A$ = 25°C.

| Symbol | Parameter | Conditions | LM48100Q | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 7) | Limits (Note 8) | |
| $t_1$ | SCL period | | | 2.5 | µs (min) |
| $t_2$ | SDA Setup Time | | | 100 | ns (min) |
| $t_3$ | SDA Stable Time | | | 0 | ns (min) |
| $t_4$ | Start Condition Time | | | 100 | ns (min) |
| $t_5$ | Stop Condition Time | | | 100 | ns (min) |
| $t_6$ | SDA Data Hold Time | | | 100 | ns (min) |
| $V_{IH}$ | Logic High Input Threshold | | | 0.7 x I²C$V_{DD}$ | V (min) |
| $V_{IL}$ | Logic Low Input Threshold | | | 0.3 x I²C$V_{DD}$ | V (max) |

## I²C Interface Characteristics $V_{DD}$ = 5V, 1.8V ≤ I²C$V_{DD}$ ≤ 2.2V (Notes 1, 2)

The following specifications apply for $A_V$ = 0dB, $R_L$ = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for $T_A$ = 25°C.

| Symbol | Parameter | Conditions | LM48100Q | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 7) | Limits (Note 8) | |
| $t_1$ | SCL period | | | 2.5 | µs (min) |
| $t_2$ | SDA Setup Time | | | 250 | ns (min) |
| $t_3$ | SDA Stable Time | | | 0 | ns (min) |
| $t_4$ | Start Condition Time | | | 250 | ns (min) |
| $t_5$ | Stop Condition Time | | | 250 | ns (min) |

| Symbol | Parameter | Conditions | LM48100Q | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 7) | Limits (Note 8) | |
| $t_6$ | SDA Data Hold Time | | | 250 | ns (min) |
| $V_{IH}$ | Logic High Input Threshold | | | 0.7 x $I^2CV_{DD}$ | V (min) |
| $V_{IL}$ | Logic Low Input Threshold | | | 0.3 x $I^2CV_{DD}$ | V (max) |

**Note 1:** "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

**Note 2:** The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

**Note 4:** Human body model, applicable std. JESD22-A114C.

**Note 5:** Machine model, applicable std. JESD22-A115-A.

**Note 6:** $\theta_{JA}$ measured with a 4 layer JEDEC board.

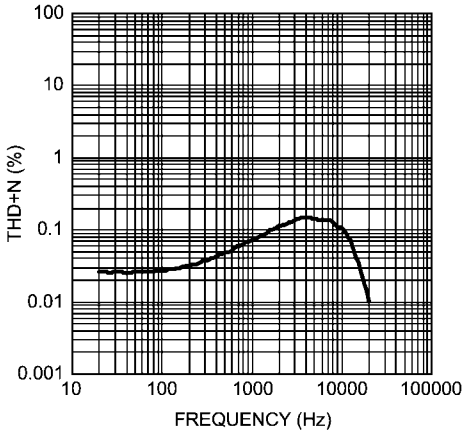
**Note 7:** Typical values represent most likely parametric norms at $T_A$ = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

**Note 8:** Datasheet min/max specification limits are guaranteed by test or statistical analysis.

**Note 9:** Min/max specification limits guaranteed for $T_A$ = –40°C to 105°C.

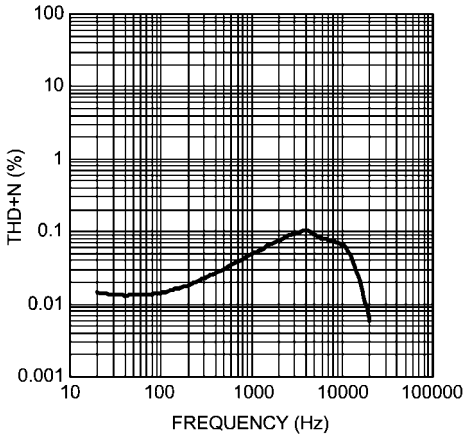
## Typical Performance Characteristics

**THD+N vs Frequency**
**$V_{DD}$ = 3.6V, $P_{OUT}$ = 600mW, $R_L$ = 4Ω**



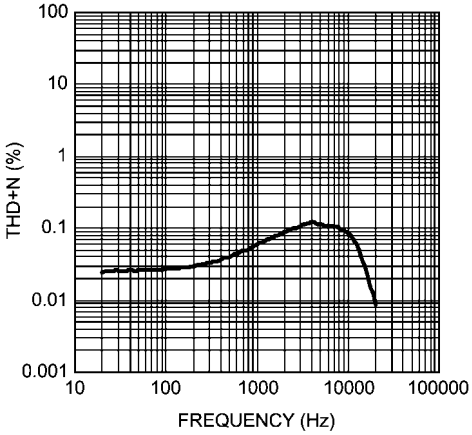

30075804

**THD+N vs Frequency**
**$V_{DD}$ = 3.6V, $P_{OUT}$ = 400mW, $R_L$ = 8Ω**



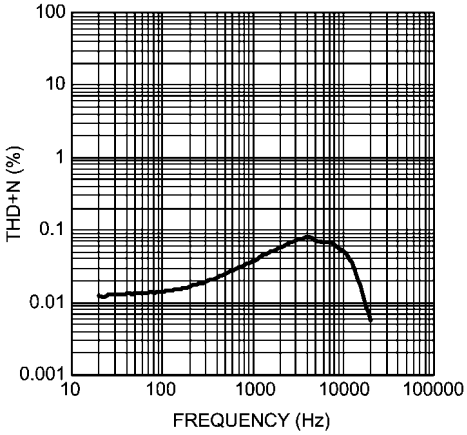

30075806

**THD+N vs Frequency**
**$V_{DD}$ = 5.0V, $P_{OUT}$ = 1.2W, $R_L$ = 4Ω**



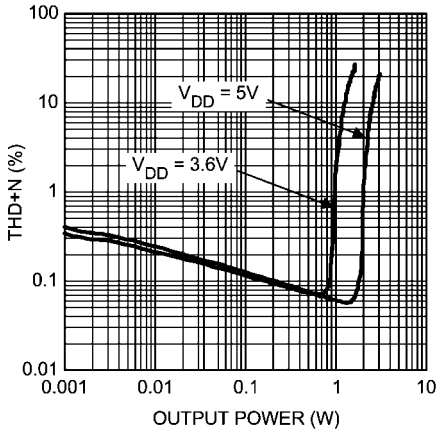

30075805

**THD+N vs Frequency**
**$V_{DD}$ = 5.0V, $P_{OUT}$ = 850mW, $R_L$ = 8Ω**



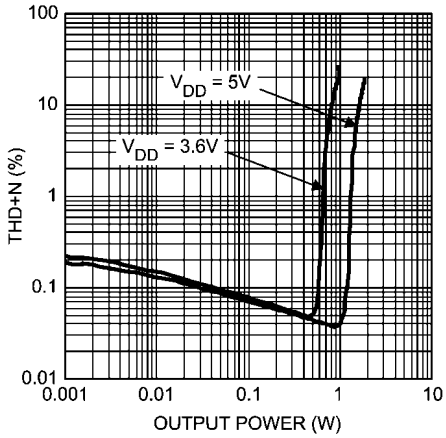

30075807

**THD+N vs Output Power**
**f = 1kHz, $R_L$ = 4Ω**



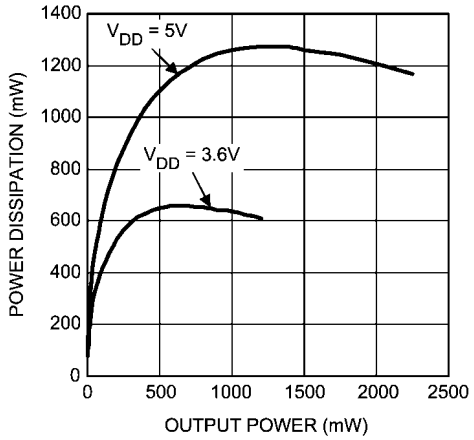

30075802

**THD+N vs Output Power**
**f = 1kHz, $R_L$ = 8Ω**



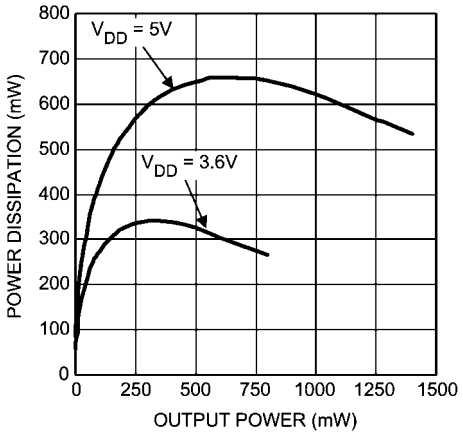

30075803

**Power Dissipation vs Output Power**
**f = 1kHz, $R_L$ = 4Ω**



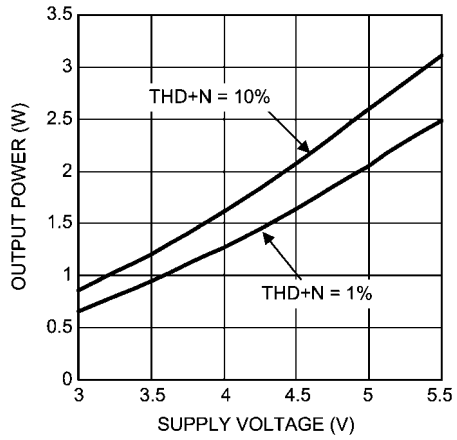

30075808

**Power Dissipation vs Output Power**
**f = 1kHz, $R_L$ = 8Ω**



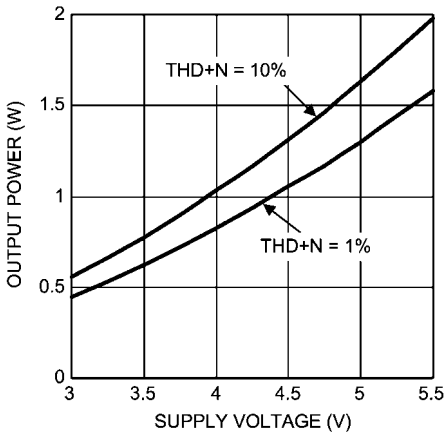

30075809

**Output Power vs Supply Voltage**
**f = 1kHz, $R_L$ = 4Ω**



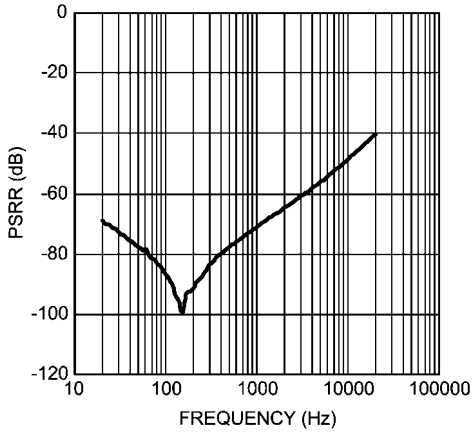

30075810

**Output Power vs Supply Voltage**
**f = 1kHz, $R_L$ = 8Ω**




30075811

**PSRR vs Frequency**
**$V_{DD}$ = 3.6V, $V_{RIPPLE}$ = 200m$V_{P-P}$, $R_L$ = 8Ω**




30075812

# Application Information

### WRITE-ONLY I²C COMPATIBLE INTERFACE

The LM48100Q is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48100Q and the master can communicate at clock rates up to 400kHz. Figure 2 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48100Q is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 3). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 4). The LM48100Q device address is 111110X, where X is determined by ADR (Table 2). ADR = 1 sets the device address to 1111101. ADR = 0 sets the device address to 1111100.

### I²C BUS FORMAT

The I²C bus format is shown in Figure 4. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit. R/$\overline{W}$ = 0 indicates the master is writing to the slave device, R$\overline{W}$ = 1 indicates the master wants to read data from the slave device. Set R/$\overline{W}$ = 0; the LM48100Q is a WRITE-ONLY device and will not respond the R/$\overline{W}$ = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48100Q receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM48100Q sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high.

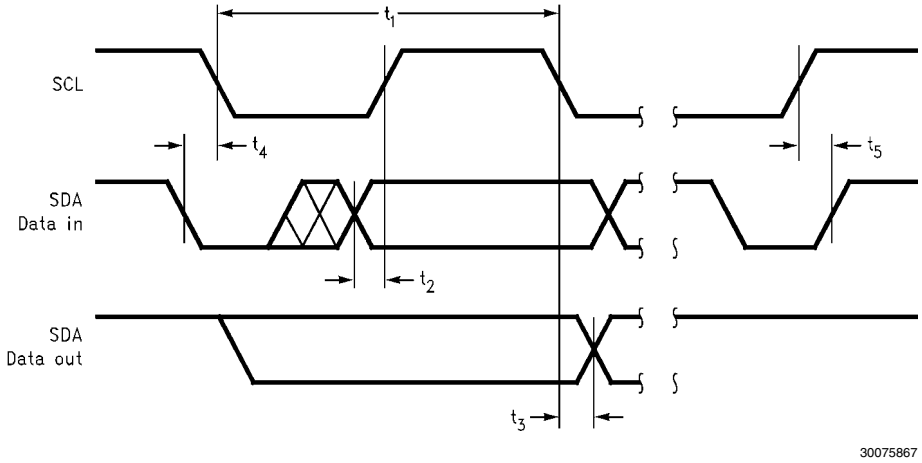



**FIGURE 2. I²C Timing Diagram**

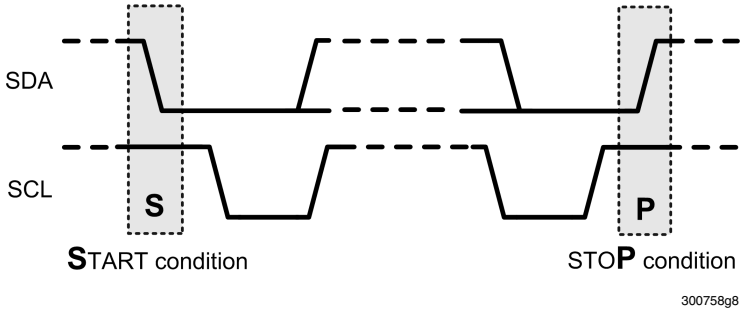



**FIGURE 3. Start and Stop Diagram**

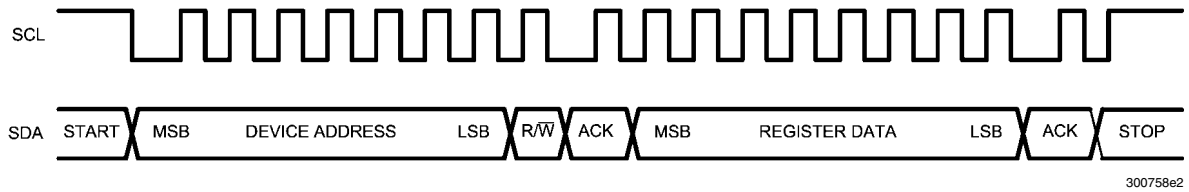



**FIGURE 4. Example Write Sequence**

**TABLE 1. Device Address**

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|---|
| ADR = 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| ADR = 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

**TABLE 2. I²C Control Registers**

| Register Address | Register Name | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | MODE CONTROL | 0 | 0 | 0 | POWER_ON | INPUT_2 | INPUT_1 | 0 | 0 |
| 1 | DIAGNOSTIC CONTROL | 0 | 0 | 1 | DG_EN | DG_CONT | DG_RESET | ILIMIT | 0 |
| 2 | FAULT DETECTION CONTROL | 0 | 1 | 0 | TSD | OCF | RAIL_SHT | OUTPUT _OPEN | OUTPUT _SHORT |
| 3 | VOLUME CONTROL 1 | 0 | 1 | 1 | VOL1_4 | VOL1_3 | VOL1_2 | VOL1_1 | VOL1_0 |
| 4 | VOLUME CONTROL 2 | 1 | 0 | 0 | VOL2_4 | VOL2_3 | VOL2_2 | VOL_2 | VOL2_0 |

**TABLE 3. Mode Control Registers**

| BIT | NAME | VALUE | DESCRIPTION |
|---|---|---|---|
| B0, B1 | RESERVED | 0 | Unused |
| B2 | INPUT_1 | 0 | IN1 Input unselected |
| | | 1 | IN1 Input selected |
| B3 | INPUT_2 | 0 | IN2 Input unselected |
| | | 1 | IN2 Input selected |
| B4 | POWER_ON | 0 | Device Disabled |
| | | 1 | Device Enabled |

## DIAGNOSTIC CONTROL

The LM48100Q output fault diagnostics are controlled through the I²C interface. When power is initially applied to the device, the LM48100Q initializes, performing the full diagnostic sequence; output short to $V_{DD}$ and GND, outputs shorted together, and no load condition, is performed. The device remains in shutdown while the initial diagnostic check is performed. Any I²C commands written to the device during this time are stored and implemented once the diagnostic check is complete. The initial diagnostic sequence can be terminated by setting DG_RESET = 1.

The Diagnostic Control register, register 1, controls the LM48100Q diagnostic process. Bit B4, DG_EN, enables the output fault detection. Set DG_EN = 1 to enable the output diagnostic test sequence. The LM48100Q treats the DG_EN bit as rising-edge-sensitive; once DG_EN = 1 is clocked into the device, the diagnostic test is performed. If the LM48100Q is in one-shot mode, once the test sequence is performed, the DG_EN bit is ignored and the test sequence will not be run again. Cycle DG_EN from high-to-low-to-high to re-enable the one-shot diagnostic test sequence.

In continuous diagnostic mode, the test sequence is repeated until either a fault condition occurs, DG_RESET is cycled, or the device is taken out of continuous diagnostic mode. Set DG_CONT = 1 before setting DG_EN = 1 to initiate a continuous diagnostic. Set DG-CONT = 0 to disable continuous diagnostic mode. When the device is active and DG_EN = 0, the LM48100Q does not perform the output short, or no load diagnostics, however, the thermal overload and output over current protection circuitry remains active, and disables the device should a thermal or over-current fault occur. The initial diagnostic operation when power is applied to the device occurs regardless of the state of DG_EN. The LM48100Q output fault detection can be set to either continuous mode where the output diagnostic occurs every 60ms, or a one-shot mode. Set bit B3 (DG_CONT) to 1 for continuous mode, set B3 = 0 for one-shot mode.

Bit B2, DG_RESET, restores the LM48100Q to normal operation after an output fault is detected. Toggle DG_RESET to re-enable the device outputs and set $\overline{\text{FAULT}}$ high.

**TABLE 4. Diagnostic Control Register**

| BIT | NAME | VALUE | DESCRIPTION |
|---|---|---|---|
| B0 | RESERVED | 0 | Unused |
| B1 | ILIMIT | 0 | Fixed output current limit |
| | | 1 | Supply dependent output current limit |
| B2 | DG _RESET | 0 | Normal operation. $\overline{\text{FAULT}}$ remains low and device is disabled once a fault occurs. |
| | | 1 | Reset $\overline{\text{FAULT}}$ output. Device returns to pre-fault operation. |
| B3 | DG _CONT | 0 | One shot diagnostic |
| | | 1 | Continuous diagnostic |
| B4 | DG_EN | 0 | Disable diagnostic |
| | | 1 | Enable diagnostic |

## FAULT DETECTION CONTROL REGISTER

The LM48100Q output fault tests are individually controlled through the Fault Detection Control register, register 2. Setting any of the bits in the Fault Detection Control register to 1 causes the $\overline{\text{FAULT}}$ circuitry to ignore the associated test. For example, if B2 (RAIL_SHT) = 1 and the output is shorted to $V_{DD}$, the $\overline{\text{FAULT}}$ output remains high. Although the $\overline{\text{FAULT}}$ circuitry ignores the selected test, the LM48100Q protection circuitry remains active, and disables the device. This feature is useful for diagnosing which fault caused a $\overline{\text{FAULT}}$condition.

If DG_EN = 1, and a diagnostic sequence is initiated, all the tests are performed regardless of their state in the Fault Detection Control register. If DG_EN = 0, the RAIL_SHT, OUTPUT_OPEN and OUTPUT_SHT tests are not performed, however, the thermal overload and output over-current detection circuitry remains active.

**TABLE 5. Fault Detection Control Register**

| BIT | NAME | VALUE | DESCRIPTION |
|---|---|---|---|
| B0 | OUTPUT _SHT | 0 | Normal operation |
| | | 1 | Ignore output short circuit fault (outputs shorted together) |
| B1 | OUTPUT _OPEN | 0 | Normal operation |
| | | 1 | Ignore output short circuit fault |
| B2 | RAIL _SHT | 0 | Normal operation |
| | | 1 | Ignore output short to $V_{DD}$ or GND fault |
| B3 | OVF | 0 | Normal operation |
| | | 1 | Ignore output over-current fault |
| B4 | TSD | 0 | Normal operation |
| | | 1 | Ignore thermal overload fault |

## GENERAL AMPLIFIER FUNCTION

### Bridge Configuration Explained

The LM48100Q is designed to drive a load differentially, a configuration commonly referred to as a bridge-tied load (BTL). The BTL configuration differs from the single-ended configuration, where one side of the load is connected to ground. A BTL amplifier offers advantages over a single-ended device. By driving the load differentially, the output voltage is doubled, compared to a single-ended amplifier under similar conditions. This doubling of the output voltage leads to a quadrupling of the output power. For example, the theoretical maximum output power for a single-ended amplifier driving 8Ω and operating from a 5V supply is 158mW, while the theoretical maximum output power for a BTL amplifier operating under the same conditions is 633mW. Since the amplifier outputs are both biased about $V_{DD}/2$, there is no net DC voltage across the load, eliminating the DC blocking capacitors required by single-ended, single-supply amplifiers.

### Input Mixer/Multiplexer

The LM48100Q features an input mixer/multiplexer controlled through the I²C interface. The mixer/multiplexer allows either input, or the combination of both inputs to appear at the device output. Bits B2 (INPUT_1) and B3 (INPUT_2) of the Mode Control Register select the individual input channels. Set INPUT_1 = 1 to select the audio signal on IN1. Set INPUT_2 = 1 to select the audio signal on IN2. Setting both INPUT_1 and INPUT_2 = 1 mixes $V_{IN1}$ and $V_{IN2}$, and the LM48100Q outputs the result as a mono signal (Table 7).

**TABLE 6. Input Multiplexer Control**

| INPUT_1 | INPUT_2 | LM48100Q OUTPUT |
|---|---|---|
| 0 | 0 | MUTE. No input selected |
| 1 | 0 | IN1 ONLY |
| 0 | 1 | IN2 ONLY |
| 1 | 1 | IN1 + IN2 |

## OUTPUT FAULT DETECTION

### Output Short to Supplies ($V_{DD}$ or GND)

With a standard speaker load (6Ω - 100Ω) connected between OUTA and OUTB, the LM48100Q can detect a short between the outputs and either $V_{DD}$ or GND. A short is detected if the impedance between either OUTA or OUTB and $V_{DD}$ or GND is less than 3kΩ. A short is also detected if the impedance between BOTH OUTA and OUTB and either $V_{DD}$ or GND is less than 6kΩ. Under either of these conditions, the amplifier outputs are disabled and $\overline{\text{FAULT}}$ is driven low. No short is detected if the impedance between either output and $V_{DD}$ or GND is greater than 7.5kΩ. Likewise, no short is detected if the impedance between BOTH outputs and $V_{DD}$ or GND is greater than 15kΩ.

### Output Short Circuit and Open Circuit Detection

The LM48100Q can detect whether the amplifier outputs have been shorted together or, an output open circuit condition has occurred. An output short circuit is detected if the impedance between OUTA and OUTB is less than 2Ω. An open circuit is detected if the impedance between OUTA and OUTB is greater than 200Ω. Under either of these conditions, the amplifier outputs are disabled and $\overline{\text{FAULT}}$ is driven low. The device remains in normal operation if the impedance between OUTA and OUTB is in the range of 6Ω to 100Ω. The output open circuit test is only performed during the initial diagnostic sequence during power up, or when DG_ENABLE is set to 1.

### Output Over-Current Detection

The LM48100Q has two over current detection modes, a fixed current limit, and a supply dependent current limit. Bit B1 (ILIMIT) of the Diagnostic Control Register selects the overcurrent detection mode. Set ILIMIT = 0 to select a fixed current limit of 1.47A (typ). Set ILIMIT = 1 to select the supply dependent current limit mode. In supply dependent mode, the current limit is determined by equation (1):

$$I_{SHTCKT} = 0.264 \times V_{DD} \quad (A) \qquad (1)$$

If the output current exceeds the current limit, the device outputs are disabled and $\overline{\text{FAULT}}$ is driven low. The output overcurrent detection circuitry remains active when the diagnostics have been disabled (DG_EN = 0).

### Thermal Overload Detection

The LM48100Q has thermal overload threshold of 170°C (typ). If the die temperature exceeds 170°C, the outputs are disabled and $\overline{\text{FAULT}}$ is driven low. The thermal overload detection circuitry remains active when the diagnostics have been disabled (DG_EN = 0).

## OPEN $\overline{\text{FAULT}}$ OUTPUT

The LM48100Q features an open drain, fault indication output, $\overline{\text{FAULT}}$, that asserts when a fault condition is detected by the device. $\overline{\text{FAULT}}$ goes low when either an output short, output open, over current, or thermal overload fault is detected, and the diagnostic test is not ignored, see *FAULT DETECTION CONTROL* section. $\overline{\text{FAULT}}$ remains low even after the fault condition has been cleared and the diagnostic tests are repeated. Toggle DG_RESET to clear $\overline{\text{FAULT}}$.

Connect a 1.5kΩ or higher pull-up resistor between $\overline{\text{FAULT}}$ and $V_{DD}$.

## VOLUME CONTROL

**TABLE 7. Volume Control**

| Volume Step | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 | Gain (dB) |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | –80 |
| 2 | 0 | 0 | 0 | 0 | 1 | –54 |
| 3 | 0 | 0 | 0 | 1 | 0 | –40.5 |
| 4 | 0 | 0 | 0 | 1 | 1 | –34.5 |
| 5 | 0 | 0 | 1 | 0 | 0 | –30 |
| 6 | 0 | 0 | 1 | 0 | 1 | –27 |
| 7 | 0 | 0 | 1 | 1 | 0 | –24 |
| 8 | 0 | 0 | 1 | 1 | 1 | –21 |
| 9 | 0 | 1 | 0 | 0 | 0 | –18 |
| 10 | 0 | 1 | 0 | 0 | 1 | –15 |
| 11 | 0 | 1 | 0 | 1 | 0 | –13.5 |
| 12 | 0 | 1 | 0 | 1 | 1 | –12 |
| 13 | 0 | 1 | 1 | 0 | 0 | –10.5 |
| 14 | 0 | 1 | 1 | 0 | 1 | –9 |
| 15 | 0 | 1 | 1 | 1 | 0 | –7.5 |
| 16 | 0 | 1 | 1 | 1 | 1 | –6 |
| 17 | 1 | 0 | 0 | 0 | 0 | –4.5 |
| 18 | 1 | 0 | 0 | 0 | 1 | –3 |
| 19 | 1 | 0 | 0 | 1 | 0 | –1.5 |
| 20 | 1 | 0 | 0 | 1 | 1 | 0 |
| 21 | 1 | 0 | 1 | 0 | 0 | 1.5 |
| 22 | 1 | 0 | 1 | 0 | 1 | 3 |
| 23 | 1 | 0 | 1 | 1 | 0 | 4.5 |
| 24 | 1 | 0 | 1 | 1 | 1 | 6 |
| 25 | 1 | 1 | 0 | 0 | 0 | 7.5 |
| 26 | 1 | 1 | 0 | 0 | 1 | 9 |
| 27 | 1 | 1 | 0 | 1 | 0 | 10.5 |
| 28 | 1 | 1 | 0 | 1 | 1 | 12 |
| 29 | 1 | 1 | 1 | 0 | 0 | 13.5 |
| 30 | 1 | 1 | 1 | 0 | 1 | 15 |
| 31 | 1 | 1 | 1 | 1 | 0 | 16.5 |
| 32 | 1 | 1 | 1 | 1 | 1 | 18 |

## SHUTDOWN FUNCTION

The LM48100Q features an I²C selectable low power shutdown mode that disables the device, reducing quiescent current consumption to 0.01µA. Set bit B4 (POWER_ON) in the Mode Control Register to 0 to disable the device. Set B0 to 1 to enable the device.

## POWER DISSIPATION

The increase in power delivered by a BTL amplifier leads to a direct increase in internal power dissipation. The maximum power dissipation for a BTL amplifier for a given supply voltage and load is given by equation (2):

$$P_{DMAX} = 4 \times V_{DD}^2 / 2\pi^2 R_L \quad \text{(Watts)} \qquad (2)$$

The maximum power dissipation of the TSSOP package is calculated by equation (3):

$$P_{DMAX\ (PKG)} = T_{JMAX} - T_A \ / \ \theta_{JA} \text{ (Watts)} \qquad (3)$$

where $T_{JMAX}$ is 150°C, $T_A$ is the ambient temperature and $\theta_{JA}$ is the thermal resistance specified in the *Absolute Maximum Ratings*.

If the power dissipation for a given operating condition exceeds the package maximum, either decrease the ambient temperature, increase air flow, add heat sinking to the device, or increase the load impedance and/or supply voltage. The LM48100Q TSSOP package features an exposed die attach pad (DAP) that can be used to increase the maximum power dissipation of the package, see *Exposed DAP Mounting Considerations*.

The LM48100Q features thermal overload protection that disables the amplifier output stage when the die temperature exceeds +170°C. See the *Thermal Overload Detection* section.

## PROPER SELECTION OF EXTERNAL COMPONENTS

### Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1µF ceramic capacitor from $V_{DD}$ to GND. Additional bulk capacitance may be added as required.

### Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48100Q. The input capacitors create a high-pass filter with the input resistors $R_{IN}$. The -3dB point of the high-pass filter is found using Equation (4) below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad \text{(Hz)} \qquad (4)$$

Where the value of $R_{IN}$ is given in the *Electrical Characteristics Table*.

High pass filtering the audio signal helps protect the speakers. When the LM48100Q is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved PSRR.

### Bias Capacitor Selection

The LM48100Q internally generates a $V_{DD}/2$ common-mode bias voltage. The BIAS capacitor $C_{BIAS}$, improves PSRR and THD+N by reducing noise at the BIAS node. Use a 2.2µF ceramic placed as close to the device as possible.

## PCB Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48100Q and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents digital noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

## Exposed Dap Mounting Considerations

The LM48100Q TSSOP-EP package features an exposed die-attach (thermal) pad on its backside. The exposed pad provides a direct heat conduction path from the die to the PCB, reducing the thermal resistance of the package. Connect the exposed pad to GND with a large pad and via to a large GND plane on the bottom of the PCB for best heat distribution.

## LM48100QTL Demoboard Bill of Materials

| Designator | Quantity | Description |
|---|---|---|
| C1 | 1 | 10µF ±10% 16V Tantalum Capacitor (B Case) AVX TPSB106K016R0800 |
| C2 | 1 | 1µF ±10% 16V X7R Ceramic Capacitor (603) Murata GRM188R71C105KA12D |
| C3, C5 | 2 | 0.1µF ±10% 16V X7R Ceramic Capacitor (603) Murata GRM188R71C104KA01D Panasonic ECJ-1VB1C104K |
| C4 | 1 | 2.2 µF ±10% 16V X7R Ceramic Capacitor (603) Murata GRM188R71A225KE15D |
| C6, C7 | 2 | 0.1µF ±10% 50V X5R Ceramic Capacitor (1206) Murata GRM319R71H104KA01D |
| R1, R2 | 2 | 5kΩ ±5% 1/10W Thick Film Resistor (603) Vishay CRCW06035R1KJNEA |
| R3 | 1 | 1.5kΩ ±5% 1/10W Thick Film Resistor (603) Vishay CRCW06031K50JNEA |
| J2 | 1 | 16-Pin Boardmount Socket 3M 8516-4500JL |
| JU1 | 1 | 3-Pin Header |
| JU2–JU12 | 11 | 2 Pin Header |
| LM48100QMH | U1 | LM48100QMH (14-Pin TSSOP-EP) |

## Demo Board Schematic

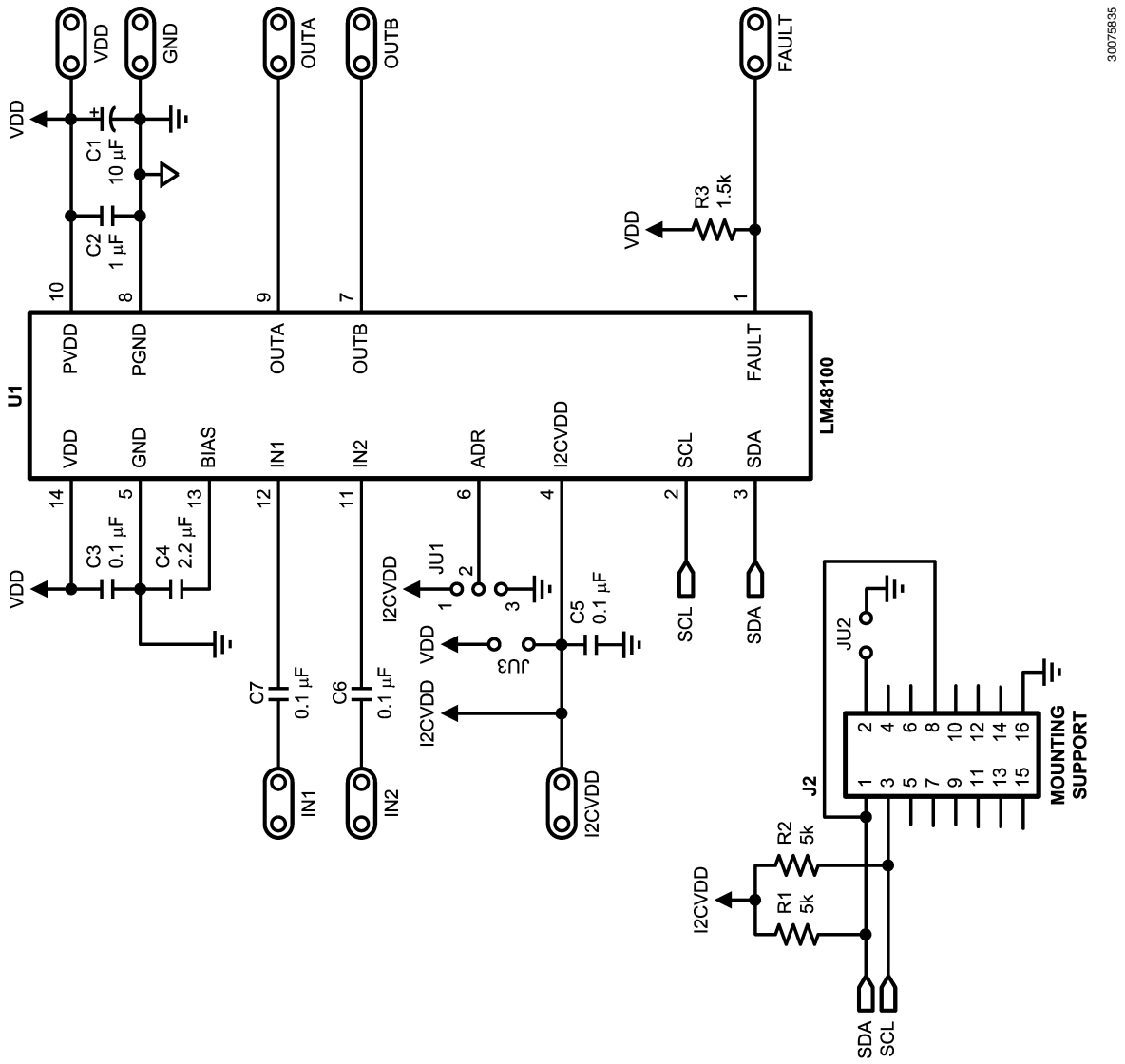
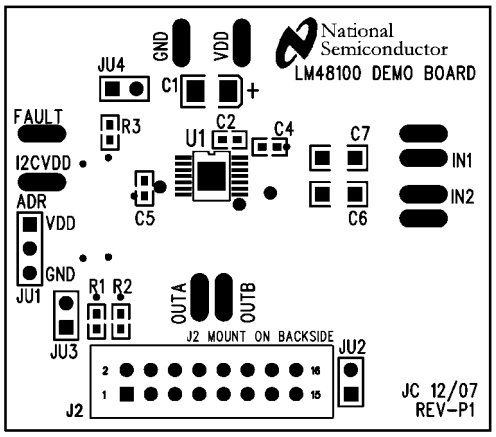


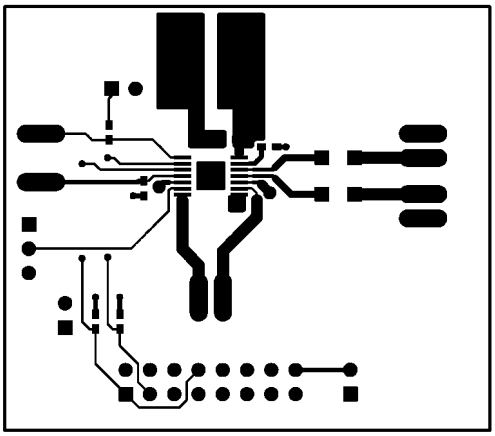

FIGURE 5. LM48100Q Demo Board Schematic

## PC Board Layout



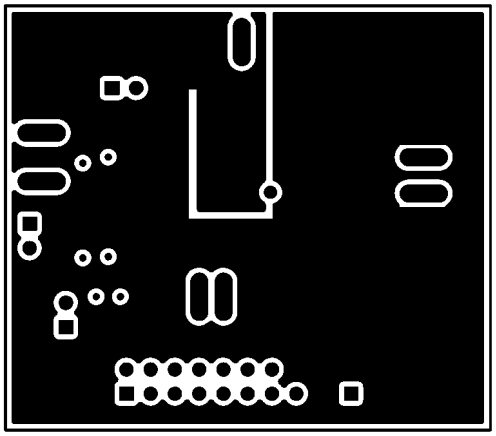

30075836

**FIGURE 6: Top Silkscreen**



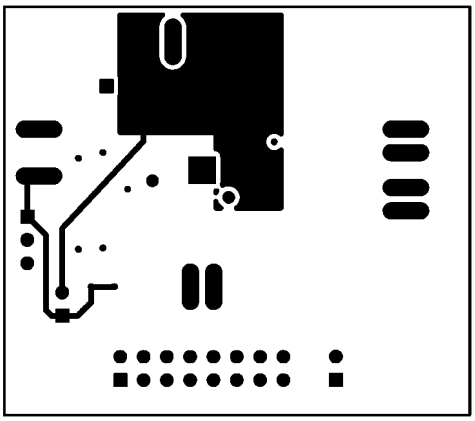
30075837

**FIGURE 7: Top Layer**



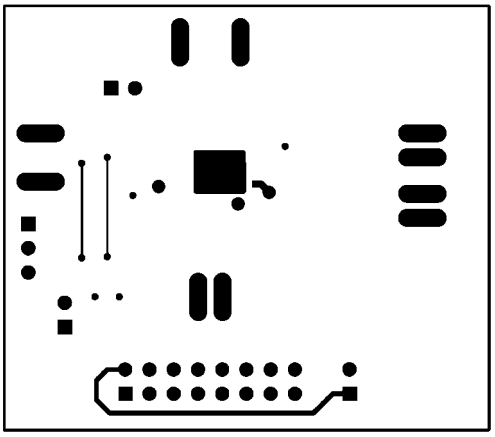
30075838

**FIGURE 8: Layer 2**



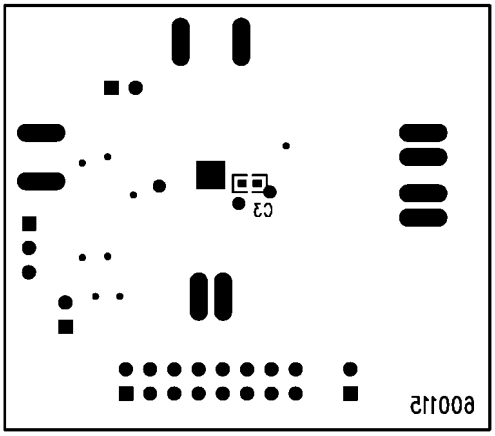
30075839

**FIGURE 9: Layer 3**



30075840

**FIGURE 10: Bottom Layer**



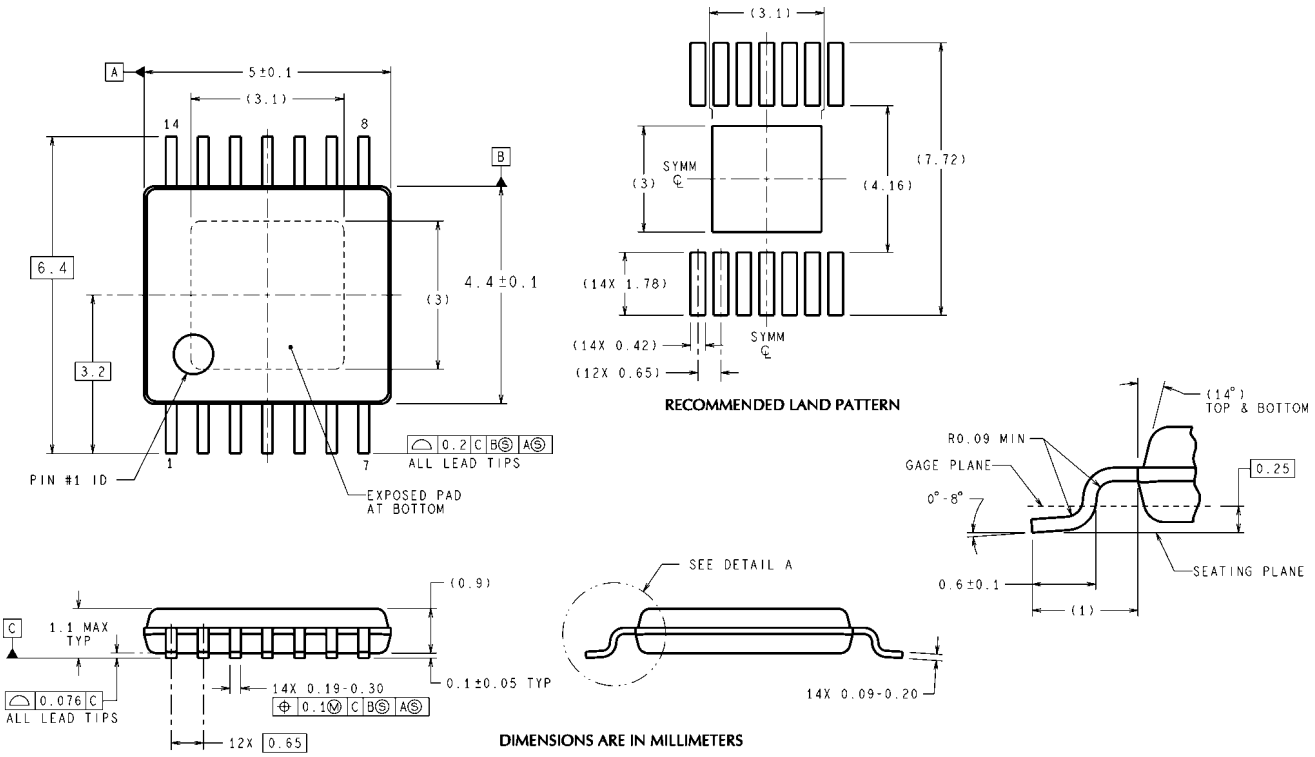

30075841

**FIGURE 11: Bottom Silkscreen**

## Revision History

| Rev | Date | Description |
|---|---|---|
| 1.0 | 10/14/08 | Initial release. |
| 1.01 | 10/20/08 | Text edits. |
| 1.02 | 11/07/08 | Added a column (Limits) in the Electrical tables. |
| 1.03 | 11/12/08 | Text edits. |

## Physical Dimensions inches (millimeters) unless otherwise noted




MXA14A (Rev A)

**14–Lead TSSOP Exposed Pad**
**Order Number LM48100QMH**
**NS Package Number MXA14A**

# Notes

# Notes

**For more National Semiconductor product information and proven design tools, visit the following Web sites at:**

| Products | | Design Support | |
|---|---|---|---|
| Amplifiers | www.national.com/amplifiers | WEBENCH® Tools | www.national.com/webench |
| Audio | www.national.com/audio | App Notes | www.national.com/appnotes |
| Clock and Timing | www.national.com/timing | Reference Designs | www.national.com/refdesigns |
| Data Converters | www.national.com/adc | Samples | www.national.com/samples |
| Interface | www.national.com/interface | Eval Boards | www.national.com/evalboards |
| LVDS | www.national.com/lvds | Packaging | www.national.com/packaging |
| Power Management | www.national.com/power | Green Compliance | www.national.com/quality/green |
| Switching Regulators | www.national.com/switchers | Distributors | www.national.com/contacts |
| LDOs | www.national.com/ldo | Quality and Reliability | www.national.com/quality |
| LED Lighting | www.national.com/led | Feedback/Support | www.national.com/feedback |
| Voltage Reference | www.national.com/vref | Design Made Easy | www.national.com/easy |
| PowerWise® Solutions | www.national.com/powerwise | Solutions | www.national.com/solutions |
| Serial Digital Interface (SDI) | www.national.com/sdi | Mil/Aero | www.national.com/milaero |
| Temperature Sensors | www.national.com/tempsensors | Solar Magic® | www.national.com/solarmagic |
| Wireless (PLL/VCO) | www.national.com/wireless | Analog University® | www.national.com/AU |



For the most current product information visit us at www.national.com

**National Semiconductor Americas Technical Support Center**
Email: support@nsc.com
Tel: 1-800-272-9959

**National Semiconductor Europe Technical Support Center**
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

**National Semiconductor Asia Pacific Technical Support Center**
Email: ap.support@nsc.com

**National Semiconductor Japan Technical Support Center**
Email: jpn.feedback@nsc.com