

# HEF40098B

Hex inverting buffer; 3-state

Rev. 06 — 24 June 2009

Product data sheet

## 1. General description

The HEF40098B is a hex inverting buffer with 3-state outputs. The 3-state outputs are controlled by two active LOW enable inputs ( $1\overline{OE}$  and  $2\overline{OE}$ ). A HIGH on  $1\overline{OE}$  causes four of the six active LOW buffer elements ( $1\overline{Y}0$  to  $1\overline{Y}3$ ) to assume a high-impedance or OFF-state regardless of the other input conditions and a HIGH on  $2\overline{OE}$  causes the outputs of the remaining two buffer elements ( $2\overline{Y}0$  and  $2\overline{Y}1$ ) to assume a high-impedance or OFF-state regardless of the other input conditions.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input. It is also suitable for use over the full industrial ( $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ) temperature range.

## 2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- Industrial

## 4. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HEF40098BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF40098BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

## 5. Functional diagram

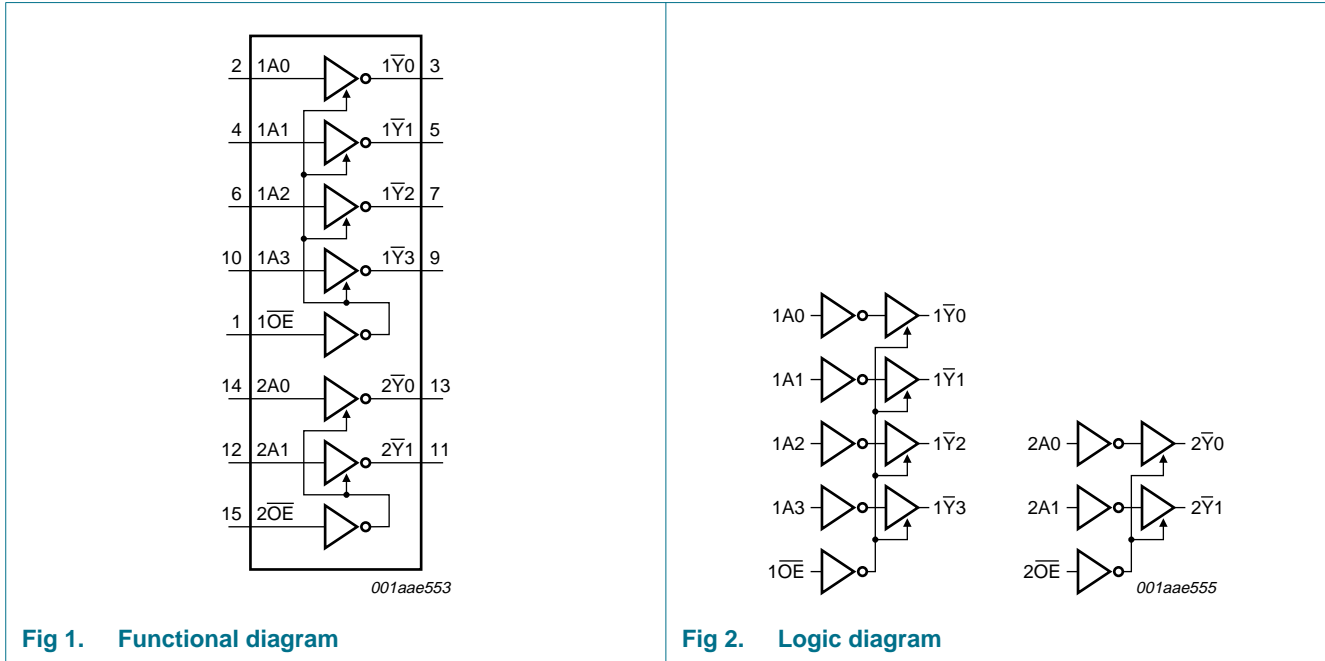


Fig 1. Functional diagram

Fig 2. Logic diagram

## 6. Pinning information

### 6.1 Pinning

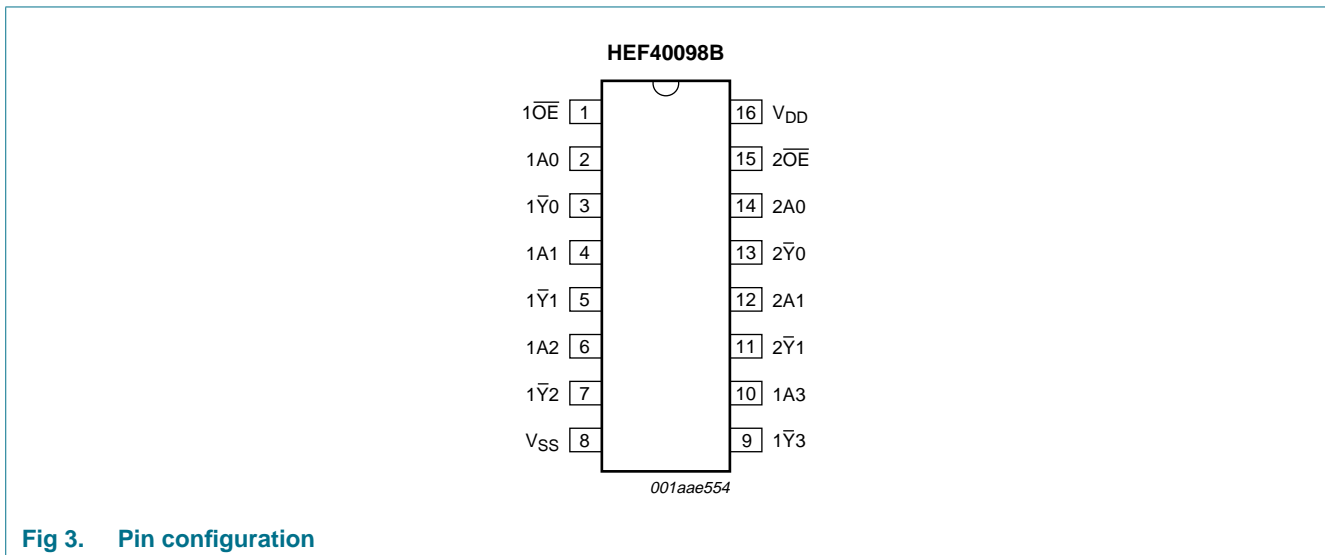


Fig 3. Pin configuration

## 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1 $\overline{OE}$	1	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 10	buffer input
1 $\overline{Y}0$ , 1 $\overline{Y}1$ , 1 $\overline{Y}2$ , 1 $\overline{Y}3$	3, 5, 7, 9	buffer output (active LOW)
V <sub>SS</sub>	8	supply voltage
2 $\overline{Y}0$ , 2 $\overline{Y}1$	13, 11	buffer output (active LOW)
2A0, 2A1	14, 12	buffer input
2 $\overline{OE}$	15	output enable input (active LOW)
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs		Output
nAn	n $\overline{OE}$	n $\overline{Y}n$
H	L	L
L	L	H
X	H	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF state.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DD</sub>	supply voltage		-0.5	+18	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA	
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V	
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA	
I <sub>I/O</sub>	input/output current		-	±10	mA	
I <sub>DD</sub>	supply current		-	50	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
T <sub>amb</sub>	ambient temperature		-40	+85	°C	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 to +85 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation		-	100	mW	

[1] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	ns/V
		$V_{DD} = 10\text{ V}$	-	-	0.5	ns/V
		$V_{DD} = 15\text{ V}$	-	-	0.08	ns/V

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-3.8	-	-3.2	-	-2.5	-	mA
		$V_O = 4.6\text{ V}$	5 V	-1.2	-	-1.0	-	-0.8	-	mA
		$V_O = 9.5\text{ V}$	10 V	-3.8	-	-3.2	-	-2.5	-	mA
		$V_O = 13.5\text{ V}$	15 V	-12.0	-	-10.0	-	-8.0	-	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$ ;	4.75 V	3.5	-	2.9	-	2.3	-	mA
		$V_O = 0.5\text{ V}$ ;	10 V	12.0	-	10.0	-	8.0	-	mA
		$V_O = 1.5\text{ V}$ ;	15 V	24.0	-	20.0	-	16.0	-	mA
$I_I$	input leakage current	$V_I = 0\text{ V}$ or $15\text{ V}$	15 V	-	0.3	-	0.3	-	1.0	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	4	-	4	-	30	$\mu\text{A}$
			10 V	-	8	-	8	-	60	$\mu\text{A}$
			15 V	-	16	-	16	-	120	$\mu\text{A}$
$I_{OZ}$	OFF-state output current		15 V	-	1.6	-	1.6	-	12.0	$\mu\text{A}$
$C_I$	input capacitance			-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; for test circuit see [Figure 6](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nYn; see <a href="#">Figure 4</a>	5 V	70 ns + (0.20 ns/pF) C <sub>L</sub>	-	80	160	ns
			10 V	31 ns + (0.08 ns/pF) C <sub>L</sub>	-	35	70	ns
			15 V	22 ns + (0.06 ns/pF) C <sub>L</sub>	-	25	50	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nYn; see <a href="#">Figure 4</a>	5 V	50 ns + (0.30 ns/pF) C <sub>L</sub>	-	65	130	ns
			10 V	24 ns + (0.13 ns/pF) C <sub>L</sub>	-	30	60	ns
			15 V	23 ns + (0.05 ns/pF) C <sub>L</sub>	-	25	50	ns
t <sub>THL</sub>	HIGH to LOW output transition time	see <a href="#">Figure 4</a>	5 V	15 ns + (0.30 ns/pF) C <sub>L</sub>	-	30	60	ns
			10 V	10 ns + (0.11 ns/pF) C <sub>L</sub>	-	15	30	ns
			15 V	7 ns + (0.07 ns/pF) C <sub>L</sub>	-	10	20	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	see <a href="#">Figure 4</a>	5 V	10 ns + (0.50 ns/pF) C <sub>L</sub>	-	35	70	ns
			10 V	8 ns + (0.24 ns/pF) C <sub>L</sub>	-	20	40	ns
			15 V	6 ns + (0.18 ns/pF) C <sub>L</sub>	-	15	30	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\overline{OE}$ , to nYn; see <a href="#">Figure 5</a>	5 V	-	-	45	85	ns
			10 V	-	-	35	65	ns
			15 V	-	-	30	60	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{OE}$ , to nYn; see <a href="#">Figure 5</a>	5 V	-	-	65	135	ns
			10 V	-	-	40	80	ns
			15 V	-	-	35	70	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	n $\overline{OE}$ , to nYn; see <a href="#">Figure 5</a>	5 V	-	-	70	140	ns
			10 V	-	-	35	75	ns
			15 V	-	-	30	65	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	n $\overline{OE}$ , to nYn; see <a href="#">Figure 5</a>	5 V	-	-	90	185	ns
			10 V	-	-	40	85	ns
			15 V	-	-	35	70	ns

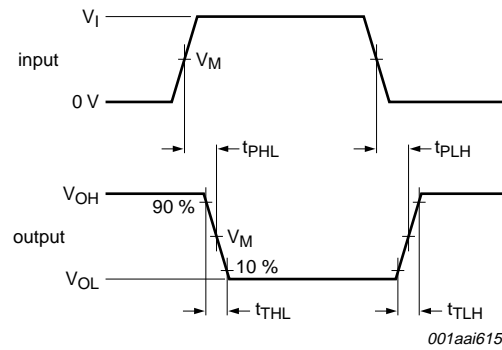
[1] The typical value of the propagation delay and transition times are calculated from the extrapolation formula as shown (C<sub>L</sub> in pF).

**Table 8. Dynamic power dissipation P<sub>D</sub>**

P<sub>D</sub> can be calculated (in  $\mu\text{W}$ ) from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ °C}$ .

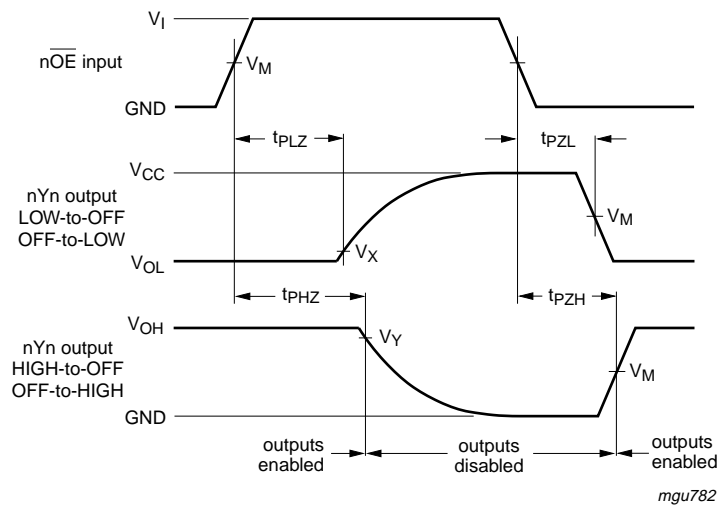
Symbol	Parameter	$V_{DD}$	Typical formula for P <sub>D</sub> ( $\mu\text{W}$ )	where:
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 5000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f <sub>i</sub> = input frequency in MHz,
		10 V	$P_D = 22800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f <sub>o</sub> = output frequency in MHz,
		15 V	$P_D = 81000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C <sub>L</sub> = output load capacitance in pF, V <sub>DD</sub> = supply voltage in V, $\Sigma(C_L \times f_o)$ = sum of the outputs.

12. AC waveforms



Measurement points are given in Table 9, VOL and VOH are typical output voltage levels that occur with the output load.

Fig 4. Input (nAn) to output (nYn) propagation delays

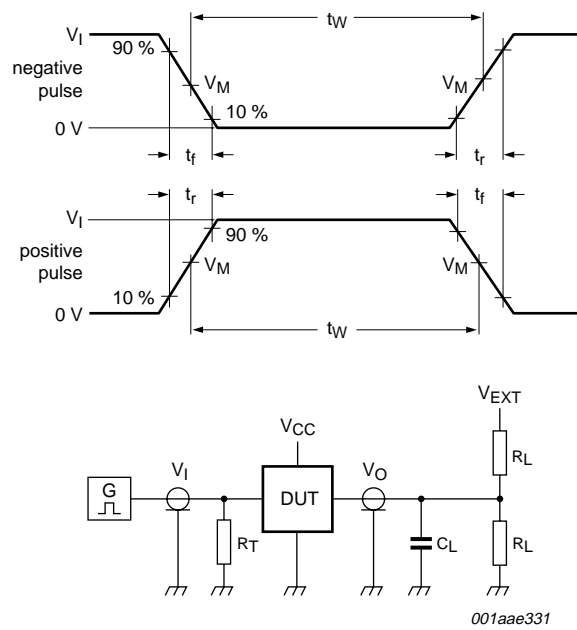


Measurement points are given in Table 9, VOL and VOH are typical output voltage levels that occur with the output load.

Fig 5. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
VDD	VM	VM	VX	VY
5 V to 15 V	0.5VDD	0.5VDD	0.1VDD	0.9VDD



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 6. Test circuitry for switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
5 V to 15 V	$V_{DD}$	$\leq 20$ ns	50 pF	1 k $\Omega$	open	$2V_{DD}$	GND

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

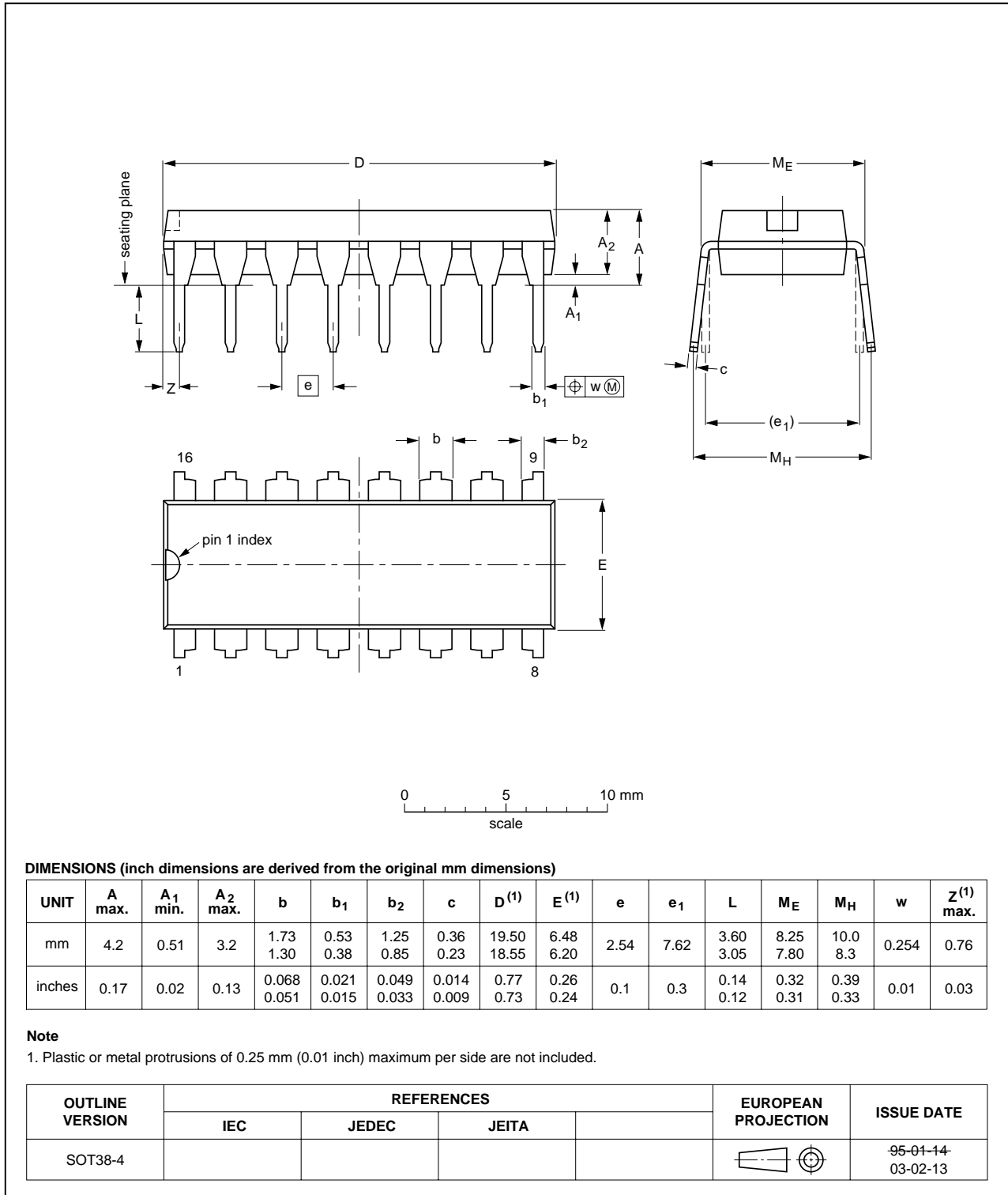


Fig 7. Package outline SOT38-4 (DIP16)



SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

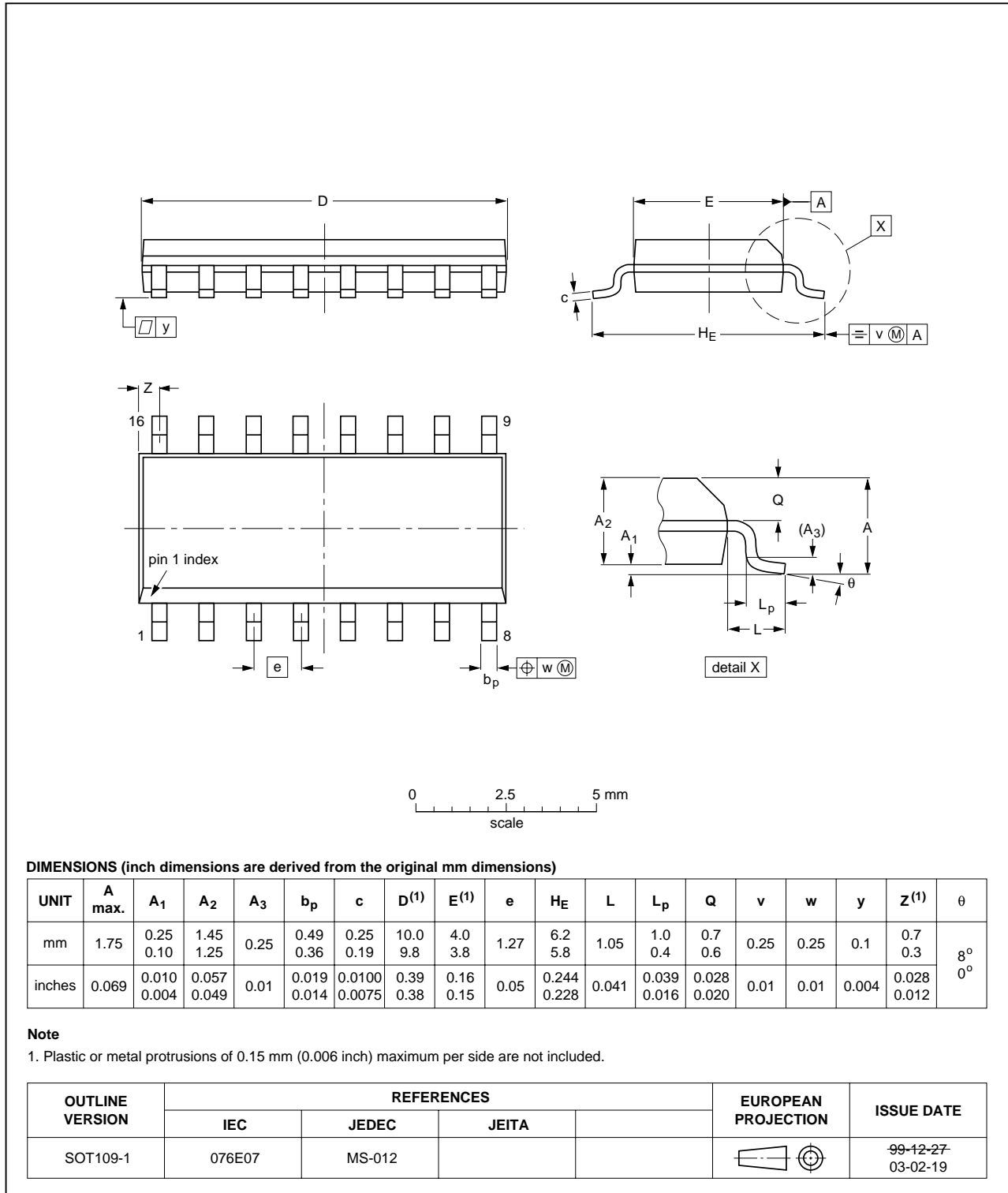


Fig 8. Package outline SOT109-1 (SO16)

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40098B_6	20090624	Product data sheet	-	HEF40098B_5
Modifications:		<ul style="list-style-type: none"><li>• Title changed.</li><li>• <a href="#">Section 2 “Features”</a>, ElectroStatic Discharge (ESD) values removed.</li><li>• <a href="#">Section 8 “Limiting values”</a>, the conditions values of <math>V_I</math> and <math>V_I</math> for <math>I_{IK}</math> and <math>I_{OK}</math> modified.</li><li>• Applications section removed.</li><li>• <a href="#">Section 15 “Legal information”</a>, export control statement added.</li></ul>		
HEF40098B_5	20081031	Product data sheet	-	HEF40098B_4
HEF40098B_4	20080731	Product data sheet	-	HEF40098B_CNV_3
HEF40098B_CNV_3	19950101	Product specification	-	HEF40098B_CNV_2
HEF40098B_CNV_2	19950101	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**17. Contents**

1 **General description** ..... 1

2 **Features** ..... 1

3 **Applications** ..... 1

4 **Ordering information** ..... 1

5 **Functional diagram** ..... 2

6 **Pinning information** ..... 2

6.1 Pinning ..... 2

6.2 Pin description ..... 3

7 **Functional description** ..... 3

8 **Limiting values** ..... 3

9 **Recommended operating conditions** ..... 4

10 **Static characteristics** ..... 4

11 **Dynamic characteristics** ..... 5

12 **AC waveforms** ..... 6

13 **Package outline** ..... 8

14 **Revision history** ..... 10

15 **Legal information** ..... 11

15.1 Data sheet status ..... 11

15.2 Definitions ..... 11

15.3 Disclaimers ..... 11

15.4 Trademarks ..... 11

16 **Contact information** ..... 11

17 **Contents** ..... 12

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