# MC74HCT14A

# Hex Schmitt-Trigger Inverter with LSTTL Compatible Inputs

## High−Performance Silicon−Gate CMOS

The MC74HCT14A may be used as a level converter for interfacing TTL or NMOS outputs to high−speed CMOS inputs.

The HCT14A is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14A finds applications in noisy environments.

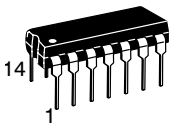
### Features

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS−Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- Pb−Free Packages are Available

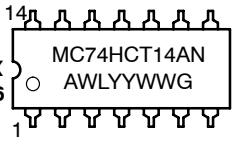
**ON Semiconductor®**

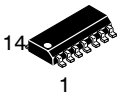
**http://onsemi.com**

**MARKING DIAGRAMS**

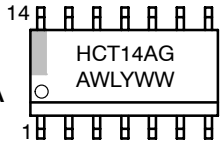


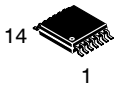

**PDIP−14**
**N SUFFIX**
**CASE 646**



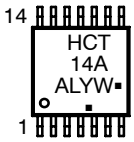



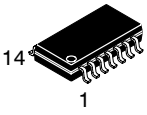

**SOIC−14**
**D SUFFIX**
**CASE 751A**



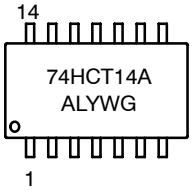




**TSSOP−14**
**DT SUFFIX**
**CASE 948G**




**SOEIAJ−14**
**F SUFFIX**
**CASE 965**



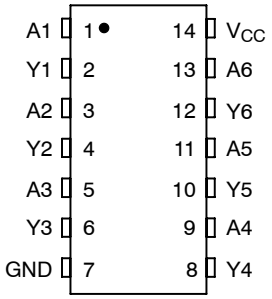

| | |
|---|---|
| A | = Assembly Location |
| L, WL | = Wafer Lot |
| Y, YY | = Year |
| W, WW | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

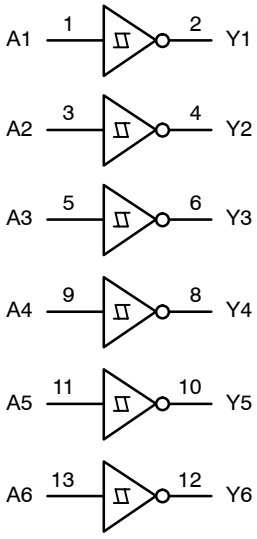
## PIN ASSIGNMENT




## FUNCTION TABLE

| Input A | Output Y |
|---|---|
| L | H |
| H | L |

## LOGIC DIAGRAM




$Y = \overline{A}$ PIN 14 = $V_{CC}$
PIN 7 = GND

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74HCT14AN | PDIP−14 | 25 Units / Rail |
| MC74HCT14ANG | PDIP−14 (Pb−Free) | |
| MC74HCT14AD | SOIC−14 | 55 Units / Rail |
| MC74HCT14ADG | SOIC−14 (Pb−Free) | |
| MC74HCT14ADR2 | SOIC−14 | 2500 / Tape & Reel |
| MC74HCT14ADR2G | SOIC−14 (Pb−Free) | |
| MC74HCT14ADTR2 | TSSOP−14* | |
| MC74HCT14ADTR2G | TSSOP−14* | |
| MC74HCT14AFEL | SOEIAJ−14 | 2000 / Tape & Reel |
| MC74HCT14AFELG | SOEIAJ−14 (Pb−Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | (Referenced to GND) | −0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | (Referenced to GND) | −0.5 to $V_{CC}$ +0.5 | V |
| $V_O$ | DC Output Voltage | (Referenced to GND) | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | DC Input Diode Current | | ±20 | mA |
| $I_{OK}$ | DC Output Diode Current | | ±25 | mA |
| $I_O$ | DC Output Sink Current | | ±25 | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | | ±50 | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | | ±50 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance | PDIP<br>SOIC<br>TSSOP | 78<br>125<br>170 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 85°C | PDIP<br>SOIC<br>TSSOP | 750<br>500<br>450 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 30% − 35% | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 1)<br>Machine Model (Note 2)<br>Charged Device Model (Note 3) | >4000<br>>300<br>>1000 | V |
| $I_{Latchup}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 85°C (Note 4) | ±300 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.
5. For high frequency or heavy load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | (Referenced to GND) | 4.5 | 5.5 | V |
| $V_I$, $V_O$ | DC Input Voltage, Output Voltage | (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | | − | (Note 6) | ns |

6. No Limit when $V_I \approx 50\%$ $V_{CC}$, $I_{CC} > 1$ mA.
7. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ Volts | Temperature Limit −55°C to 25°C Min | −55°C to 25°C Max | ≤85°C Min | ≤85°C Max | ≤125°C Min | ≤125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ max | Maximum Positive−Going Input Threshold Voltage | $V_O$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | | 1.9<br>2.1 | | 1.9<br>2.1 | | 1.9<br>2.1 | V |
| $V_{T+}$ min | Minimum Positive−Going Input Threshold Voltage | $V_O$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | 1.2<br>1.4 | | 1.2<br>1.4 | | 1.2<br>1.4 | | V |
| $V_{T-}$ max | Maximum Negative−Going Input Threshold Voltage | $V_O$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | | 1.2<br>1.4 | | 1.2<br>1.4 | | 1.2<br>1.4 | |
| $V_{T-}$ min | Minimum Negative−Going Input Threshold Voltage | $V_O$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | 0.5<br>0.6 | | 0.5<br>0.6 | | 0.5<br>0.6 | | |
| $V_H$ max | Maximum Hysteresis Voltage | $V_O$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | | 1.4<br>1.5 | | 1.4<br>1.5 | | 1.4<br>1.5 | |
| $V_H$ min | Minimum Hysteresis Voltage | $V_O$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | 0.4<br>0.4 | | 0.4<br>0.4 | | 0.4<br>0 4 | | |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_I < V_{T-}$ min<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | 4.4<br>5.4 | | 4.4<br>5.4 | | 4.4<br>5.4 | | V |
| | | $V_I < V_{T-}$ min<br>$\|I_{out}\| \le 4.0$ mA | 4.5 | 3.98 | | 3.84 | | 3.7 | | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_I \ge V_{T+}$ max<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | | 0.1<br>0.1 | | 0.1<br>0.1 | | 0.1<br>0.1 | V |
| | | $V_I \ge V_{T+}$ max<br>$\|I_{out}\| \le 4.0$ mA | 4.5 | | 0.26 | | 0.33 | | 0.4 | |
| $I_{IK}$ | Maximum Input Leakage Current | $V_I = V_{CC}$ or GND | 5.5 | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per package) | $V_I = V_{CC}$ or GND<br>$I_{out}$ = 0 μA | 5.5 | | 1.0 | | 10 | | 40 | μA |
| | | | | ≥ −55°C | | 25°C to 125°C | | | | |
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_I$ = 2.4 V, Any One Input<br>$V_I = V_{CC}$ or GND, Other Inputs<br>$I_{out}$ = 0 μA | 5.5 | 2.9 | | 2.4 | | | | mA |

8. Information on typical parametric values can be found in the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

**AC CHARACTERISTICS** ($C_L$ = 50 pF; Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | Test Conditions | Figures | Guaranteed Limit −55°C to 25°C Min | −55°C to 25°C Max | ≤85°C Min | ≤85°C Max | ≤125°C Min | ≤125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | |
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, Input A to Output Y (L to H) | $V_{CC}$ = 5.0 V ±10%<br>$C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns | 1 & 2 | | 32 | | 40 | | 48 | ns |
| $t_{TLH}$,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output | $V_{CC}$ = 5.0 V ± 10%<br>$C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns | 1 & 2 | | 15 | | 19 | | 22 | ns |

9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance, per Inverter (Note 10) | 32 | pF |

10. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

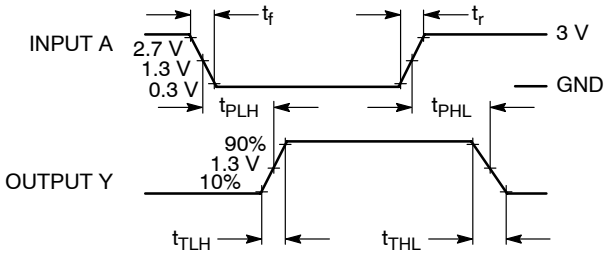
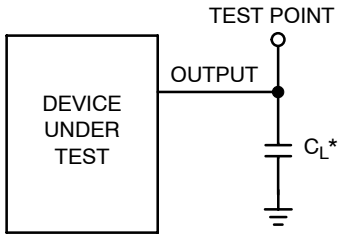



**Figure 1. Switching Waveforms**

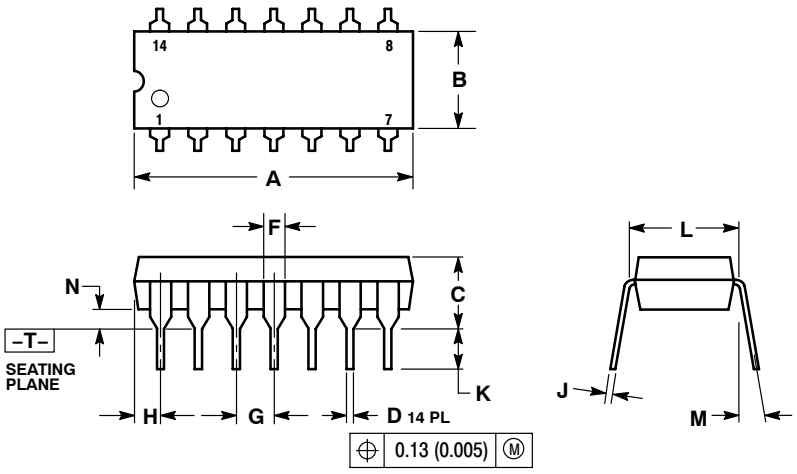



*Includes all probe and jig capacitance.

**Figure 2. Test Circuit**

## PACKAGE DIMENSIONS

**PDIP−14**
CASE 646−06
ISSUE P

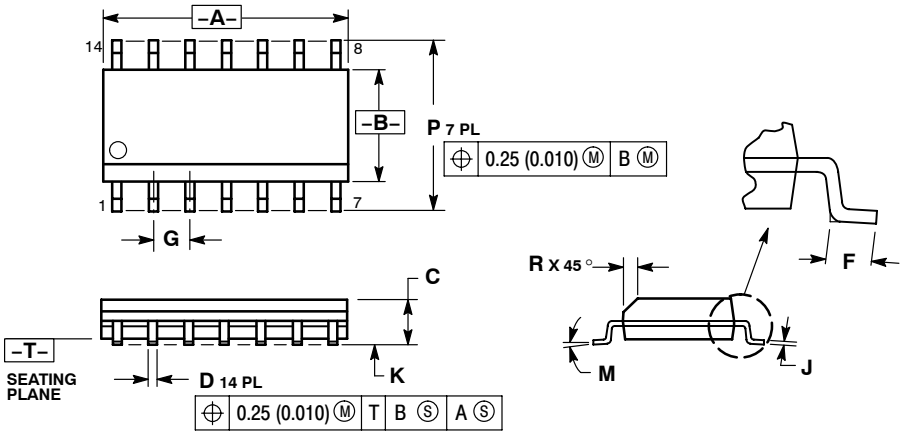



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | −−− | 10 ° | −−− | 10 ° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

## PACKAGE DIMENSIONS

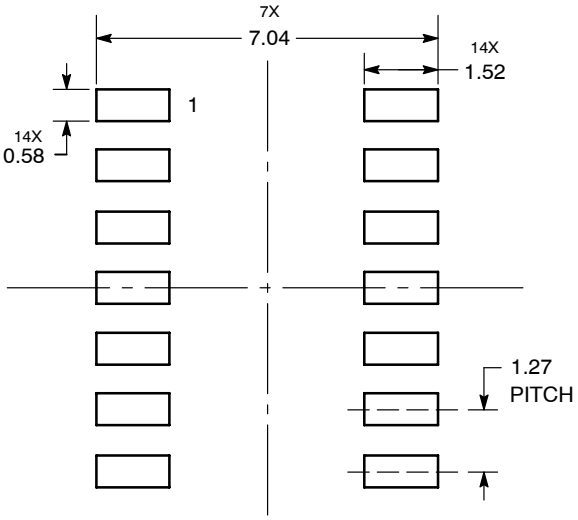
**SOIC−14**
CASE 751A−03
ISSUE H




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

### SOLDERING FOOTPRINT*

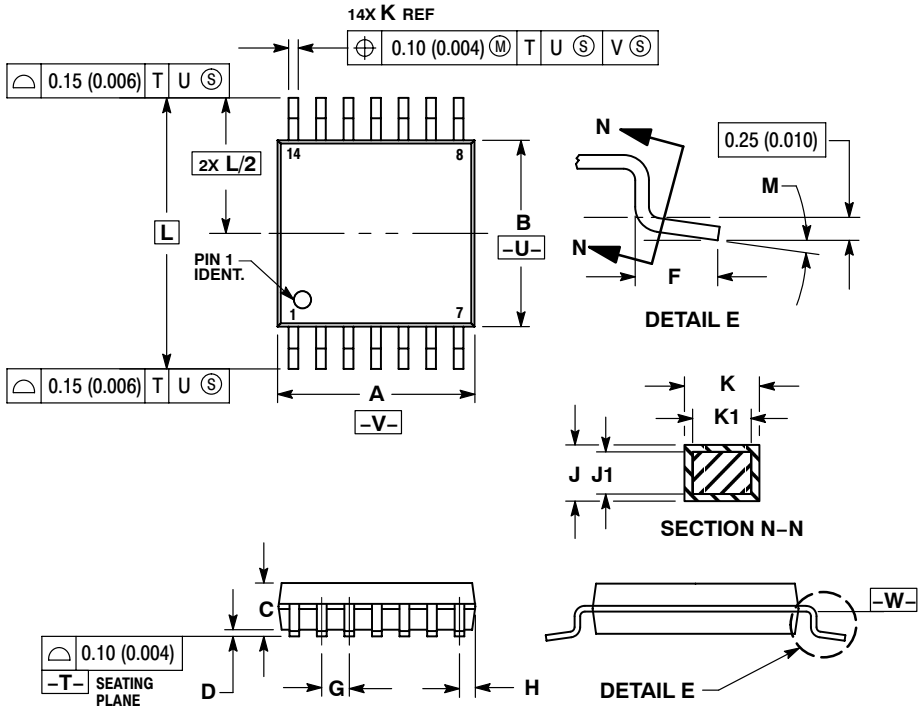



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

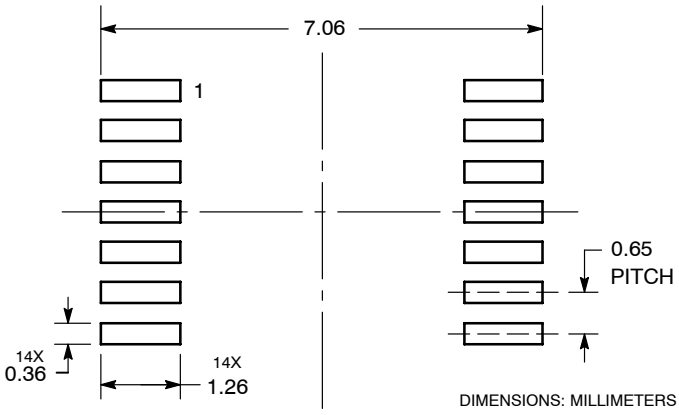
**TSSOP−14**
CASE 948G−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### SOLDERING FOOTPRINT*

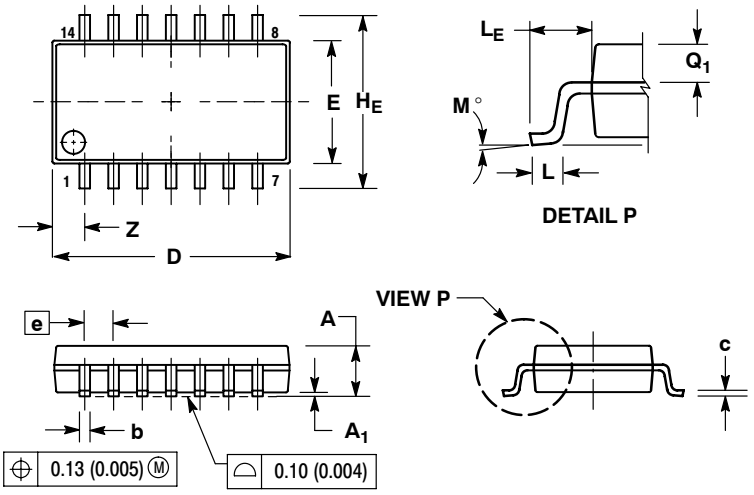



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HCT14A

## PACKAGE DIMENSIONS

**SOEIAJ−14**
CASE 965−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.004 | 0.008 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| 0.50 | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |



## PUBLICATION ORDERING INFORMATION

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