

# NL27WZ00

## Dual 2-Input NAND Gate

The NL27WZ00 is a high performance dual 2-input NAND Gate operating from a 1.65 V to 5.5 V supply.

### Features

- Extremely High Speed:  $t_{PD}$  2.4 ns (typical) at  $V_{CC} = 5.0$  V
- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- Over Voltage Tolerant Inputs
- LVTTL Compatible – Interface Capability With 5.0 V TTL Logic with  $V_{CC} = 3.0$  V
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Replacement for NC7WZ00
- Chip Complexity: FET = 112
- Pb-Free Package is Available

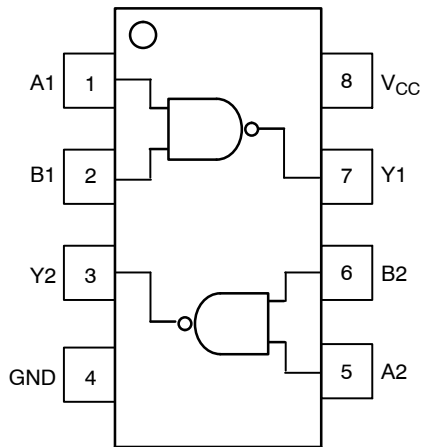


Figure 1. Pinout

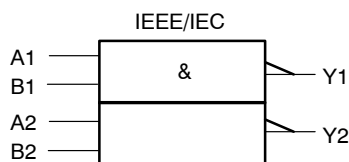
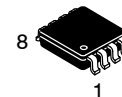


Figure 2. Logic Symbol



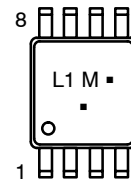
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**US8  
US SUFFIX  
CASE 493**

### MARKING DIAGRAM



- L1 = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### PIN ASSIGNMENT

Pin	Function
1	A1
2	B1
3	Y2
4	GND
5	A2
6	B2
7	Y1
8	$V_{CC}$

### FUNCTION TABLE

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NL27WZ00

## MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage	$V_I$	-0.5 to +7.0	V
DC Output Voltage	$V_O$	-0.5 to +7.0	V
DC Input Diode Current $V_I < \text{GND}$	$I_{IK}$	-50	mA
DC Output Diode Current $V_O < \text{GND}$	$I_{OK}$	-50	mA
DC Output Sink Current	$I_O$	$\pm 50$	mA
DC Supply Current per Supply Pin	$I_{CC}$	$\pm 100$	mA
DC Ground Current per Ground Pin	$I_{GND}$	$\pm 100$	mA
Storage Temperature Range	$T_{STG}$	-65 to +150	$^{\circ}\text{C}$
Lead Temperature, 1 mm from Case for 10 Seconds	$T_L$	260	$^{\circ}\text{C}$
Junction Temperature under Bias	$T_J$	+150	$^{\circ}\text{C}$
Thermal Resistance (Note 1)	$\theta_{JA}$	250	$^{\circ}\text{C}/\text{W}$
Power Dissipation in Still Air at 85 $^{\circ}\text{C}$	$P_D$	250	mW
Moisture Sensitivity	MSL	Level 1	
Flammability Rating Oxygen Index: 28 to 34	$F_R$	UL 94 V-0 @ 0.125 in	
ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	$V_{ESD}$	> 2000 > 200 N/A	V
Latchup Performance Above $V_{CC}$ and Below GND at 85 $^{\circ}\text{C}$ (Note 5)	$I_{Latchup}$	$\pm 500$	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage Operating Data Retention Only	$V_{CC}$	1.65 1.5	5.5 5.5	V
Input Voltage (Note 6)	$V_I$	0	5.5	V
Output Voltage (HIGH or LOW State)	$V_O$	0	$V_{CC}$	V
Operating Free-Air Temperature	$T_A$	-55	+125	$^{\circ}\text{C}$
Input Transition Rise or Fall Rate $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ $V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	$\Delta t/\Delta V$	0 0 0	20 10 5	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

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## DC ELECTRICAL CHARACTERISTICS

Parameter	Condition	Symbol	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
High-Level Input Voltage		V <sub>IH</sub>	1.65 2.3 to 5.5	0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub>			0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub>		V
Low-Level Input Voltage		V <sub>IL</sub>	1.65 2.3 to 5.5			0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub>		0.25 0.3 V <sub>CC</sub>	V
High-Level Output Voltage V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -100 μA I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -16 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -32 mA	V <sub>OH</sub>	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V <sub>CC</sub> - 0.1 1.29 1.9 2.2 2.4 2.5 3.8	V <sub>CC</sub> 1.5 2.1 2.4 2.7 2.5 4.0		V <sub>CC</sub> - 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>OH</sub>	I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 32 mA	V <sub>OL</sub>	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.0 0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	I <sub>IN</sub>	0 to 5.5			±0.1		±1.0	μA
Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	I <sub>CC</sub>	5.5			1.0		10	μA

## AC ELECTRICAL CHARACTERISTICS t<sub>R</sub> = t<sub>F</sub> = 3.0 ns

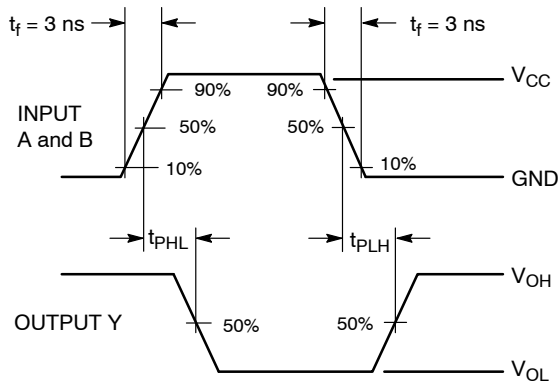
Parameter	Condition	Symbol	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
Propagation Delay (Figure 3 and 4)	R <sub>L</sub> = 1 MΩ, C <sub>L</sub> = 15 pF	t <sub>PLH</sub> t <sub>PHL</sub>	1.8 ± 0.15	2.0	5.7	10.5	2.0	11.0	ns
			2.5 ± 0.2	1.2	3.2	5.3	1.2	5.7	
	R <sub>L</sub> = 1 MΩ, C <sub>L</sub> = 15 pF		3.3 ± 0.3	0.8	2.4	3.7	0.8	4.0	
			R <sub>L</sub> = 500 Ω, C <sub>L</sub> = 50 pF	1.2	3.0	4.6	1.2	4.9	
			R <sub>L</sub> = 1 MΩ, C <sub>L</sub> = 15 pF	5.0 ± 0.5	0.5	1.9	2.9	0.5	
R <sub>L</sub> = 500 Ω, C <sub>L</sub> = 50 pF	0.8	2.4	3.6	0.8	3.9				

## CAPACITIVE CHARACTERISTICS

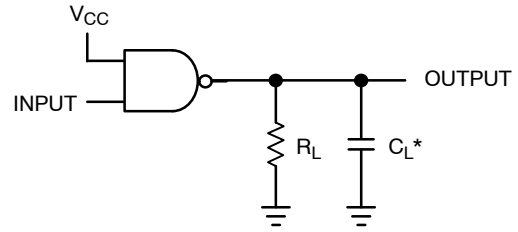
Parameter	Condition	Symbol	Typical	Unit
Input Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	C <sub>IN</sub>	2.5	pF
Power Dissipation Capacitance (Note 7)	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	C <sub>PD</sub>	9	pF
	10 MHz, V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>		11	

7. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

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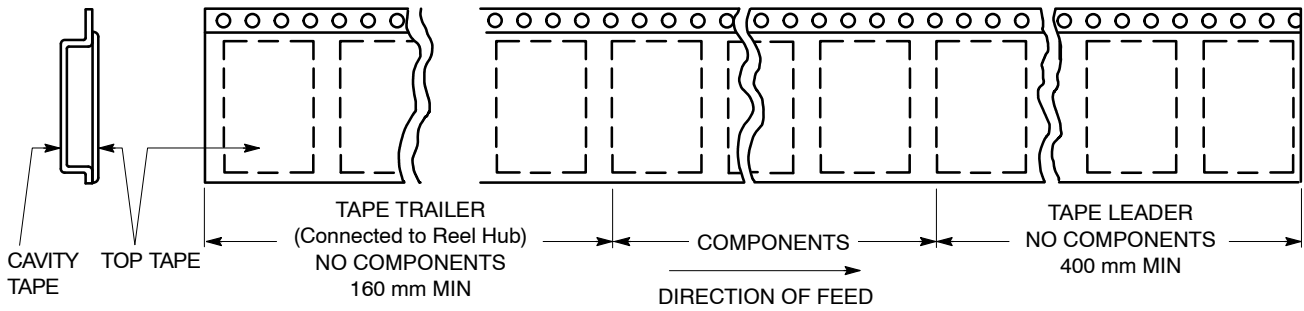


**Figure 3. Switching Waveform**

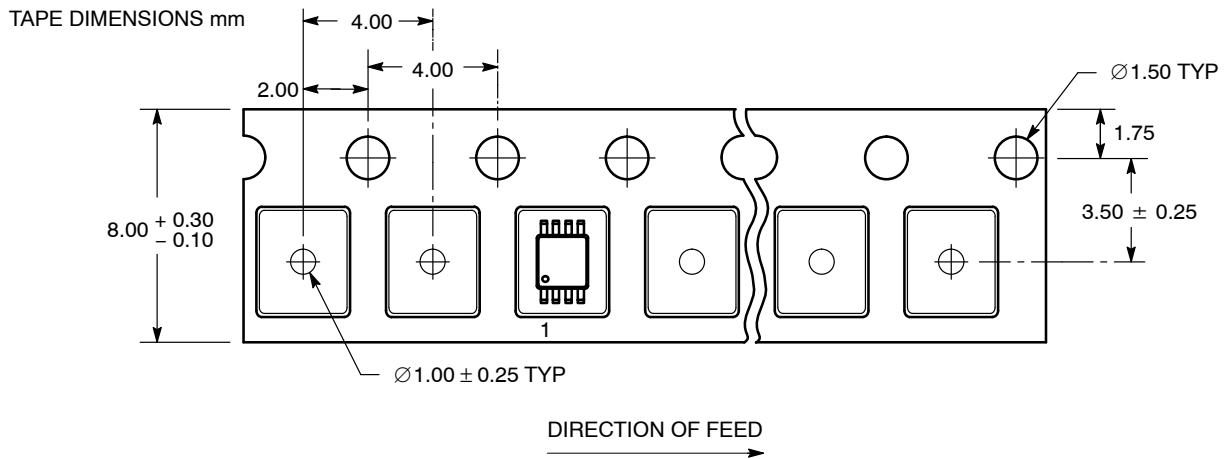


\*C<sub>L</sub> includes all probe and jig capacitances.  
A 1-MHz square input wave is recommended for propagation delay tests.

**Figure 4. Test Circuit**



**Figure 5. Tape Ends for Finished Goods**



**Figure 6. US8 Reel Configuration/Orientation**

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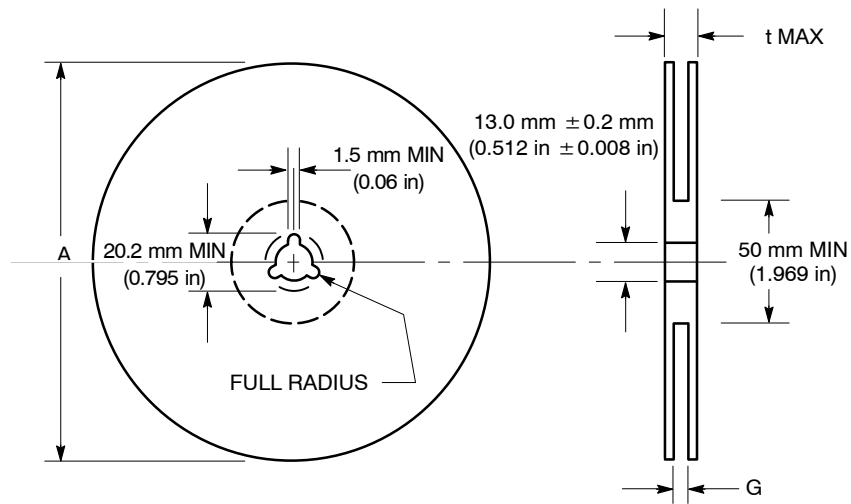


Figure 7. Reel Dimensions

## REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	US	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

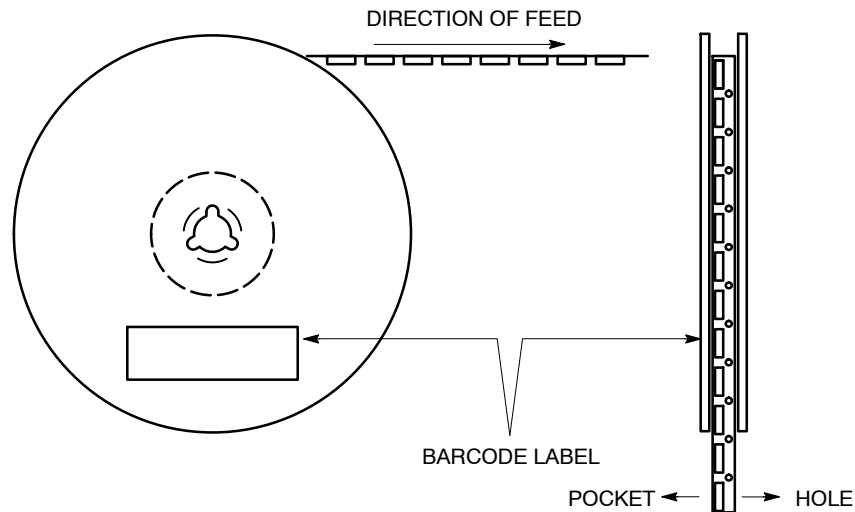


Figure 8. Reel Winding Direction

## ORDERING INFORMATION

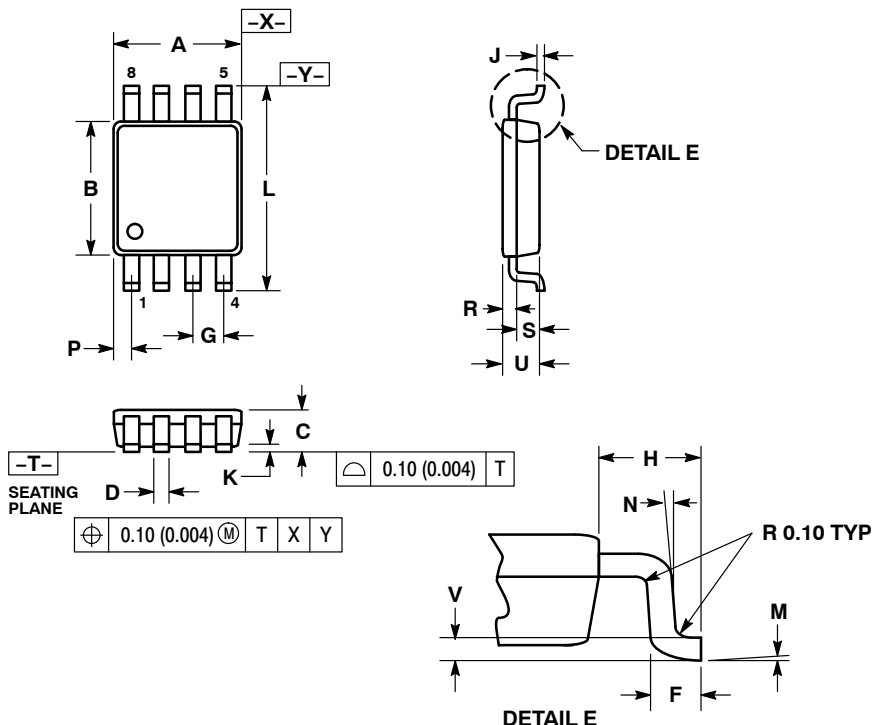
Device	Device Nomenclature						Package	Shipping†
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix		
NL27WZ00US	NL	2	7	WZ	00	US	US8	3000/Tape & Reel
NL27WZ00USG								

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

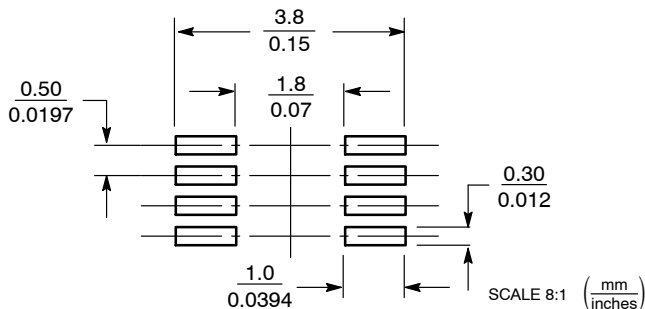
US8  
CASE 493-02  
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 °).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 ").

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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